Low Cost, High-Density Digital Electronics for Nuclear Physics

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Outline

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  - Example experiment with 1,359 digital DAQ channels.
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- Questions for the NP community.

Description of Phase II project

Problem or situation that is being addressed.

In Nuclear Physics there is need for cost effective, high density data acquisition (DAQ) systems with hundreds or even thousands of channels capable of signal monitoring and analysis.

How this problem or situation is being addressed.

We are developing digital DAQ modules with dozens of channels of waveform digitization, on-board FPGA, Ethernet, USB-2, and VME interfaces, and running Linux on-board.

The deliverables.

- The products will be scalable, from a single-channel table-top units, all the way to systems with thousands of channels.
- The table top units will serve small NP experiments, radiation detector development, or student labs teaching Nuclear Physics.
- Larger systems will serve experiments conducted at DOE facilities, e.g., Facility for Rare Isotope Beams (FRIB), which is a new national user facility for Nuclear Physics.

The company and its capabilities

We focus on data acquisition (DAQ) for nuclear physics, high energy physics, and particle astrophysics.

Our instruments use digital techniques to acquire and process signals from nuclear radiation detectors.

Our capabilities:

- Electronic design “top to bottom”: from the requirements, through schematic capture and board layout, all the way to prototyping, production, and support.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors, with special focus on Embedded Linux.
- Algorithms for pulse processing.
- Algorithm implementation in the FPGA (VHDL, Verilog) and in embedded processors (python, C).
- Development of nuclear radiation detector readout using vacuum or silicon photomultipliers.

Our customers

University of Rochester

Los Alamos National Laboratory

Houghton College

Fermilab

The University of Tennessee Knoxville

Wiener Plein & Baus, Corp.

Albert Einstein Center for Fundamental Physics

Universität Bern

SFU Simon Fraser University Engaging the World

Université Laval

上海交通大學 Shanghai Jiao Tong University

We Are Building DAQ Electronics for Dark Matter Search

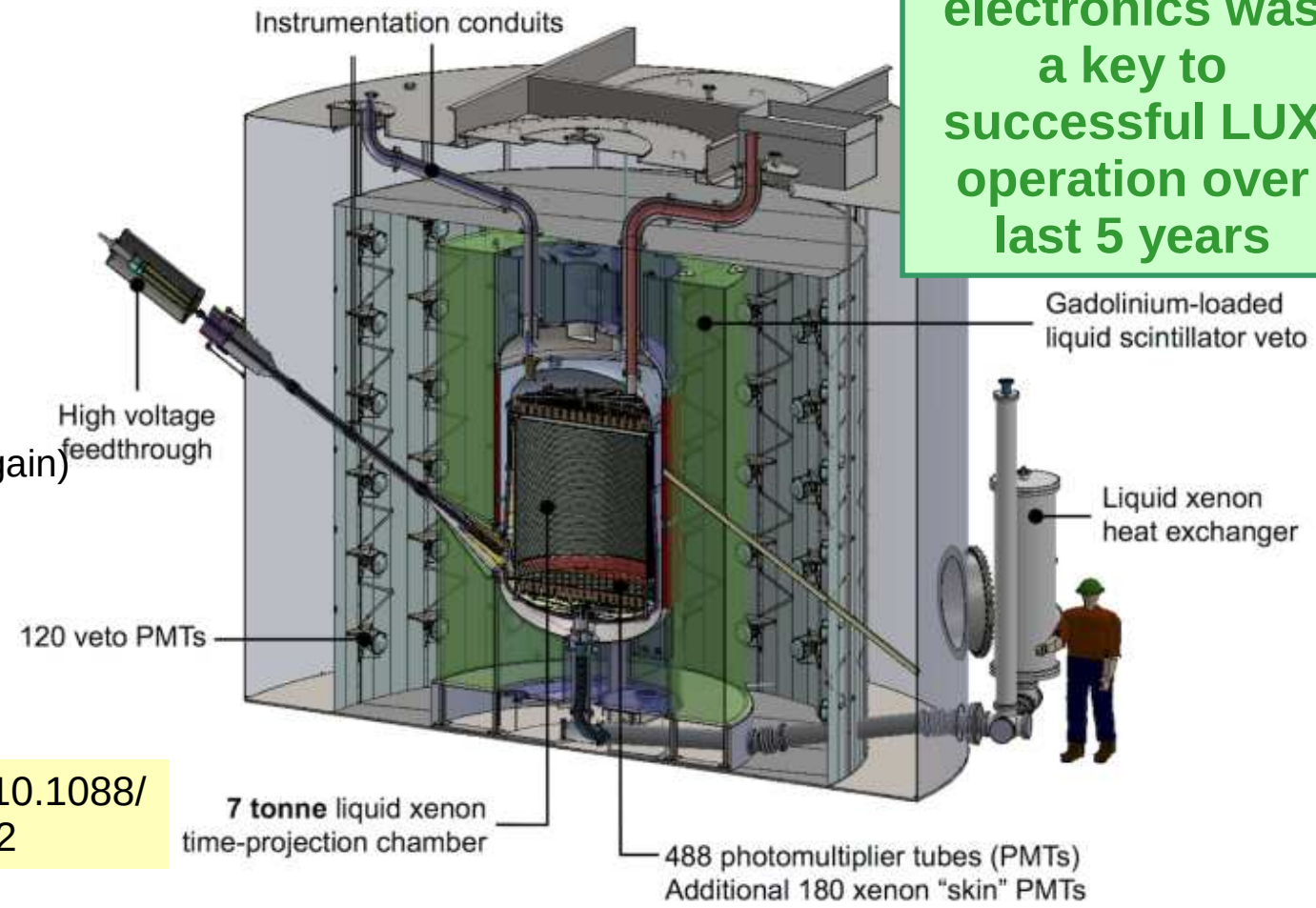
SkuTek collaboration with UofR Physics and Astronomy

LUX-Zepplin is the “ultimate Dark Matter Search Detector”. Together with UofR we are building the digital DAQ for LZ with **1,359** channels. **(Non-SBIR funding!)**

SkuTek Digital Trigger electronics was a key to successful LUX operation over last 5 years

- Amount of Xenon:
  - 5.6 tons fiducial
  - 7 tons in the vessel
  - 10 tons total.
  - Drift time in Xenon: 700 μs.
- Number of PMTs:
  - 494 main volume (dual gain)
  - 131 “skin”
  - 120 outer detector veto (dual gain)
  - Total **745** PMTs.
- Electronic channels:

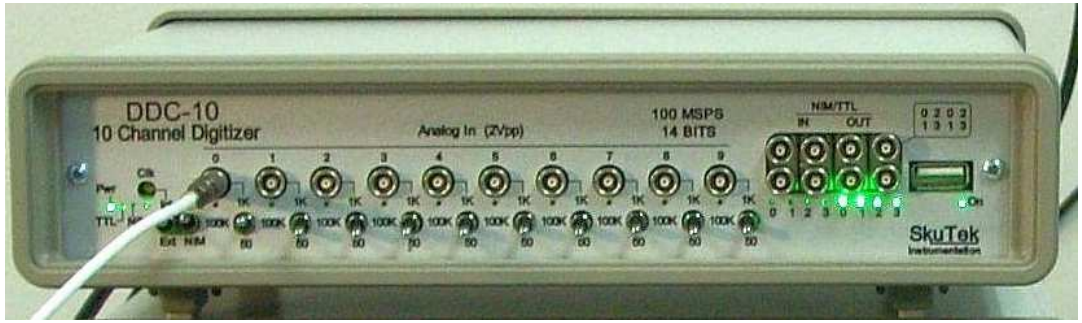
  2*494 + 131 + 2*120 = **1,359**.



http://iopscience.iop.org/article/10.1088/1748-0221/11/02/C02072

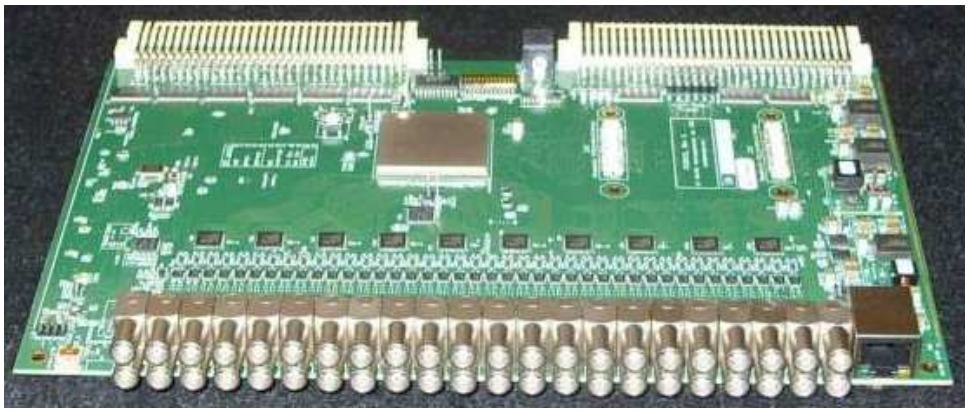
DAQ Products: VME Modules and Table Top Units

Standalone networked digitizer (10 channels)



Low cost networked digitizer (2 channels)

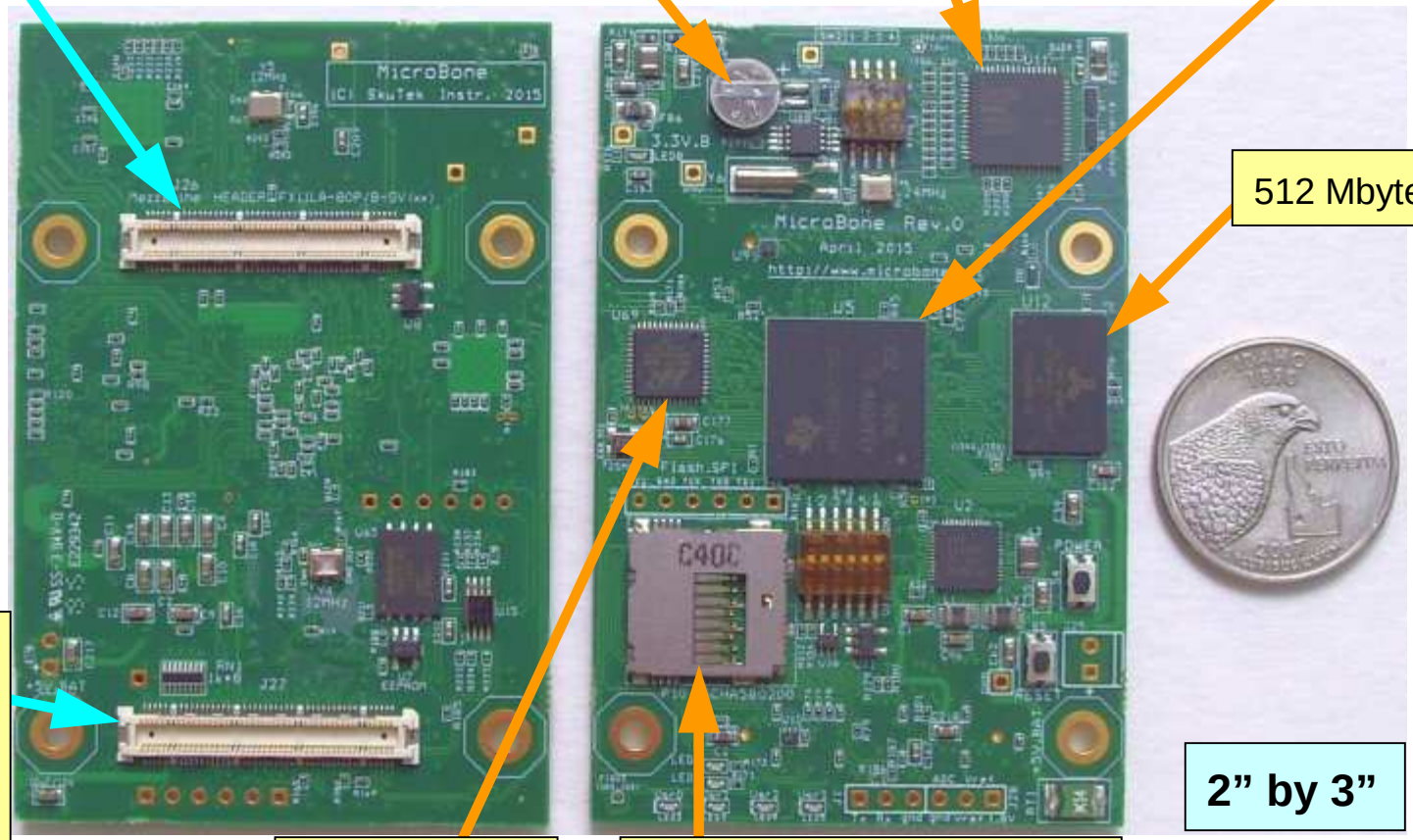
VME digitizer: 40 channels



VME trigger module

We Use Embedded Linux for Monitoring and Control

- We developed the ARM Linux System on Module (SOM) with a low-power 1 GHz ARM processor.
- It will provide a (much needed!) real-time monitoring and diagnostics. The experimenter will NOT have to wait minutes (or hours…) until the data percolates through the analysis cluster to see if the detector channels are working.



Linux SOM Mounted Inside the 10-Channel Digitizer

- System-on-Module running Linux is setting up the FPGA and then reading data.
- The control software was written in C and Python, using Jupyter web interface.
- The FPGA is mapped as memory in the Linux address space.

This digitizer was used during the test.

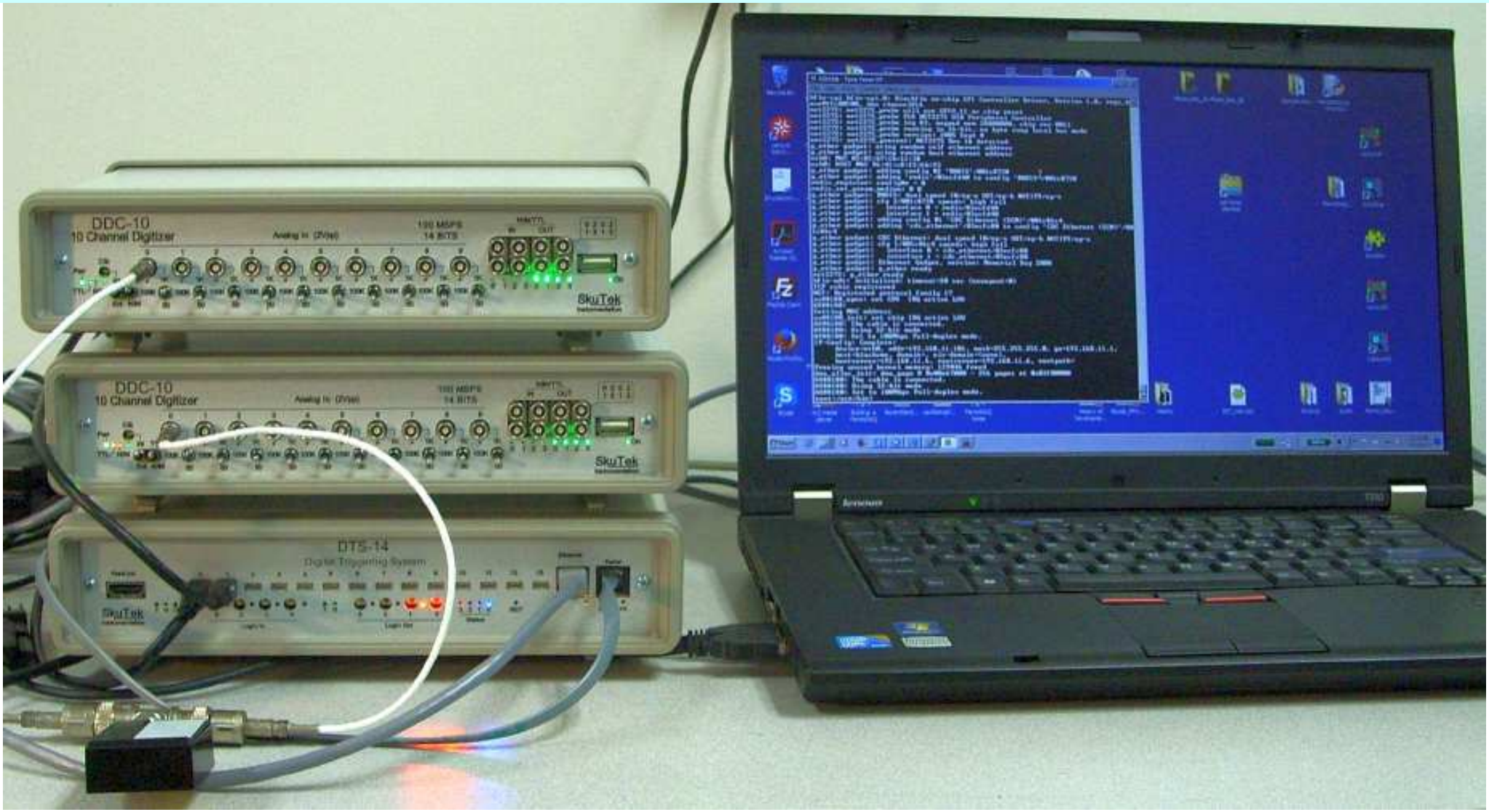
Linux SOM

System Prototype Test

Two 10-channel Digitizers + Trigger / Logic DAQ Manager

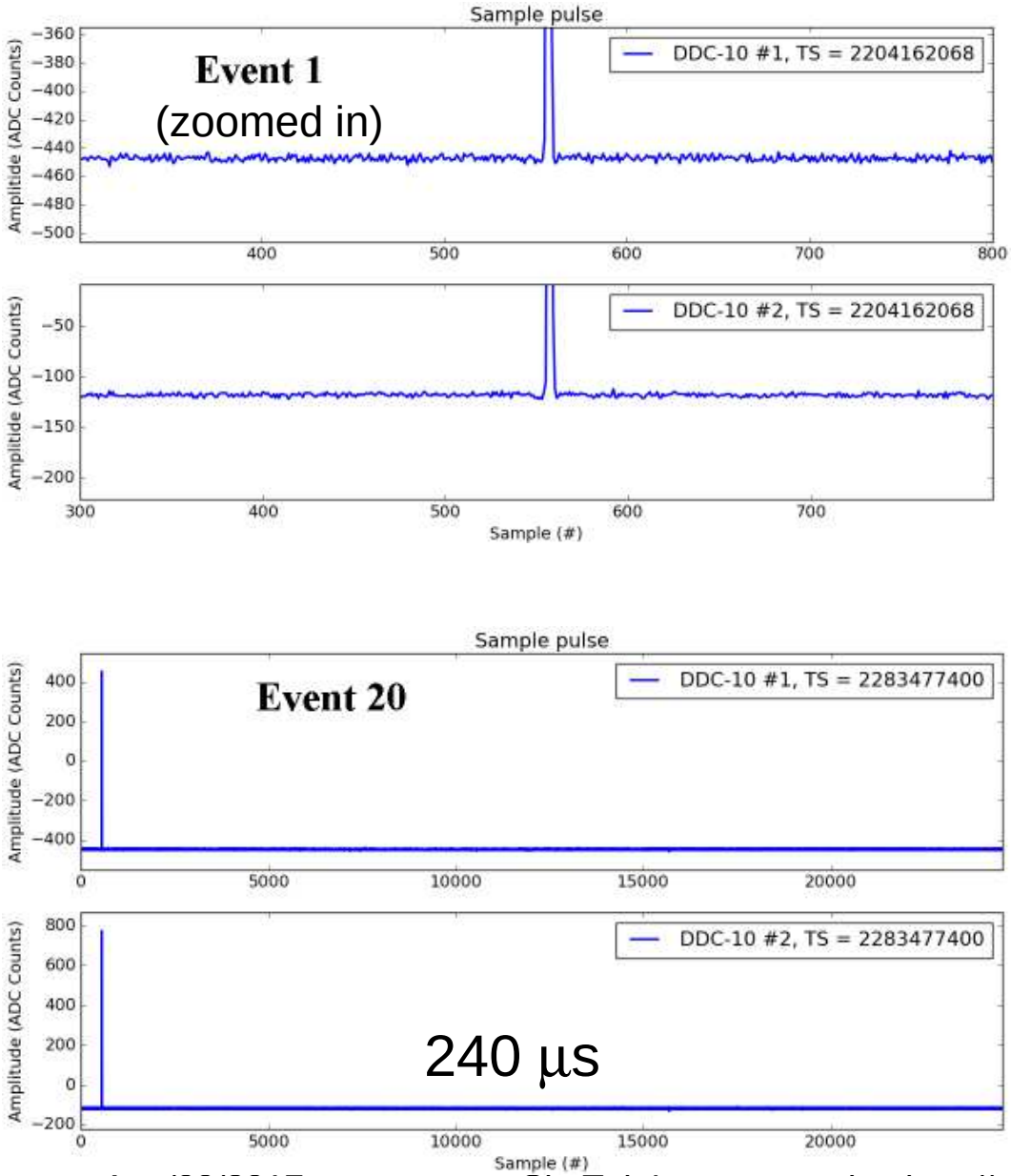
Both digitizers run the same ADC clock and Time Stamp (from the DAQ Manager)

Both digitizers write separate binary event files with time stamped waveforms

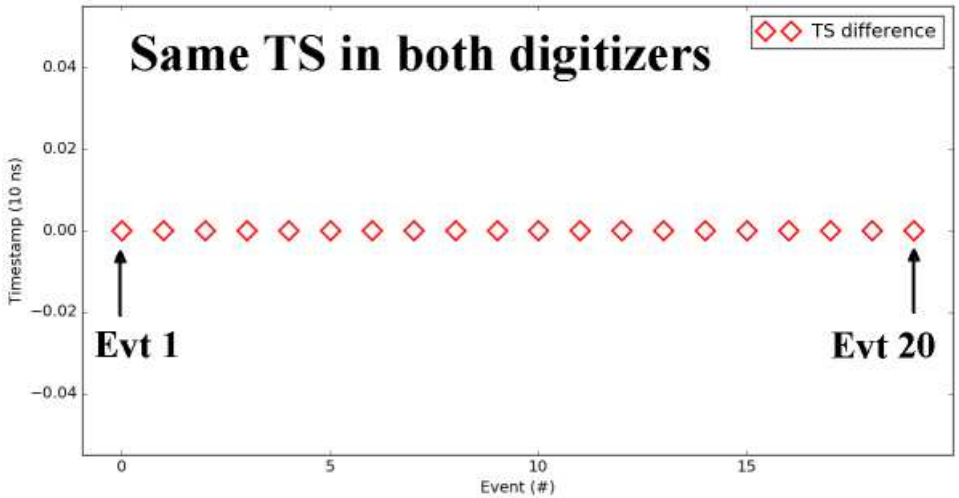


Time Stamp and ADC Clock Synchronization

Time stamps and ADC clock synchronized in both digitizers and the DAQ Manager



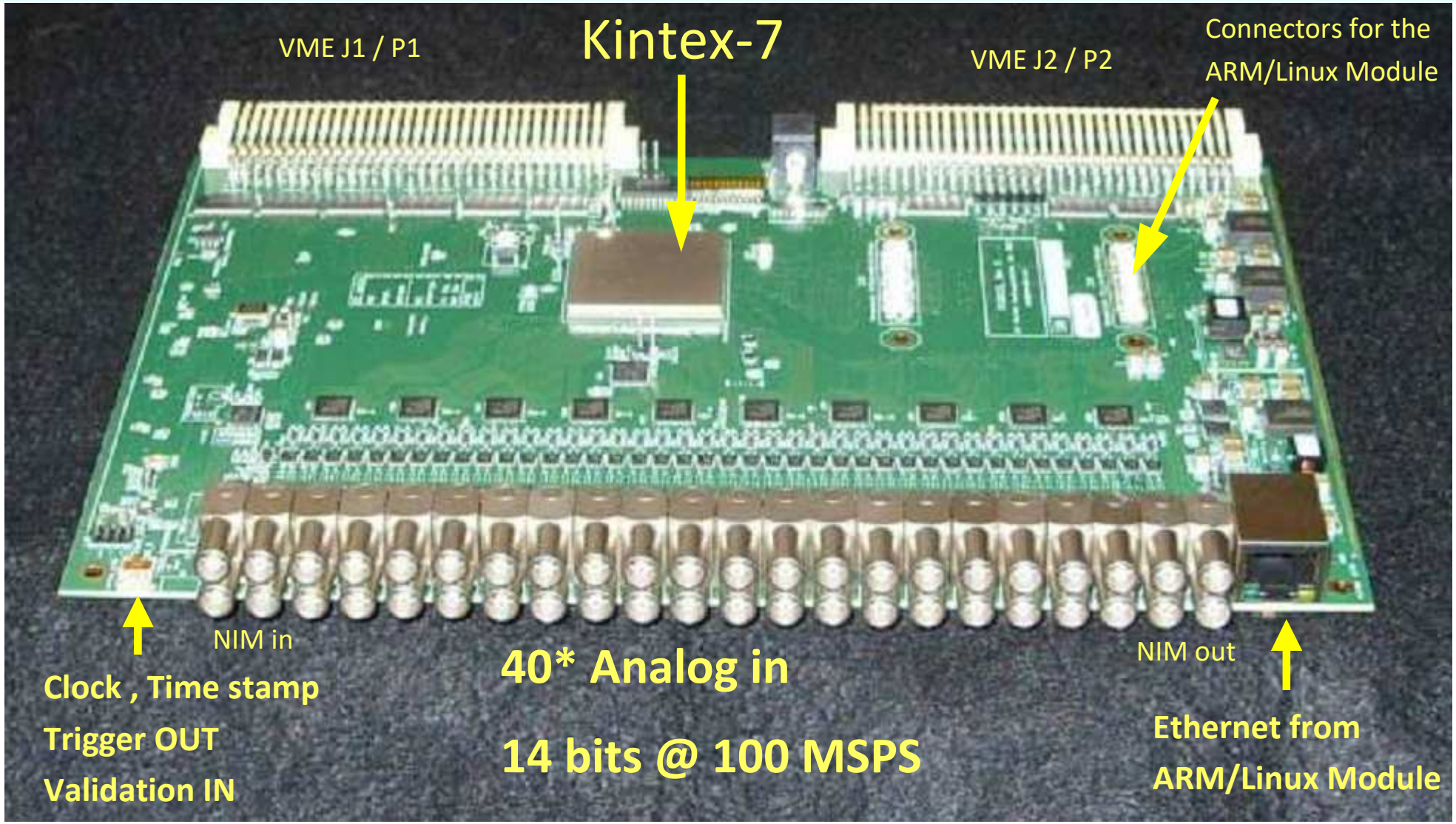
TS granularity = 10 ns
All three modules in synch



Time span = 79.315 ms

The Highlight: 40-Channel Digitizer With Kintex-7

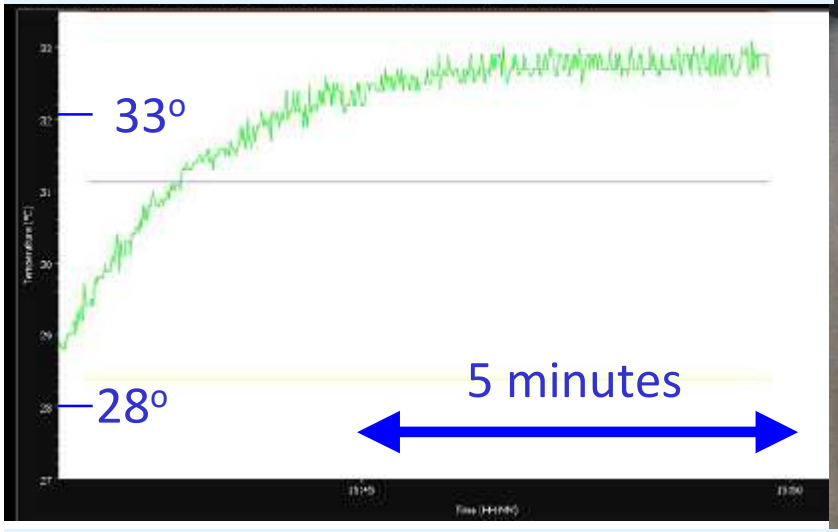
- Waveform time span: **222.5** µs or **397.5** µs per channel, depending on the FPGA size.
- Low RMS noise: **162 µV** = **1.33** LSB (shown on the next slides).
- Mentioned by Robert Janssens (ANL) in his closing remarks during plenary LECM session.

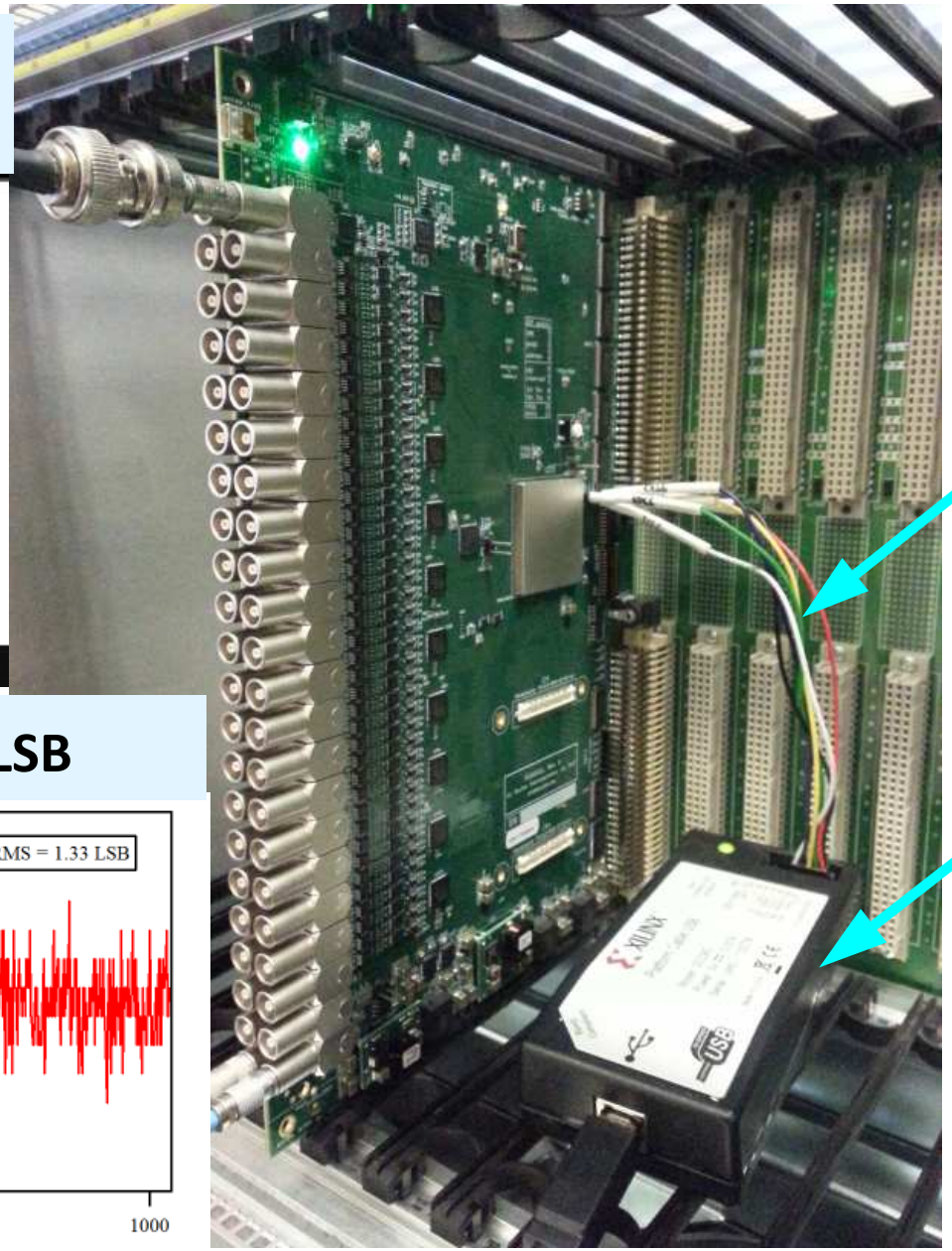


DDC-40 Digitizer in the VME Crate

One board **is here at the meeting**, the 2nd prototype is now being tested.

Temperature of the FPGA measured with the internal FPGA sensor.

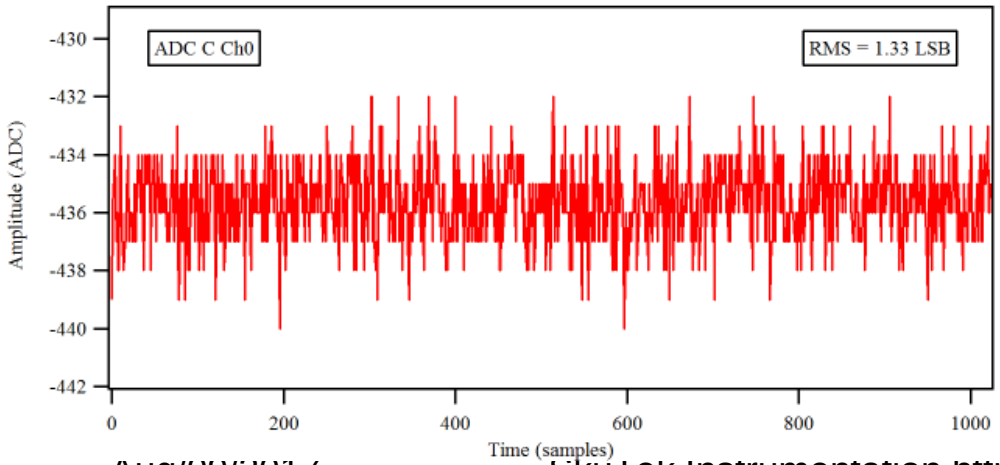




JTAG Cable

Xilinx JTAG interface

The waveform: RMS = 1.33 LSB

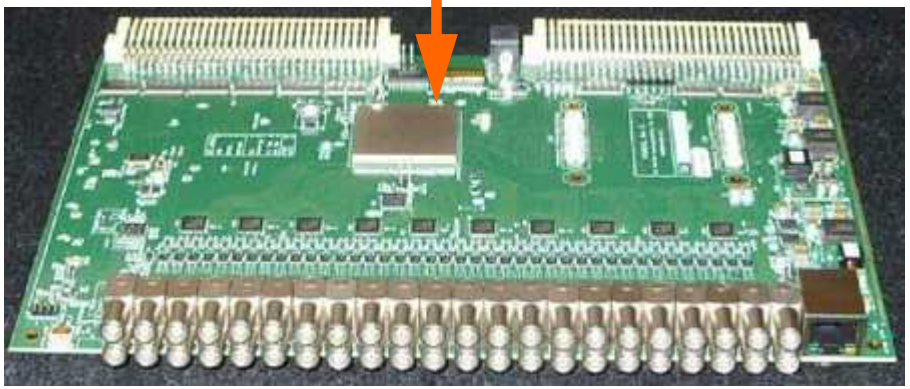


The Future Begins Today

- The entire GRETA crystal (36 segments + central contact) can be processed in one place, using a very powerful modern FPGA.
- Waveform time span: **397.5** µs per channel. It will be needed for in-depth crystal studies.

5x more logic, **15x** more DSP slices, and **15x** more memory than the present GRETINA digitizer

Start your firmware development TODAY.



No need for a separate SW development machine:

- The board itself runs Python and Jupyter.
- The board runs the C/C++ compiler.
- The board runs X-windows….
- The board can mount remote disks (NFS, SAMBA).
- The board can record data to the SD card (64 GB).

Signals from one GRETA crystal in one place

No need for a VME crate. Just use **Ethernet**.

A complete DAQ and development system in one box.

Summary of Technical Achievements

- 40-channel digitizer has been designed. Two prototypes (80 channels) were built and tested.
- All 80 channels performed flawlessly after I replaced one cracked resistor in one channel.
- Five 10-channel units were built and tested. Two units were already shipped to a customer.
- A small scale DAQ System test was performed (two digitizers + Trigger Module).
  - ADC clock distribution, time stamping, and triggering among two digitizers and the TM.
  - Event time stamping was accurate to 10 ns, using a shared ADC clock.
  - The digitizers were controlled and set up using embedded Jupyter interfaces. (I.e., iPython.)
  - Both digitizers wrote separate, but coordinated binary data files.
  - The final event building was performed offline, based on time stamps in the event files.
  - All of the above mimics on a small scale, what the “big DAQ” is supposed to do.
  - The three-module system was shipped to a customer.
- The Embedded Linux SOM has proven its worth.
  - Easy software development: python is instantaneous, Jupyter is convenient.
  - C utilities are compiled on the board. A separate development machine is not needed!
- The know-how was used for designing an LZ digitizer with 32 channels (separate funding).

Future Plans

- Continue development of firmware and software for both digitizers (10 and 40 channel).
- Upgrade the Trigger / Logic Module to ARM and Kintex (ongoing, very advanced).
- Develop systems of many digitizers managed by Trigger / Logic DAQ Managers.
- Increase the reach of the inter-module links from meters to ~hundred meters.
  - This will allow to synchronize DAQ Systems deployed at separate locations.
- Develop 250 MHz versions of our low density modules (2 and 10 channels).
- **Implement interfaces between "small DAQ" and "big DAQ".**
  - Smaller groups need to participate in experiments with large detectors, using their own "small DAQ" systems. These need to be interfaced with the "big DAQ".
  - Currently, protocols and standards for DAQ to DAQ interfacing are hardly available.
  - The PI participates in the FRIB DAQ Working Group spearheaded by Robert Varner (ORNL). The Workgroup is developing guidelines to make the above possible.

    https://www.phy.ornl.gov/fribdaq/
  - SkuTek will use the FRIB DAQ Working Group guidelines, when they become available.

Questions for the NP Community

- The community needs to provide a set of guidelines and technical standards for the inter-DAQ communication and synchronization.
  - Such standards were crucial in the past. (E.g., NIM or CAMAC).
  - The intermodule communication standards are well developed (e.g., VME).
  - The inter-system standards are lacking.
  - It is not specified how to tie together separate DAQ systems.
    - How to exchange trigger, validation, time stamps, and other controls between separate DAQ systems, either developed in-house or delivered by the vendors?
    - A solution may be based on existing GRETINA / DGS trigger electronics (Myriad).
    - Is this solution “ad hoc” for today, or is it long range for the next decade?
    - The discussions are ongoing: https://www.phy.ornl.gov/fribdaq/

Acknowledgements

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Thank you for your attention.

Backup slides

Kintex-7 will improve the performance of our products

Kintex-7: more logic, more memory

- Spartan-6 was the best tradeoff between price and performance circa five years ago.
- The new Series-7 FPGAs now offers more digital resources at a reasonable cost.

Feature	XC3S5000 Spartan-3 a)	XC6SLX150 Spartan-6 b)	XC7K325T Kintex-7 c)	XC7K410T Kintex-7 c)	Relative to XC3S5000
Equivalent logic cells from Data Sheet	74,880	147,443	326,080	406,720	2.0 / 4.4 / **5.4**
Multiply-accumulate units	104 d)	180	840	1540	1.7 / 8.1 / **14.8**
Waveform memory (k samples) e)	104 k	268 k	890 k	1,590 k	2.6 / 8.6 / **15.3**
Balls per package	900	900	900	900	same
I/O pins	633	576	500	500	0.9 / 0.8 / 0.8
Price lowest speed grade (900 balls)	$166	$210	$1,032	$1,496	1.3 / 6.2 / 9.0
Price “our” speed grade (900 balls)	$191	$210	$1,550	$1,796	1.1 / 8.1 / 9.4
$$ per channel for 32+ channels f)	$5	$5	$40	$45	

a) XC3S5000 is used in present GRETINA digitizers. It is the community’s performance yardstick.

b) XC6SLX150 is used in our present 10-channel and 32-channel digitizers.

c) These pin compatible Kintex-7 chips will be used in our forthcoming high density digitizers (40 channels).

d) XC3S5000 provides multipliers without the built-in accumulate register.

e) Total number of block RAM bits divided by 18. Parity bits are considered not useful for waveform storage.

f) Approximate FPGA cost per channel for 32+ channels.

Linux System-On-Module Development Board

- The SOM is hosted by a development board.
- The entire Linux is contained on the MicroSD card. The entire Linux can be upgraded **in 10 seconds**.
- The RTC with battery keeps track of the wall clock. (No need to call NTP…)
- Eight analog pins can be individually configured as 12-bit ADC, 12-bit DAC, or 5V-tolerant logic I/Os.