

Low Cost, High-Density Digital Electronics for Nuclear Physics

Wojtek Skulski

Principal Investigator

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Outline

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- Questions for the NP community.

The company and its capabilities

We focus on data acquisition (DAQ) for nuclear physics, high energy physics, and particle astrophysics. Our instruments use digital techniques to acquire and process signals from nuclear radiation detectors.

Our capabilities:

- Electronic design “top to bottom”: from the requirements, through schematic capture and board layout, all the way to prototyping, production, and support.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors, with special focus on Embedded Linux.
- Algorithms for pulse processing.
- Algorithm implementation in the FPGA (VHDL, Verilog) and in embedded processors (python, C).
- Development of nuclear radiation detector readout using vacuum or silicon photomultipliers.

Our customers



Los Alamos National Laboratory

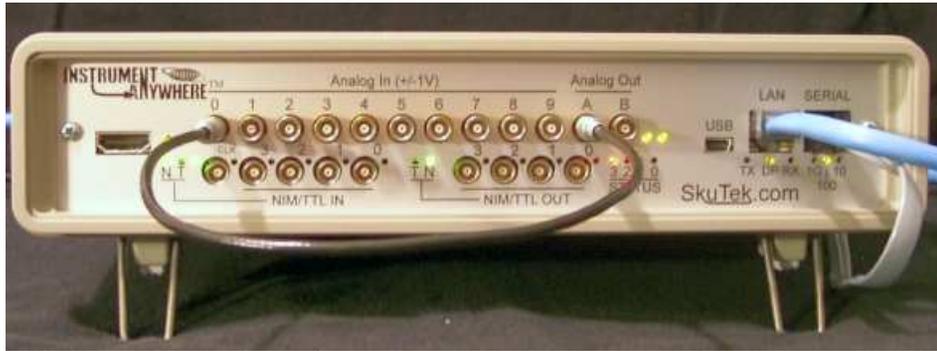


**Albert Einstein Center
for Fundamental
Physics**

**UNIVERSITÄT
BERN**

Products: VME modules and table top DAQ units

Standalone networked digitizer (10 channels)



Low cost networked digitizer (2 channels)



VME digitizer



VME trigger module



Description of Phase II project

Problem or situation that is being addressed.

In Nuclear Physics there is need for cost effective, high density data acquisition (DAQ) systems with hundreds or even thousands of channels capable of signal monitoring and analysis.

How this problem or situation is being addressed.

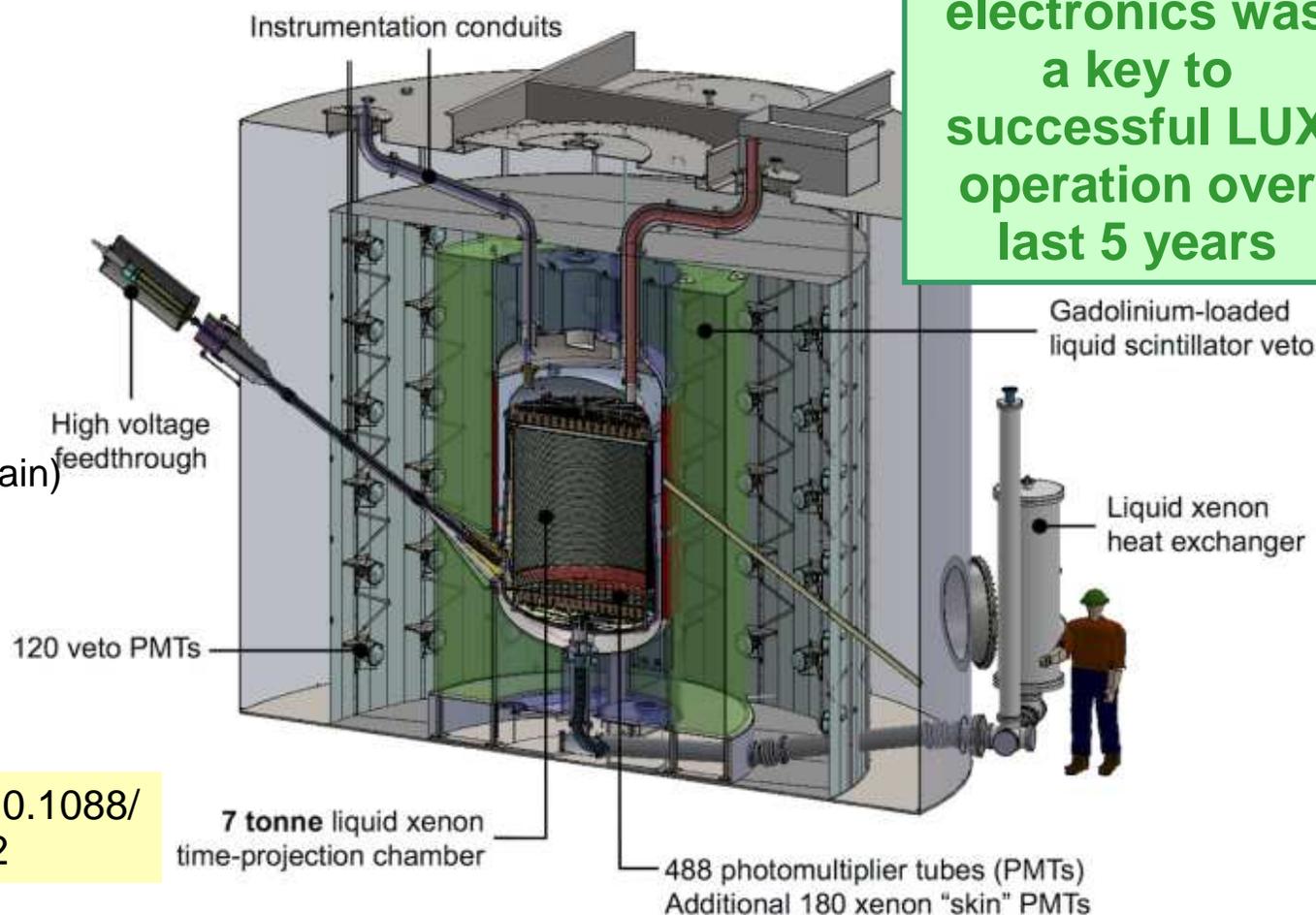
We are developing digital DAQ modules with dozens of channels of waveform digitization, on-board FPGA, Ethernet, USB-2, and VME interfaces, and running Linux on-board.

The deliverables.

- The products will be extremely scalable, from a single-channel table-top units, all the way to systems with thousands of channels.
- The table top units will serve small NP experiments, radiation detector development, or student labs teaching Nuclear Physics.
- Larger systems will serve experiments conducted at DOE facilities, e.g., Facility for Rare Isotope Beams (FRIB), which is a new national user facility for Nuclear Physics.

LUX-Zepplin is the “ultimate Dark Matter Search Detector” under development by 32 institutions. We are building the digital DAQ for LZ with **1,359** channels.

- Amount of Xenon:
 - 5.6 tons fiducial
 - 7 tons in the vessel
 - 10 tons total.
 - Drift time in Xenon: 700 μ s.
- Number of PMTs:
 - 494 main volume (dual gain)
 - 131 “skin”
 - 120 outer detector veto (dual gain)
 - Total **745** PMTs.
- Electronic channels:
 $2 \times 494 + 131 + 2 \times 120 = \mathbf{1,359}$.



SkuTek
Digital Trigger
electronics was
a key to
successful LUX
operation over
last 5 years

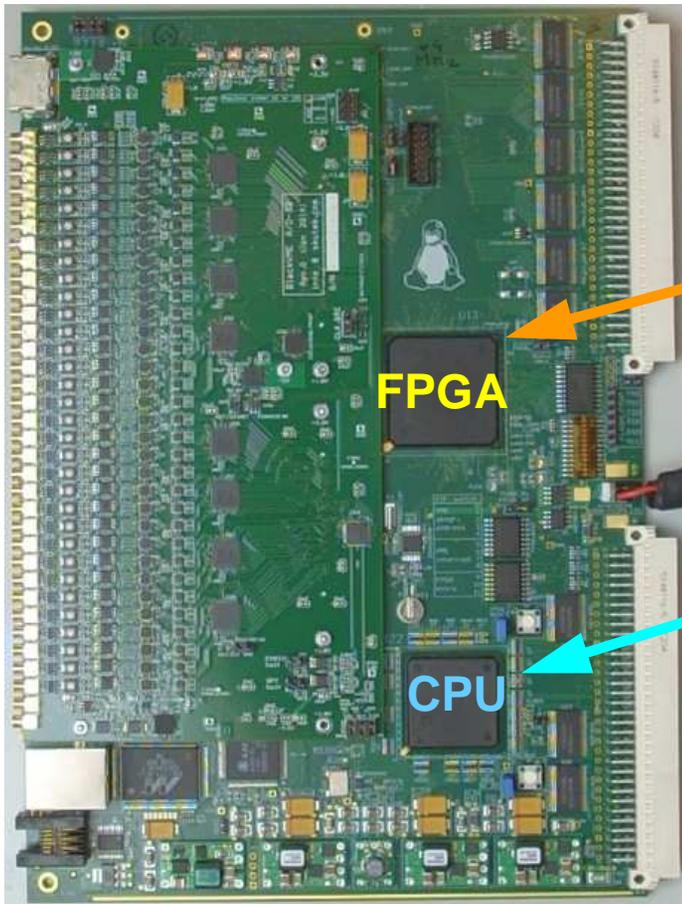
<http://iopscience.iop.org/article/10.1088/1748-0221/11/02/C02072>

Electronics for the Data Acquisition System

A modern digital DAQ is composed of digitizers and the Trigger / Logic modules. The current SkuTek designs employ Blackfin processors and Spartan-6 FPGAs. We are upgrading the electronics with **ARM processors** and **Kintex-7 FPGAs** in order to improve the performance.

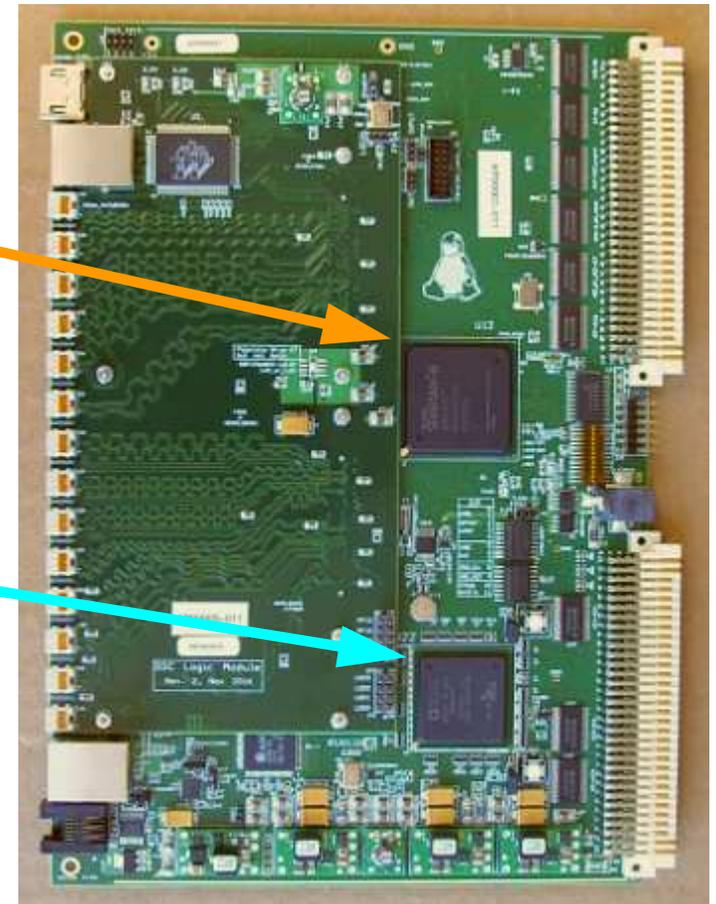
High density digitizer: **32 channels**

Trigger / Logic module: **14 inputs**



FPGA upgrade
Spartan-6 to Kintex-7

CPU upgrade
Blackfin to ARM



Kintex-7 will improve the performance of our products

Kintex-7: more logic, more memory

- Spartan-6 was the best tradeoff between price and performance circa five years ago.
- The new Series-7 FPGAs now offers more digital resources at a reasonable cost.

Feature	XC3S5000 Spartan-3 a)	XC6SLX150 Spartan-6 b)	XC7K325T Kintex-7 c)	XC7K410T Kintex-7 c)	Relative to XC3S5000
Equivalent logic cells from Data Sheet	74,880	147,443	326,080	406,720	2.0 / 4.4 / 5.4
Multiply-accumulate units	104 d)	180	840	1540	1.7 / 8.1 / 14.8
Waveform memory (k samples) e)	104 k	268 k	890 k	1,590 k	2.6 / 8.6 / 15.3
Balls per package	900	900	900	900	same
I/O pins	633	576	500	500	0.9 / 0.8 / 0.8
Price lowest speed grade (900 balls)	\$166	\$210	\$1,032	\$1,496	1.3 / 6.2 / 9.0
Price "our" speed grade (900 balls)	\$191	\$210	\$1,550	\$1,796	1.1 / 8.1 / 9.4
\$\$ per channel for 32+ channels f)	\$5	\$5	\$40	\$45	

a) XC3S5000 is used in present GRETINA digitizers. It is the community's performance yardstick.

b) XC6SLX150 is used in our present 10-channel and 32-channel digitizers.

c) These pin compatible Kintex-7 chips will be used in our forthcoming high density digitizers (40 channels).

d) XC3S5000 provides multipliers without the built-in accumulate register.

e) Total number of block RAM bits divided by 18. Parity bits are considered not useful for waveform storage.

f) Approximate FPGA cost per channel for 32+ channels.

ARM will save board space and enable more channels

In order to upgrade our electronics, we developed the ARM Linux System on Module (SOM) with a low-power, high-performance 1 GHz ARM processor.

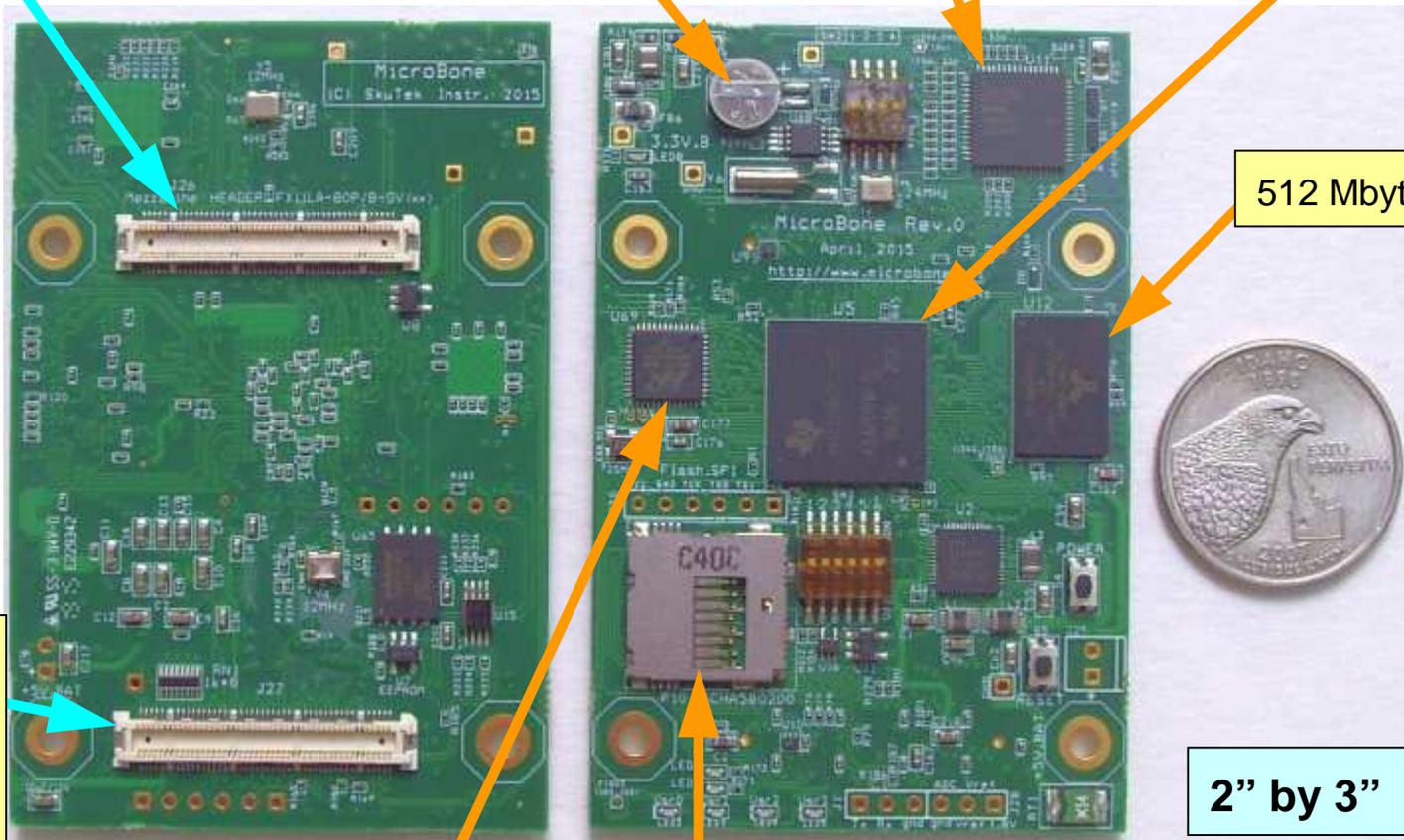
We will use it in our forthcoming electronics. The SOM module itself will also be offered to the community.

80-pin expansion connector A.
Memory interface, USB, video.

Real Time Clock with battery.

Video driver chip.
(Optional.)

1 GHz ARM with two
Programmable Real Time Units



512 Mbytes DDR3

2" by 3"

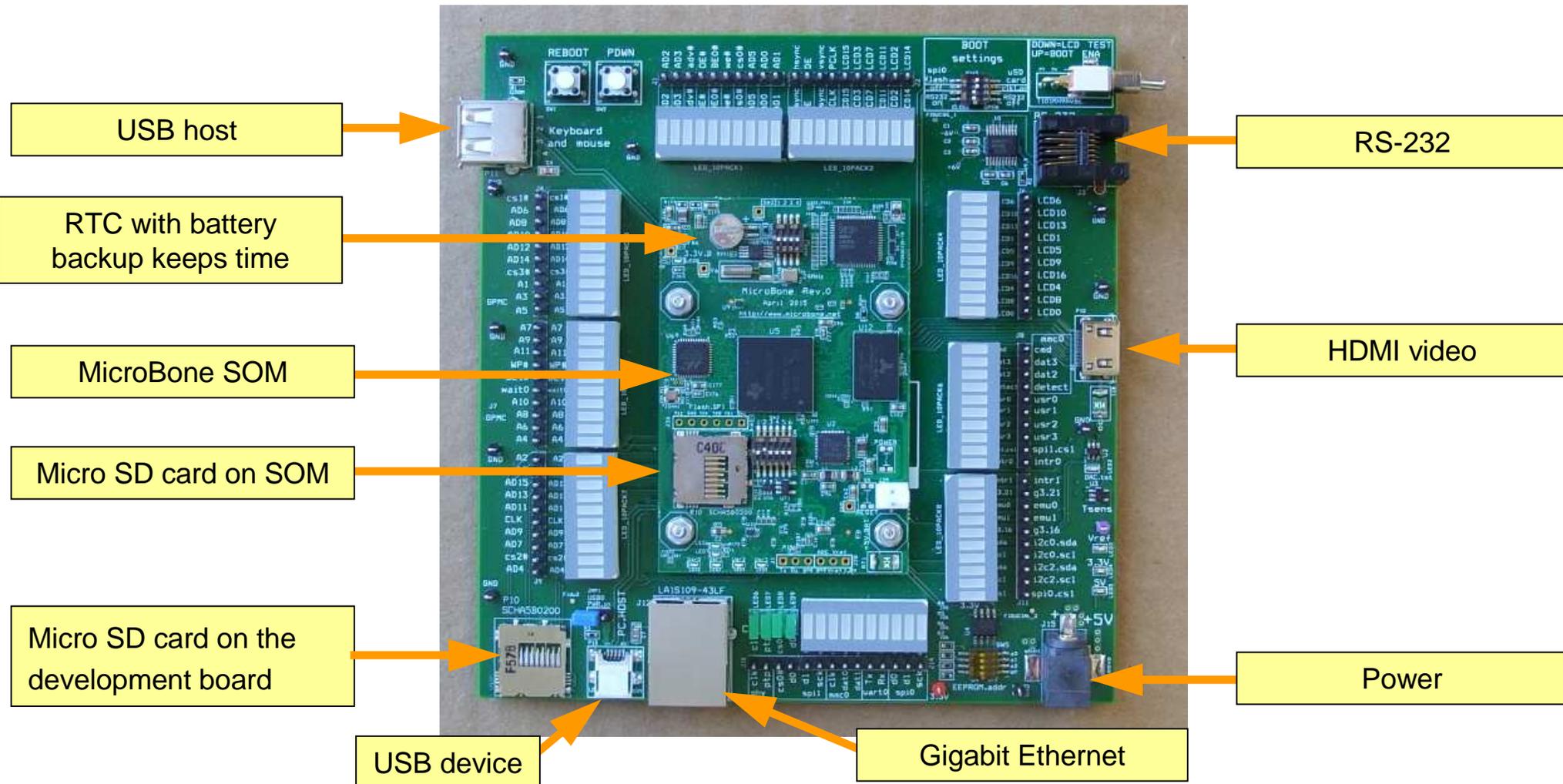
Gigabit PHY

Micro SD card

80-pin expansion B.
Gigabit Ethernet, SPI, I²C.
Includes 8 analog pins:
12-bit ADC/DAC/GPIO

SOM Development Board

- The SOM is hosted by a development board.
- The entire Linux is contained on the MicroSD card. **The entire Linux can be upgraded in 10 seconds.**
- The RTC with battery keeps track of the wall clock. (No need to call NTP...)
- Eight analog pins can be individually configured as 12-bit ADC, 12-bit DAC, or 5V-tolerant logic I/Os.



The Industrial Internet of Things transforms isolated programmable devices into intelligent networks of connected machines. The cloud is a component in these systems, but it is hardly primary. The intelligent software that drives these systems must also reside in the field at the "edge." There is no time, bandwidth or reason to send the data from these devices to a data center. Instead, the compute must come to the devices.

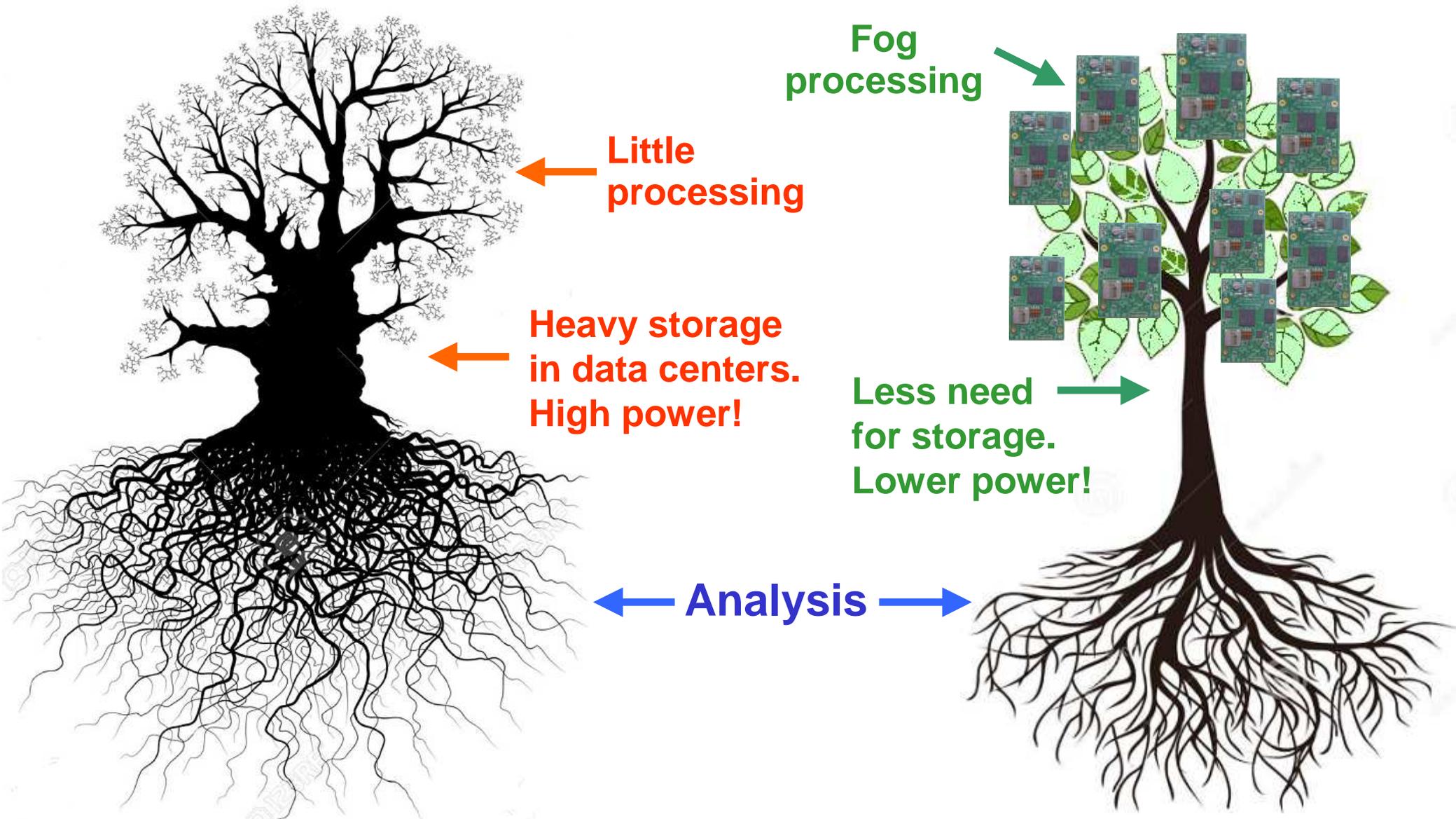
This design is called "fog computing."

Dr. Stan Schneider, CEO, RTI

- Do we have the bandwidth to **always** send **all** the data from the digitizers to a data center?
- Do we have the reason for always doing so?
- Can we rather use computing power inside the DAQ modules?
- Can we find worthy tasks for embedded processing?
 - In-situ histogramming?
 - Waveform preprocessing?
 - Pulse deconvolution?
 - Local trigger calculations?
 - Signal quality monitoring?

Can Fog Computing reduce the need for storage?

Can **this** be replaced with **this**?



Dual channel FemtoDAQ with Silicon Photomultiplier control: an entry-level, low cost, easy to use DAQ.

Instrument: [FemtoDAQ.com](http://www.femtoDAQ.com)

Fog
development?

Example application: CosmicRayNet.net

FemtoDAQ LV-2

2 Channel Digitizer with Detector Bias Supply
Waveform capture, pulse height histograms, event file recording

A small, affordable data acquisition system for physics researchers, educators, and students

Available now!

Buttons: About FemtoDAQ, Description, Status, Near time with SPI, Near time with uPort PMT, VMI Feedback

FemtoDAQ LV-2 is an ideal instrument for researchers, engineers, educators, and students.

FemtoDAQ instruments support particle physics experiments and measurement systems in research, education and industry. The instruments are easy to use with an excellent price / performance ratio.

An illustrative example is presented and discussed on the [Cosmic Ray Net](http://CosmicRayNet.net) website. You will find many details there, such as FemtoDAQ data analysis and techniques of random background reduction. Please have a look!

What can you do with a FemtoDAQ LV-2?

- Deploy the handheld FemtoDAQ anywhere: on a desktop, on a lab bench, or remotely on a network.
- Capture waveforms, generate histograms, and record event files.
- Develop data acquisition and process control software in programming languages such as Python or C.
- Gather slow control data and drive actuators using SPI or PC.
- Use logic signals for triggering.
- Set it up as a standalone DAQ workstation by attaching a mouse, keyboard, and video display to the instrument.

Cosmic Ray Net Cosmos on your desktop

Welcome to Cosmic Ray Net [About ourselves](#) [Contact](#)

Highlights of our recent cosmic ray measurement

On this page we will interpret the results of the analysis described on the [analysis page](#). We will demonstrate two important physical phenomena.

1. Time dilation due to Special Relativity.
2. The Bragg Peak in energy deposition by charged particles.

Is it not amazing that we can demonstrate such important physics with a piece of scintillating plastic, a phototube, and a bunch of electronics?

Cosmic mu-meson decay time distribution proves Special Relativity

Figure C.1. Measured interval distribution between the leading and the trailing pulses after removing the random background. The measured mean lifetime τ is in good agreement with the official value 2.197 microseconds.

FemtoDAQ: Easy to use GUI for everyone

Dual channel FemtoDAQ is easy to operate for first-time users.

Traditional setup screen

FemtoDAQ LV-2 Control Program

Block Flow | Signal Flow | Display Waveforms | Display Histograms | Record Events

Channel A: Front End (NONIN, INVER, Signal Polarity), Internal Test Generator (PULSE, Test Select), Baseline Restore (Baseline % Offset, Test Enable, Baseline Blocking Duration), Discriminator (RISING, FALLIN, Trigger Edge, Trigger Threshold), Triggering (Trigger Enable, Trigger Averaging), Waveform (Source, NORM, RAW, TRD), Histogram (Histogram Scaling, Signal Averaging), Time Settings (Channels A, B, Trigger X Position, Pileup Detection Duration, Pulse Energy Measurement Duration), Coincidence (Channels A, B, OR, AND, Global Coincidence Duration), Detector Bias (Voltage Range, Voltage Setting, Voltage Setting).

Channel B: Front End (NONIN, INVER, Signal Polarity), Internal Test Generator (PULSE, Test Select), Baseline Restore (Baseline % Offset, Test Enable, Baseline Blocking Duration), Discriminator (RISING, FALLIN, Trigger Edge, Trigger Threshold), Triggering (Trigger Enable, Trigger Averaging, External Trigger Enable), Waveform (Source, NORM, RAW, TRD), Histogram (Histogram Scaling, Signal Averaging), Time Settings (Channels A, B, Trigger X Position, Pileup Detection Duration, Pulse Energy Measurement Duration), Coincidence (Channels A, B, OR, AND, Global Coincidence Duration), Detector Bias (Voltage Range, Voltage Setting, Voltage Setting).

TO START: Connect to the instrument using the FemtoDAQ menu Units: ADC

Data flow setup screen

FemtoDAQ LV-2 Control Program

Block Flow | Signal Flow | Display Waveforms | Display Histograms | Record Events

Channel 0: IN A, ADC, Baseline % Offset, Signal Polarity, Baseline Blocking, Channel Trigger, Trigger Averaging, Trigger Threshold, Trigger Edge, Signal Averaging, Histogram Scaling, Pileup Detection Duration, Pulse Energy Measurement Duration.

Channel 1: IN B, ADC, Baseline % Offset, Signal Polarity, Baseline Blocking, Channel Trigger, Trigger Averaging, Trigger Threshold, Trigger Edge, Signal Averaging, Histogram Scaling, Pileup Detection Duration, Pulse Energy Measurement Duration.

TO START: Connect to the instrument using the FemtoDAQ menu Units: ADC

Waveform display

FemtoDAQ LV-2 Control Program

Settings | Measurement

WAVEFORM - FemtoDAQ LV-2

Ch0

TRIGGER STATUS	STATUS	ADC	Mult Trig Cnt	Baseline Avg	Integ Pulse Hgt	Plot Max/Min	Waveform Mean	Normalized RMS
START CAPTURE	CH 0	OK	---	---	---	-7464	-7737	65.859
STOP CAPTURE	CH 1	OK	---	---	---	---	---	---

Data Written to file D:\Program Files\FemtoDAQ LV-2\Waveform0.bt Units: ADC

Histogram display

FemtoDAQ LV-2 Control Program

Settings | Measurement

HISTOGRAM - FemtoDAQ LV-2

Ch0

TRIGGER STATUS	STATUS	ADC	Mult Trig Cnt	Baseline Avg	Integ Pulse Hgt	Plot Max/Min	Waveform Mean	Normalized RMS
START CAPTURE	CH 0	OK	---	---	---	4014	---	---
STOP CAPTURE	CH 1	OK	---	---	---	---	---	---

Histogram Capture Plot Complete Units: ADC

Schedule

- Standalone table top DAQ units with ARM running Debian Linux.
 - **FemtoDAQ: 2 channels, 14 bits @ 100 MSPS, Spartan-6: AVAILABLE NOW.**
 - We are working with our customers on improving its features.
 - **DDC-10 100 MHz: 10 channels, 14 bits @ 100 MSPS, Spartan-6: SENT TO PRODUCTION.**
 - **DDC-10 250 MHz: 10 channels, 14 bits @ 250 MSPS, Spartan-6: next in line.**
- VME DAQ modules with Kintex and optional ARM running Debian Linux: **under development.**
 - **High density 100 MHz: 32+ channels, 14 bits @ 100 MSPS, Kintex-7.**
 - **Logic Unit** for triggering and data streaming, Kintex-7.
- ARM SOM will be offered to customers.
 - ARM SOM can be embedded in third party instruments.
 - Can be used for standalone control applications (it has the 12-bit ADC/DAC).



Future plans

"Prediction is very difficult, especially if it's about the future." -- Niels Bohr

We plan the following:

- Complete the high density digitizer with 32+ channels per unit.
- Complete the 250 MHz versions of our low density modules (2 and 10 channels).
- Develop the ARM SOM into a full featured product of its own.
 - Establish and nurture the SOM user community.
- Keep improving the features of our instruments according to the feedback from customers.
- Add more kinds of modules to our product line.
- Our plans depend on the reception of our work by the community.

Questions for the NP community

- What difficulties do you have with your current DAQ systems?
- What features should a DAQ system provide to best support your experiments?

Acknowledgements:

David Hunter, Joanna Klima, Gregory Kick, William Noonan

Eryk Druszkiewicz, Dev Khaitan, Jun Yin, Frank Wolfs



Backup slides

Improved CPU performance in numbers

- ARM has superior performance thanks to integration of many peripherals on chip.
- ARM will provide 4x more RAM with 3x higher nominal performance.
- NEON vector floating point unit and the Mobile GPU which can be used for event processing.
- Programmable Real Time Units (PRU) can be used for software trigger with deterministic latency.
- ARM will run mainstream Linux (Debian, Ubuntu, etc.) with up to date security features.

Feature	BF561 (present)	ARM AM335x (new products)	Improvement?
# cores	two	three (1 ARM + 2 PRU)	yes
Speed	2*600 MHz	1 GHz + 2*200 MHz	~same
Off-chip RAM memory	128 MB	512 MB	4x more
Type of RAM memory	SDRAM	DDR3	
Memory bus	133 MHz * 32 bits	400 MHz * 16 bits * 2 (DDR)	3x more
Separate SDRAM / SRAM buses	no	yes	yes
Floating point	no	yes	yes
USB-2 on chip	no	yes	yes
Gigabit MAC on chip	no	yes	yes
Graphics unit on chip (GPU)	no	yes	yes
Resident GUI	no	yes	yes
Linux version running on-board	uClinux	full Linux (Debian, Ubuntu, ...)	yes
Linux community projects	few	many	yes