



**Ridgetop Group Inc**  
ENGINEERING INNOVATION

# DOE ADC Designs Program Review August 2014

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Contract No.: DE-SC0006340

Contractor Name: Ridgetop Group, Inc.

Contractor Address: 3580 West Ina Road, Tucson, AZ 85741

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# Ridgetop Group, Inc.

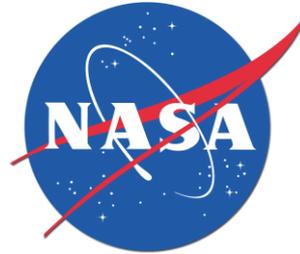


- Arizona-based firm, founded in 2000, with focus on electronics for critical applications
- Two divisions: Semiconductor & Precision Instruments (SPI) and Advanced Diagnostics & Prognostics (ADP)
- Technology leader in precision mixed signal IC design for harsh environments
- Expertise in mitigation of radiation effects
- Complete Cadence-based IC design tool set

- Extensive instrumentation design experience
- Foundation in physics-of-failure for reliable electronic systems



# Partners and Customers



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# Award-Winning Design Recognition



Raytheon Small Business Partner Award



Japanese IP Innovation Award

# Ridgetop Accreditations



ISO9001:2008 Quality Management System

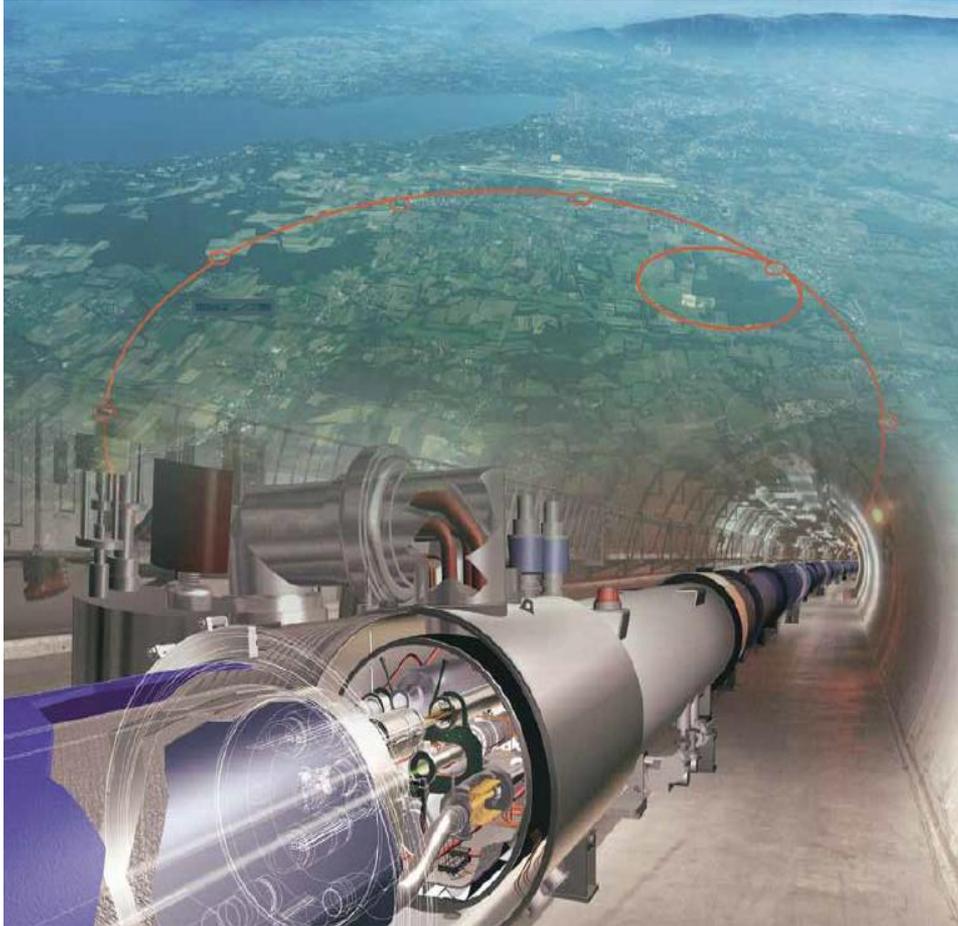


AS9100C Quality Management System



Microelectronics Trusted Supplier (Defense Microelectronics Agency)

# Primary application



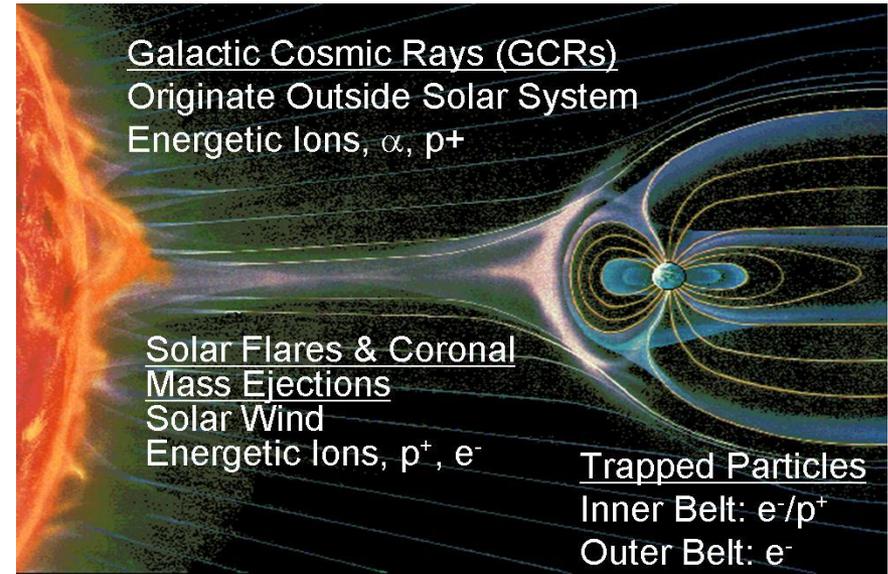
**Radiation-Hardened ADC  
for Particle Accelerator  
Instrumentation clusters**

**Strong interest from CAEN**

**Two ADC orders from ON  
Semiconductor for ADC design**

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# Secondary Application



**Trapped protons cause most of the degradation effects TID/oxide damage, displacement damage and resulting SEEs from heavy ion strikes)**



# Radiation Mitigation Methods

## Rad-Hard by Design

**Rad Hard Libraries**

**ProChek for  
validation**

**Adaptive Biasing for  
analog circuits**

**TMR and DICE  
latches for digital  
circuitry**

## Rad-Hard by Shielding

**RadChek™ Radiation  
Shielding Tool**

**Use iteratively to  
reduce impact of  
space radiation**

**Special  
consideration for  
neutron fluence  
analysis**

## Rad-Hard by Process

**Utilize Silicon on  
Insulator (SOI)  
process to avoid  
latchup issues**

**Smaller geometry  
devices have  
reduced TID issues**

00402d



# SBIR Program Objectives

## ADC 3 GSPS 12 bit (Topic 44g)

R&D Program started 8/8/12 and Ends 8/8/14

Programmable, Time-Interleaved double sampled pipeline, high speed (500 MS/s – 3 GS/s), high resolution (12-14 bits) analog-to-digital data converter (ADC), highly linear with an INL and DNL of no more than  $\pm 0.5$  LSB, an operating temperature range of at least -10 to 80 °C, a very high effective number of bits (ENOB) of 11.0, and a total ionization dose (TID) rating of 1 Mrad.

## ADC 40 MSPS 12 bit (Topic 61a)

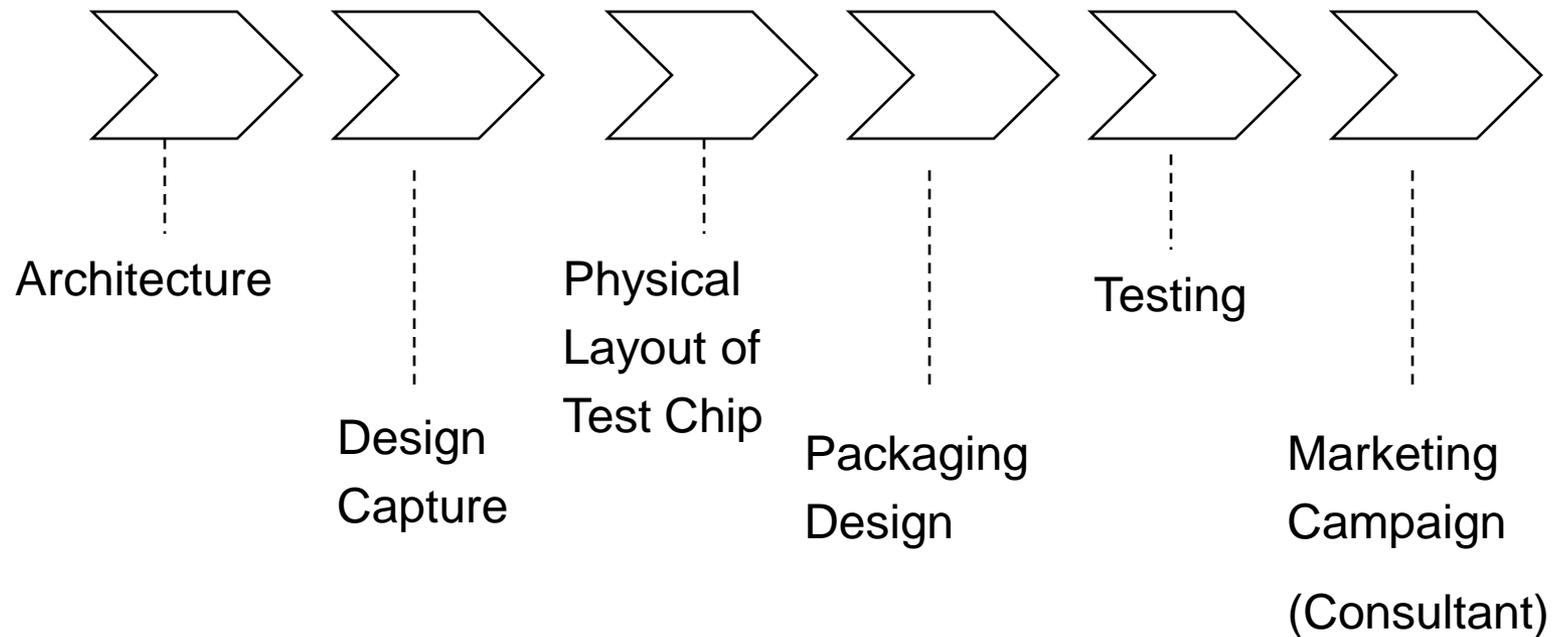
R&D Program started 8/8/12 and Ends 8/8/14

Programmable, low-power pipeline (<100 mW), high performance (40 MS/s), high resolution (12 bits) analog-to-digital converter (ADC), highly linear with an INL and DNL of no more than  $\pm 0.5$  LSB, an operating temperature range of at least -10 to 80 °C, a very high effective number of bits (ENOB) of 10.0, and a total ionization dose (TID) rating of 1 Mrad.

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# IC Design Flow



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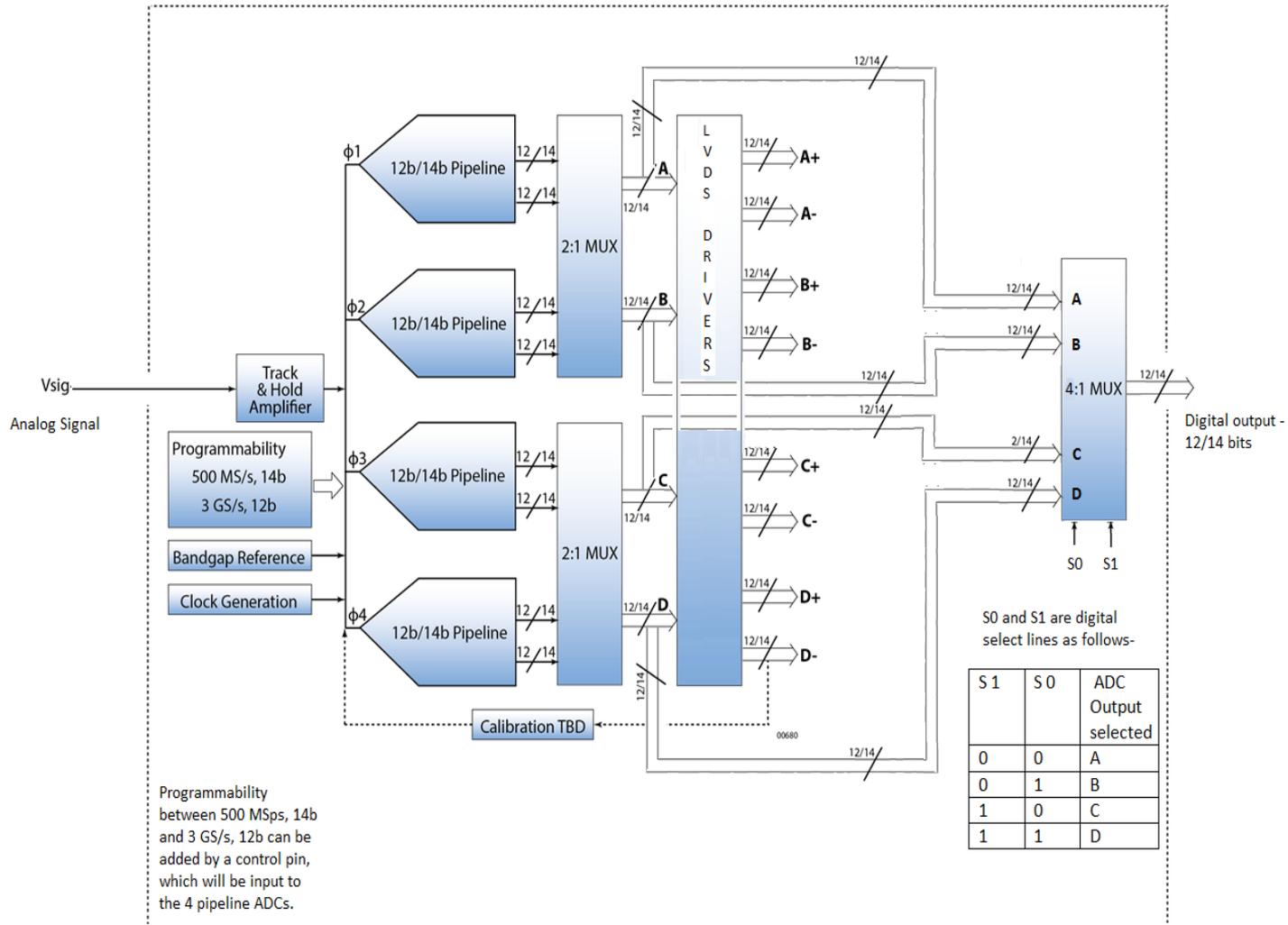
# ADC Pipeline 3 GSPS

- Programmable ADC
- Time-Interleaved double sampled pipeline, high speed (500 MS/s – 3 GS/s)
- High resolution (12-14 bits)
- Highly linear with an INL and DNL of no more than  $\pm 0.5$  LSB,
- Operating temperature range of at least -10 to 80 °C,
- Total ionization dose (TID) rating of 1 Mrad.

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# ADC Architecture 3 GSPS



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# 3 GSPS ADC Targeted Specifications

Specification	Original Goal	Current Estimate
Resolution [bits]	12	12
Sampling speed [GS/s]	0.5 - 3.0	0.5 - 3.0
Input analog bandwidth [GHz]	2.0	12
Power [W]	1.0	2.5
SFDR [dB]	74	72.7
ENOB at 250MHz input [bits]	11.0	11.0
ENOB at 1.5GHz input [bits]	11.0	8.5
TID hardness [krad]	1000	>1000
SEL hardness [Mev-cm <sup>2</sup> /mg]	120	120
Process	IBM 130 nm SiGe	IBM 130 nm SiGe
Operating Temperature	-40 to +85 °C	-40 to +85 °C

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# Centering the ADC Design

- **Small-geometry fabrication processes are very complex and have many reliability concerns for demanding applications:**
  - **Bias Temperature Instabilities (NBTI and PBTI)**
    - Including hard-to-detect annealing effects
  - **Dielectric Breakdown**
  - **Hot Carrier Effects**
  - **Radiation**
  - **Combined effects (e.g., radiation and NBTI)**
  - **Electromigration**
  - **Stress Migration**
  - **Process Mismatch Effects**
  - **Lot-to-lot Variation**
  - **Etc.**

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# Remaining 3 GSPS ADC Challenges

- Design is largely complete and verified using IBM Process Design Kit (PDK) and recommended Cadence simulator
- Ridgetop requests bridge funding for high density packaging that is required at RF frequencies (flip chip) and radiation testing. There is a tradeoff of dynamic range and radiation hardness involved.
- There is confirmation of demand from key players such as CAEN, Boeing and ON Semiconductor

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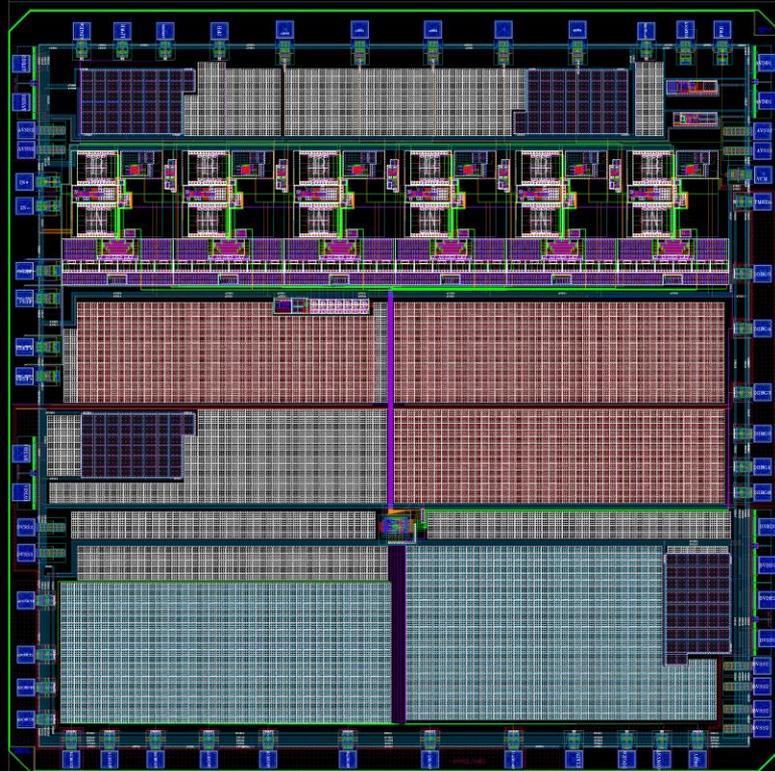
# 40 MSPS - ADC Specifications

Spec	Original Goal	Simulated
Resolution [bits]	12	12
Sampling speed [MS/s]	40	40
Power [mW]	<100.0	22.5
SFDR [dB]	74	72
ENOB input [bits]	11	10
TID hardness [krad]	1000	>1000
SEL hardness [Mev-cm <sup>2</sup> /mg]	120	120
Process	IBM 130 nm SiGe	IBM 130 nm SiGe
Operating Temperature	-40 to +85 °C	-40 to +85 °C

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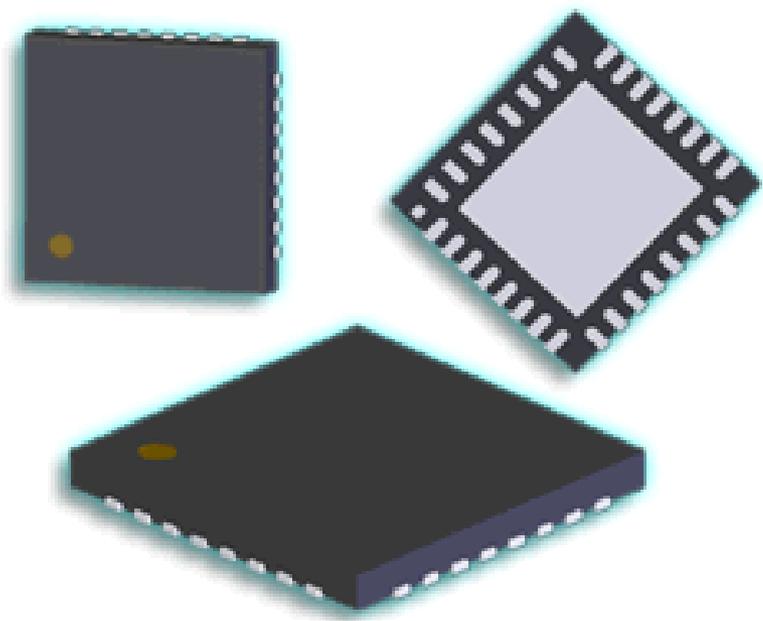
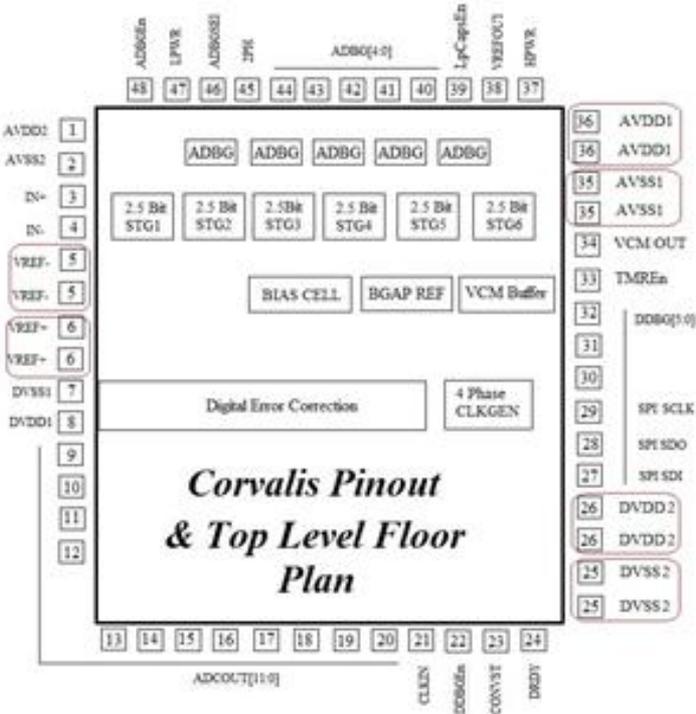


# 40 MSPS ADC Layout



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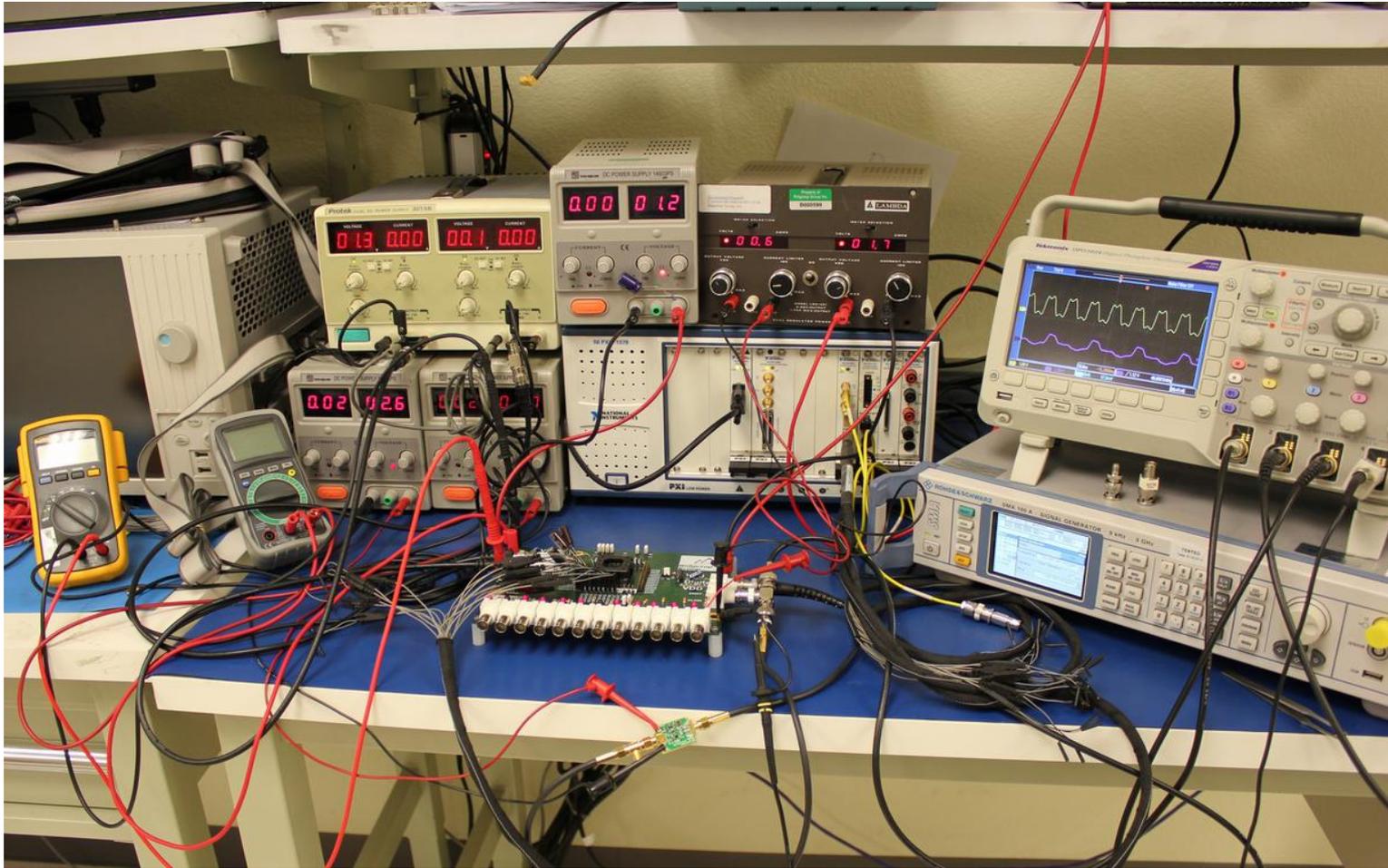
# 40 MSPS - Packaging



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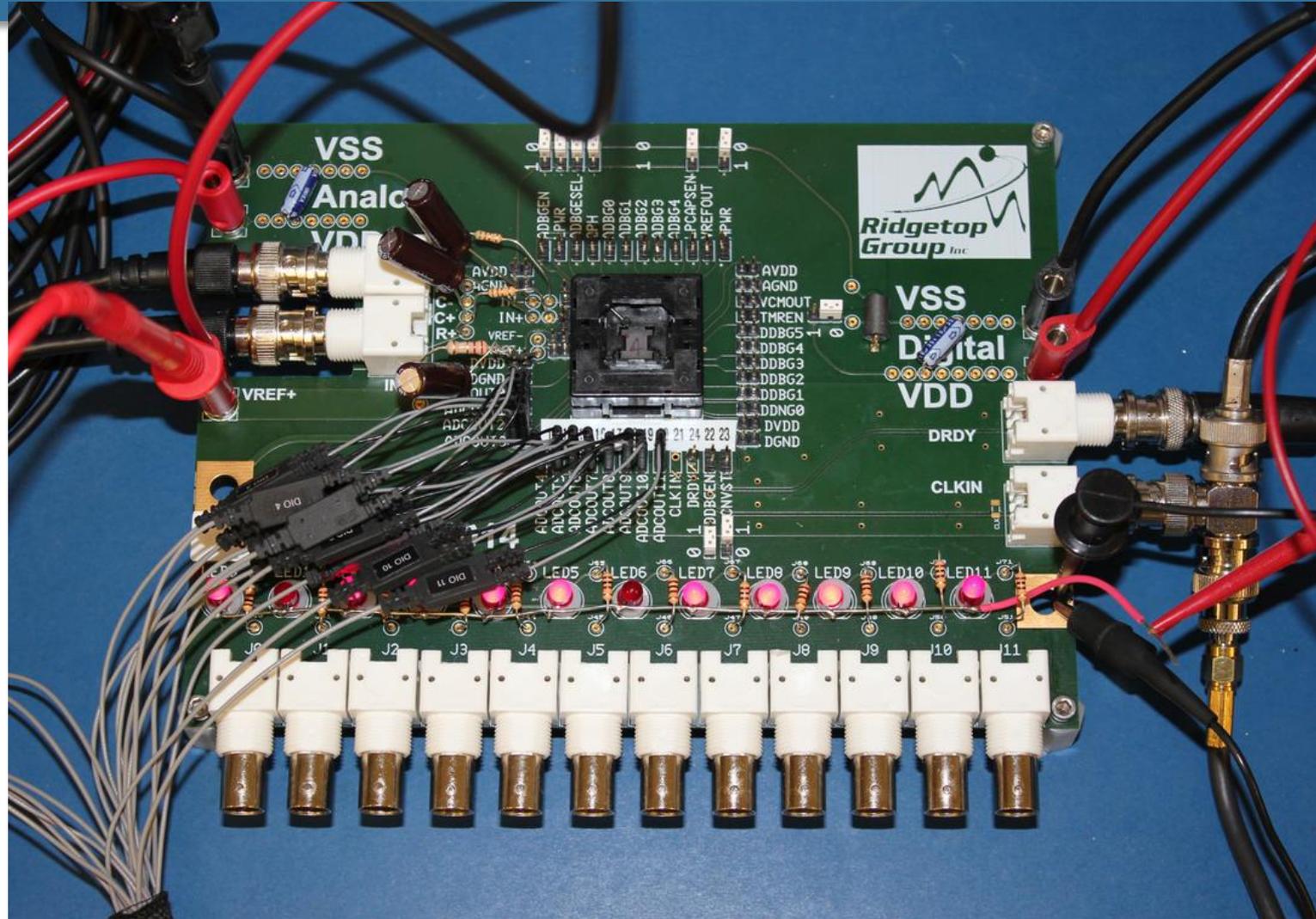


# Evaluation Test Bed – 40 MSPS ADC



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# Test Board – 40 MSPS ADC



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# Commercialization with CAEN

- CAEN is a leading supplier of precision instruments for particle accelerators.
- Strong interest from CAEN in using Rad Hard ADC from this SBIR program
- Possible collaboration on other products as well.



Dear Doug,

thank you once more for your visit in CAEN !

As promised, I'm sending you in attachment the data sheet of the commercial ADC that we have installed in our fastest digitizers, respectively:

V1751 "4/8 Channel 10 bit 2/1 GS/s Digitizer"

and

V1761 "2 Channel 10 bit 4GS/s Digitizer"

As you remember, these digitizers are available also in the desktop and NIM form factors.

Coming to the radiation levels present in LHC and SuperLHC experiments at CERN, just to have an idea about the environment which your ADC can find, I can confirm you the values expected for LHC in the so called balconies, i.e. at some meters of distance from the beam.

They are:

1\*10E11 proton/cm2

2\*10E12 neutron/cm2

15 kRad TID

But this is already history, in fact the SuperLHC experiments will face higher values, both for the increased luminosity, and for the fact that digitizing electronics will be probably located closer to the beam, with respect to the balconies.

If you have more questions or comments, please feel free to ask !

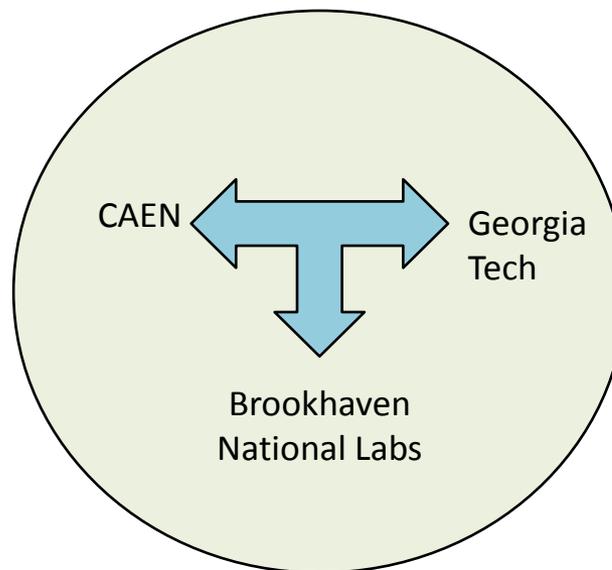
Best Regards

Claudio

# Development Ecosystem

- Ridgetop Group, Inc.  
Sampath Venkatesan,  
Principal Investigator
- Domain Expertise: Dr. Chen,  
Brookhaven National Labs
- System Integration Expertise :  
CAEN –Claudio Raffo
- SiGe Semiconductor  
Expertise – Dr John Cressler  
at Georgia Tech

Ridgetop Group, Inc.  
SBIR Recipient



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# ADC– Additional Applications

## Terrestrial Communication Systems

Provides the high-speed ADC required within high performance transceiver hardware.



Software Defined Radio Applications



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# ADCs – Path forward

- Exceptionally challenging design that can revolutionize measurements in presence of radiation.
- Continue to use SiGe technology with assistance from Georgia Tech
- Develop commercialization paths with CAEN and Boeing, and ON Semiconductor.
- Have received strong interest in extending our work.
- Bridge funding for packaging and refinement are needed

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# Summary

- Significant progress in providing rad hard ADCs to support DOE and CERN Programs
- Additional funding sought for finalization, packaging and radiation testing.
- Strong commercial market “pull” for performance point of both ADCs

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# Contact Information



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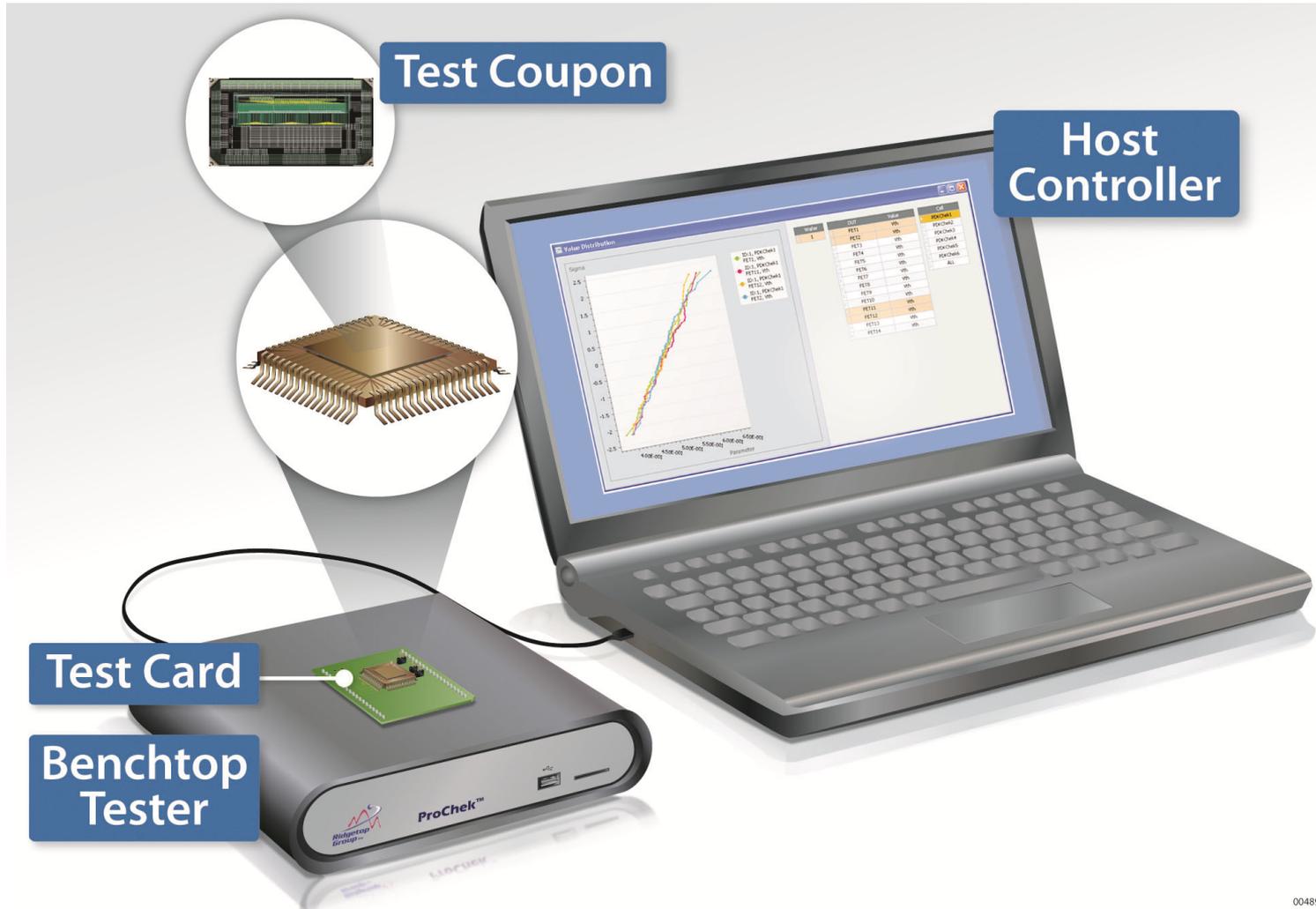


# Additional Rad Hard Tools

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# ProChek Semiconductor Characterization Platform



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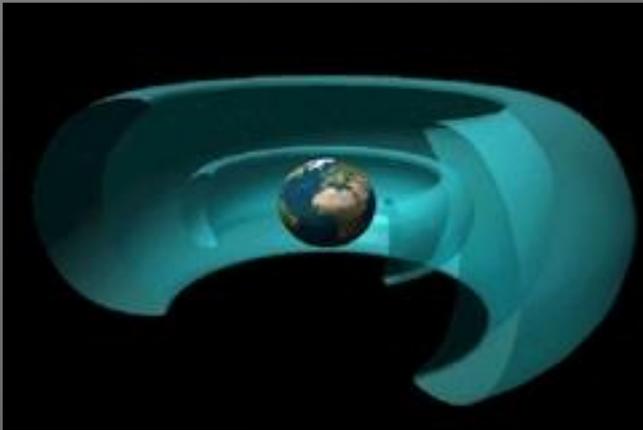
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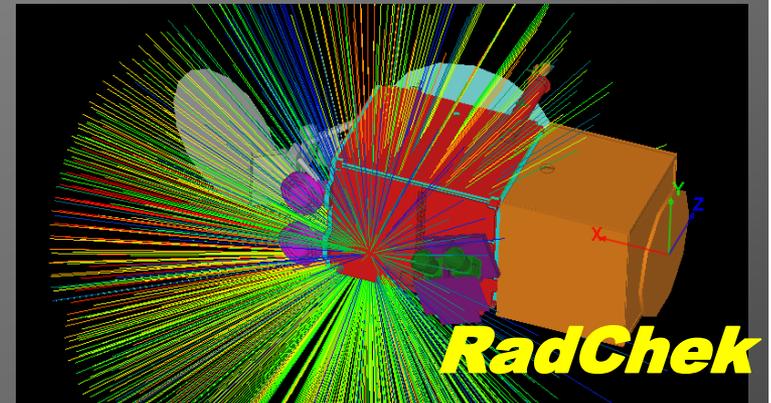
# RadChek™ Radiation Shielding Tool

- Estimate and Analyze the dose reaching the sensitive components...

Environment Modeling



Transport through satellite structure & shielding



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