SBIR Topic: DOE 2009 – 44d
CMOS Foundry for Monolithic Particle Detectors

DOE-NP SBIR/STTR Exchange Meeting November 2013

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Voxtel Inc.

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Outline

- Brief Introduction to Voxtel
- Overview of Problem/Opportunity:
  (a) Si Detector CMOS Process, (b) Starting Materials, and (c) FEOL and BEOL Processes
- Discussion of Solution:
  "Through-BOX-Via" (TBV) Detectors at Sandia National Labs (SNL)
- Silicon detector array developments at Voxtel

  As potential candidates for SNL TBV processed silicon pixelated array detectors (PADs)
- Summary and Discussion

"Detector funding in Europe is good; in Japan, modest; but in the US, totally inadequate."

Chris Damerell of Rutherford Appleton Laboratory and chair of the Detector Panel, warned at SNOWMASS

About Voxtel

VOXTELOPTO

Corporate Offices / Voxtel Opto (Beaverton, Oregon)

- Contract Administration
- Opto Products Group
  - InGaAs and silicon photodiodes, avalanche photodiodes (APDs), photoreceivers, and focal plane arrays
  - Readout integrated circuits (ROICs) for imaging, LADAR, and radiation detection
  - Single-photon-sensitive detectors and instruments
  - Electro-Optic systems engineering

Voxtel Nano (Eugene, Oregon)

- Nano Products Group
  - Colloidal semiconductor quantum dots (PbS, CdSe, InP, SnTe, etc.)
  - Rare-earth-doped nanocrystals (ZnS, YVO_4, LaF_3, etc.)
  - Ligand design and custom surface functionalization
  - Optical up- and down-conversion
  - Security inks and covert taggants
  - Nanocrystal-sensitized photovoltaic and photoconductive devices
  - Continuous flow reactors for nanocrystal/quantum dot synthesis
- Analytical Facilities

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VoxtelOpto's Product Focus

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Laser Rangefinders and Photoreceivers

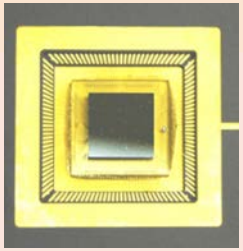
Laser Rangefinders

Low noise MHz-GHz SWIR receivers

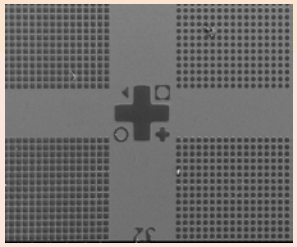
Avalanche Photodiodes and Detector Arrays

High Gain, Low Noise APDs

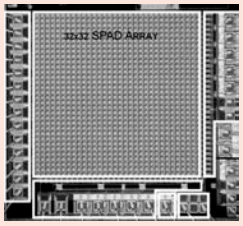
InGaAs photodiode and APD arrays



SWIR/MWIR HgCdTe APDs



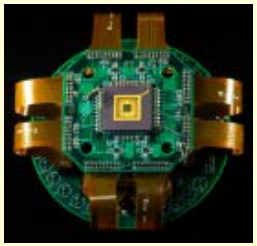
Back-illuminated Mesa III-V Arrays



SiPM / SPAD Arrays

Parallel Segmented Pixels

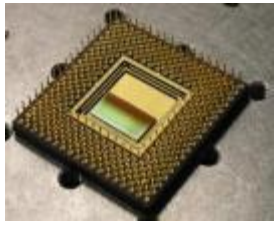
Event-driven Sampling & Waveform Flash LADAR



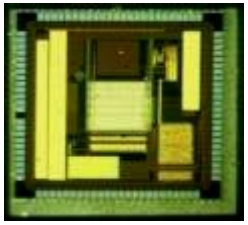
Time & Pulse Sampled and Waveform LADAR Receivers

< 30 ps, 1024 channel time-to-digital converter with TOT

Photon Counting & Event Driven Asynchronous ROICS and FPAs

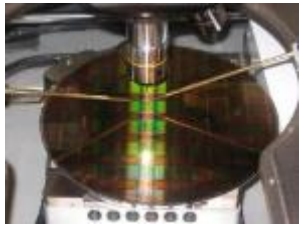


Sparsified, event driven amplitude or arrival time of photons



Asynchronous Event-driven Counting/ Timestamping

Active/Passive FPAs



3D ROICs with sparse and event driven readout

MWIR/SWIR Active Passive Imager

The Problem Facing Si Pixelated Detector Array Designers

Si Detector Requirements

1. *Analog/ Mixed signal*
2. *High resistivity (4 kΩ/cm)*
3. *Thick electrically/optically active layer*
4. *High biases (5 VDC → 50+ VDC)*
5. *Thick, thermal oxides with ultra-low leakage*
6. *Large, high linearity capacitors*
7. *Full wafer integration*
8. *Custom materials, process flows and implants*
9. *< 5" wafers available from R&D & MEMS fabs*
10. *Need trained domestic work force*

Commercial Sub-µm CMOS Properties

1. *Digital (high leakage currents)*
2. *Low resistivity (heavy doping) (5 Ω/cm)*
3. *Thin electrically active layer (thin depletion)*
4. *Low voltage (0.9 VDC ←1.8 VDC)*
5. *Thin high k+ oxides*
6. *Standard process flows*
7. *Full reticle integration (22 x 22 mm^2)*
8. *Mask costs > $2M*
9. *No variability in materials or process*
10. *200 mm + wafers - only*
11. *Trained mostly foreign work force*

Today's CMOS processes are increasingly antithetical to high performance detector processing, and as they diverge, there is no stable high-volume manufacturing capability for silicon scientific detectors

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FEOL and BEOL Solutions Available for Detector Developers

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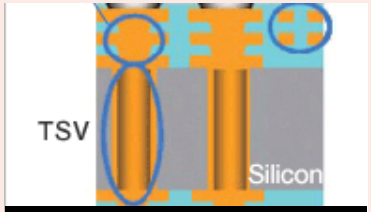
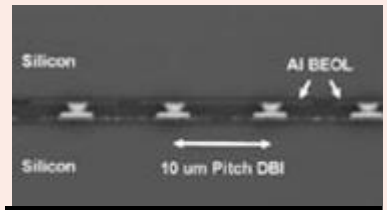
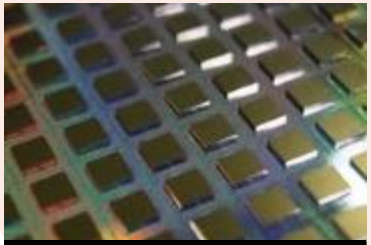
(1) BEOL: Via-less and TSV 3D Wafer Stacking

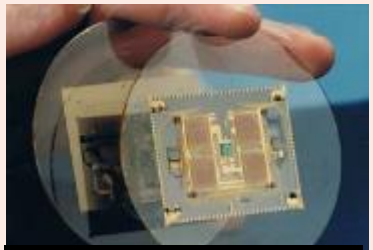


Through Silicon Via (TSV)

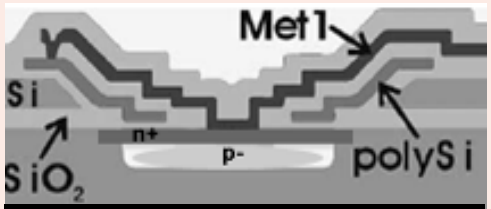


Vialess Stack

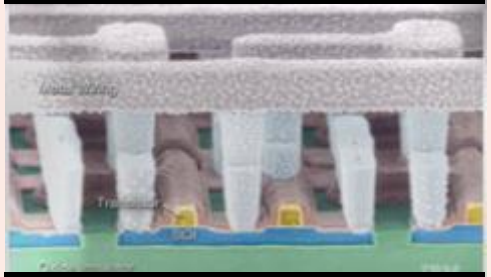

Die to Wafer Bond


Wafer to Wafer Bond

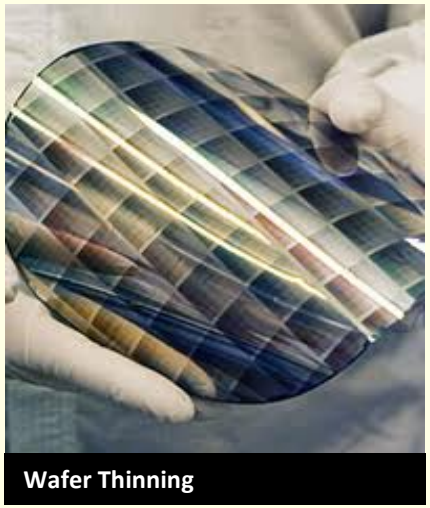
(2) FEOL: Through BOX SOI Wafers



SIT Through Vias


SOT

BEOL: Wafer Thinning


Wafer Thinning

- **Back-end of Line (BEOL) processes largely inaccessible to detector developers**
  - developed on 200+ mm wafer tooling
    - 200 mm fabs not widely available for detector development
  - requires full wafers (no multi-project chips)
    - 0.18 um reticle costs and first lot run is about $480K (nanoscale 40 nm is $3M)
  - twice the cost when two wafers are being used (wafer to wafer bonding)
- **However, currently there are no ready sources of monolithic SOI CMOS TBVs**

BEOL:

Face-to-Face (F2F) 3D Detector Integration

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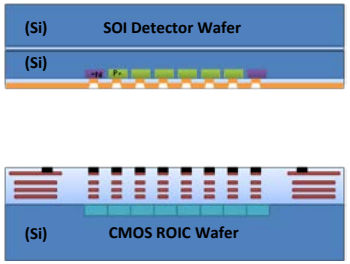
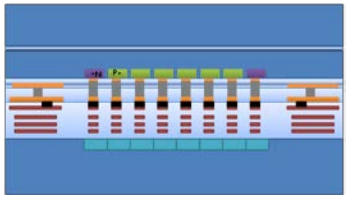
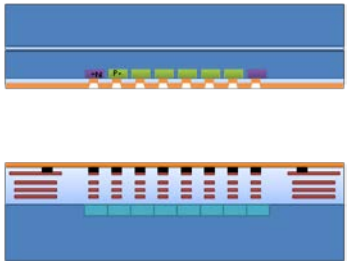


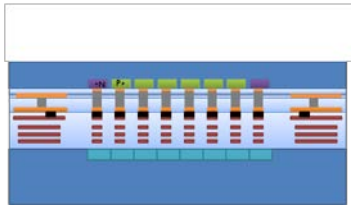
Starting Materials: SOI detector wafer has global Al deposition; CMOS ROIC wafer is planar with last VIA up to surface.



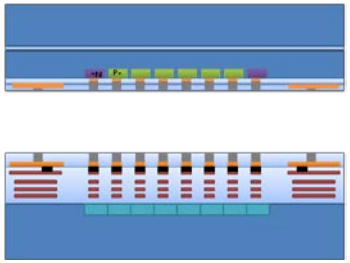
Step 5: Bond SOI detector and ROIC wafers at room temperature following preparation with NH_4OH solution.



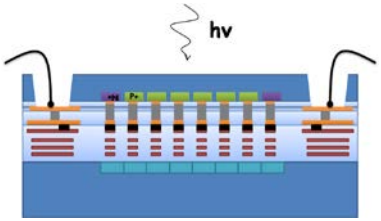
Step 1: CMOS ROIC wafer receives a global seed metal (Al) deposition. SOI detector wafer already has global seed metal.



Steps 6-7: Grind away silicon handle wafer of SOI within 50-µm of BOX. Remove remaining Si handle and BOX using wet etch process.

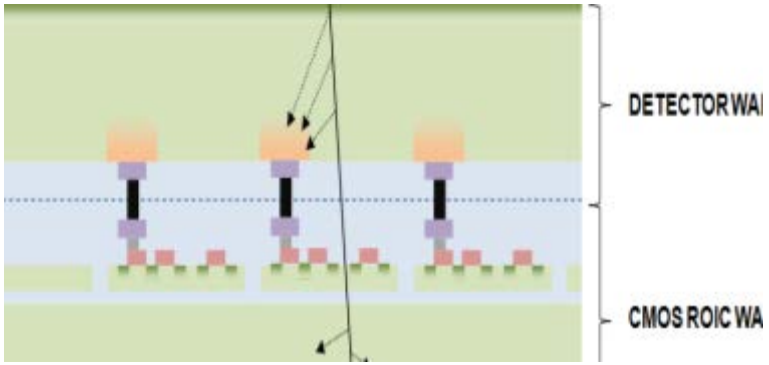


Steps 2-4: Both wafers pattern/plate DBI metal (Ni), etch seed metal, and receive oxide deposition/planarization.

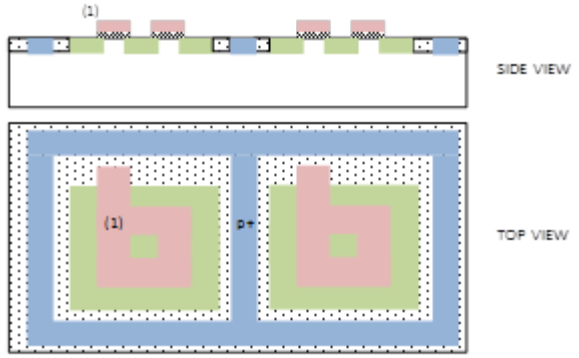


Steps 8-9: Remove Si material above CMOS ROIC bond pads. Open SiO_2 passivation above ROIC pads. Package device.

Wafer-to-wafer processing and bonding flow for SOI detector array



- **Standard SOI CMOS bottom ROIC wafer; upper detector wafer is high-resistivity silicon substrate**
- **two wafers are bonded using direct-oxide bond technology, allowing <10-µm pitch.**



Enclosed-layout transistor (ELT) device. All leakage paths are removed using the enclosed layout with p+ guard rings.

BEOL:

F2F Wafer Bonding and Back-thinning of SOI Wafer

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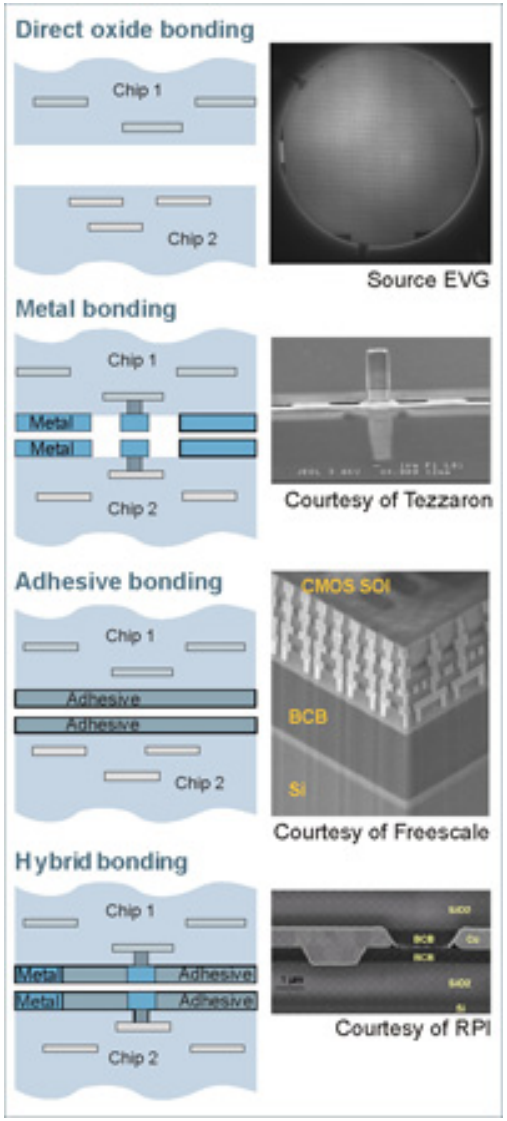
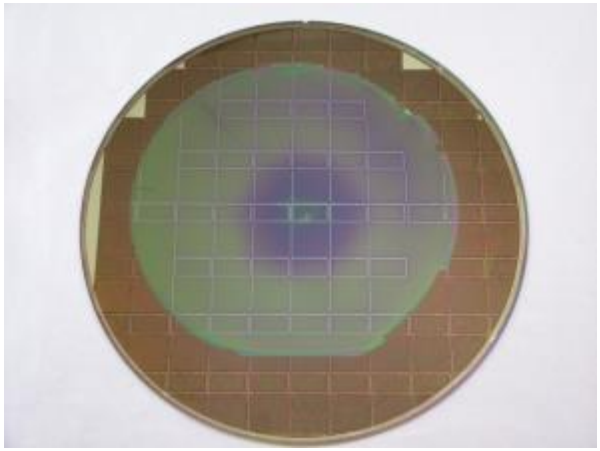
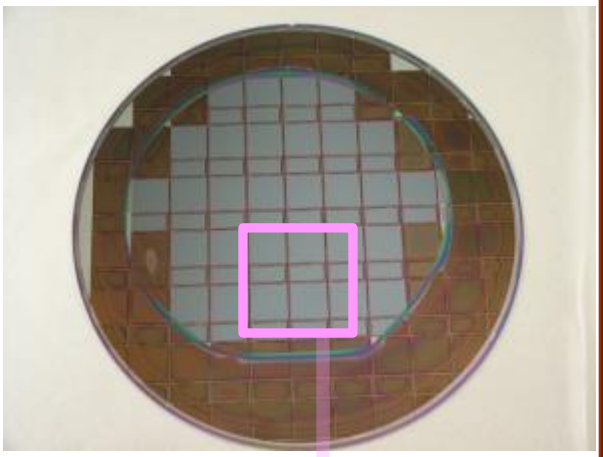


3D Bonding and Back-thinning of wafers



Bonded Voxtel VX-802 ROIC wafer bonded to detector before thinning

- 200-mm ROIC wafer bonded to 150-mm detector wafer
- Detector layer 20 um thick

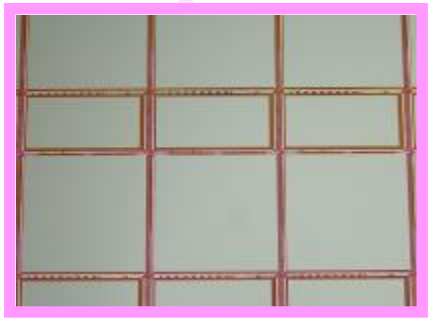


Wafers after bonding and thinning

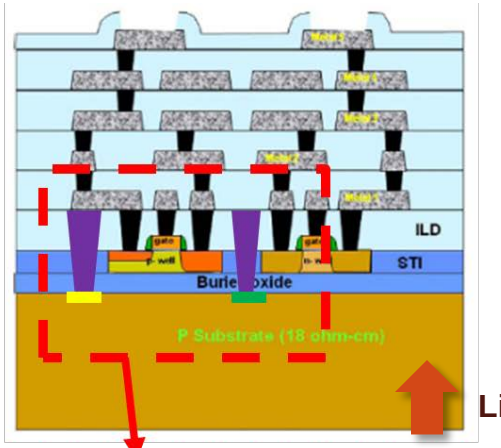
- detector mesas formed and bond pad openings etched

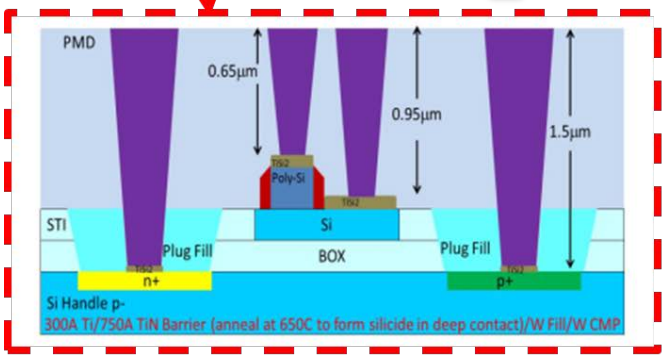
Zoom of device (large square) in wafer form.

- gray areas are the mesas with a 20 µm thick detector
- small pads in the brown areas are the bond pads for the sensor.

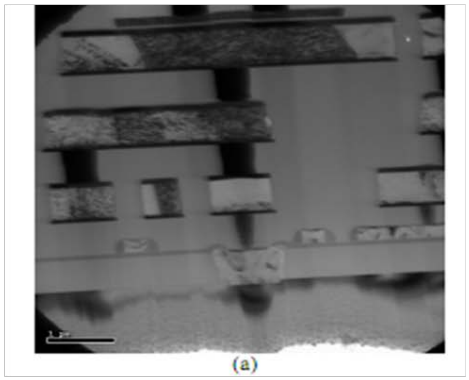


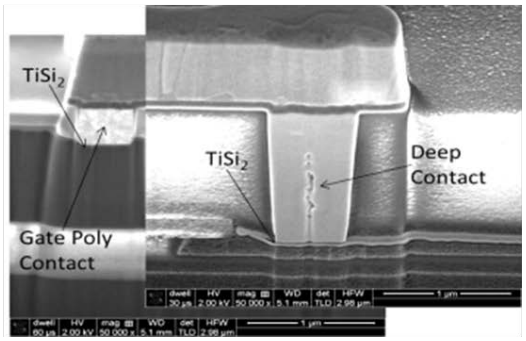
FEOL Through Via Process Implemented on Sandia CMOS7 SOI CMOS





Trench Silicided Deep Contact Option





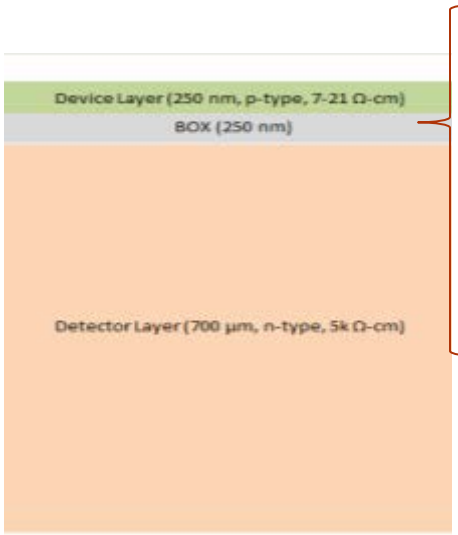
FIB cross sections of deep contacts

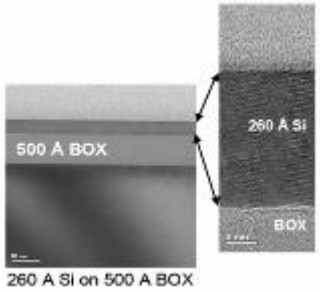
Sandia's CMOS7 technology:

- ***SOI (Silicon-on-Insulator) CMOS process***
- ***24 mask level process with 5 metal layers***
- ***strategically radiation-hardened,***
- ***3.3-volt,***
- ***0.35-micrometer,***
- ***high reliability digital, analog and mixed-signal ASICs.***

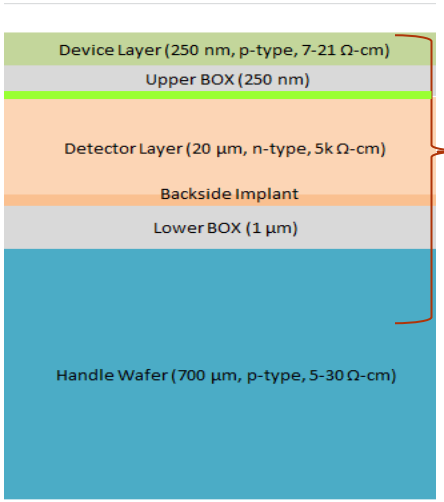
- **Due to trench isolation SOI is inherently rad tolerant and less susceptible to SEU**
- **Voxtel developed, under SBIR funding:**
  - processes for forming electrical through BOX via to SOI substrate
  - double SOI wafer design and specification
  - photodiode architecture

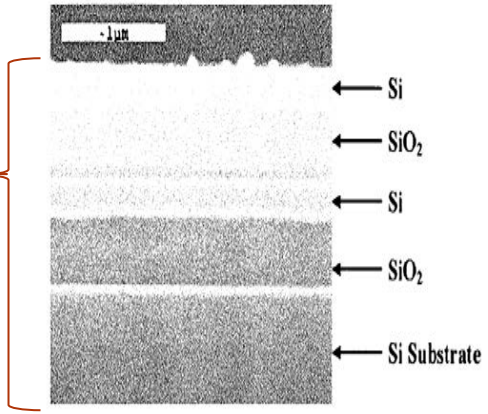
Starting SOI Wafer Substrates





SEM Cross section of a SOI wafer.





SEM of double SOI layer

Cross-section of common single BOX SOI wafer

Cross-section of double BOX SOI wafer used for back-thinning

- **Double SOI Substrates Engineered for High Performance Detectors**
  - Low resistivity transistor layer
  - High resistivity detector layer
  - Passivating implants integrated into wafer layers during construction
  - Lowest BOX layer used to promote thinning
  - Topmost BOX has detector vias
- **Engineered double SOI wafers inserted into CMOS process at beginning, with only minimal changes to CMOS process required**

Through BOX Via Process Implemented in Sandia CMOS7 process

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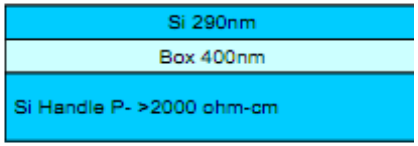
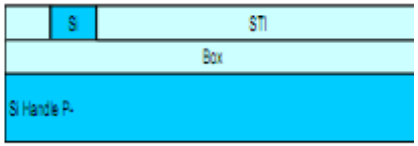
1) Start material 250nm 1-0-0 p-type silicon on 400nm BOX SOI (silicon on insulator) with 625um handle wafer FZ (Float Zone) with greater than 2000 ohm-cm resistivity (SOITEC material)

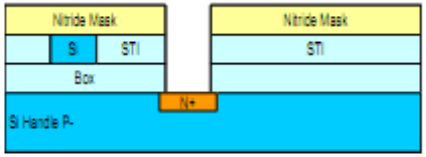


2) CMOS7 after standard STI (shallow trench isolation)

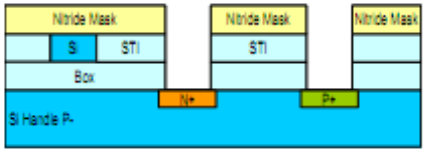


3) Protect nitride deposition 250nm with NBOX CUT photolithography and etch.

4) Implant NBOX CUT regions with phosphorous to form cathode doping

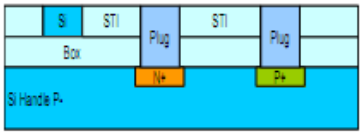


5) PBOX CUT photolithography and etch followed by implant into PBOX CUT regions with boron to form anode guard ring doping

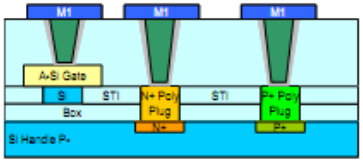


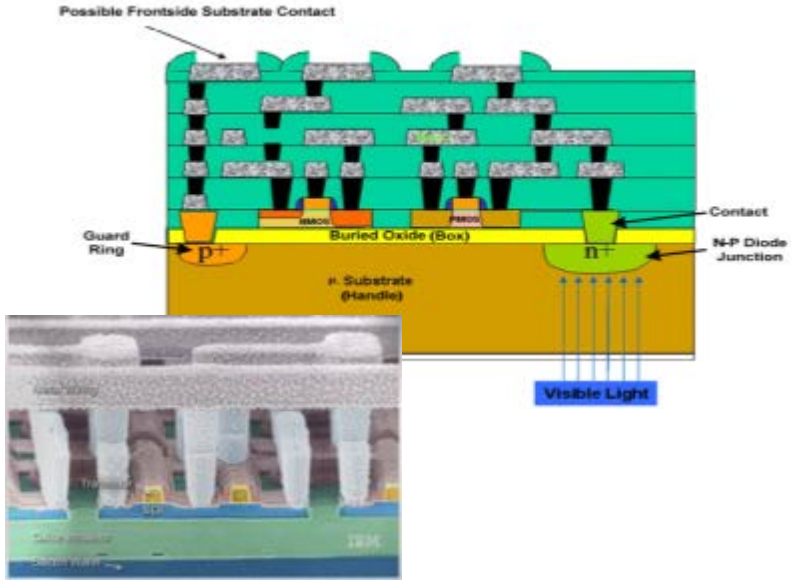
6) Polysilicon deposition into NBOX CUT and PBOX CUT areas followed by CMP (Chemical Mechanical Polish)

7) Protect silicon nitride is removed and devices are reinserted into standard CMOS7 processing

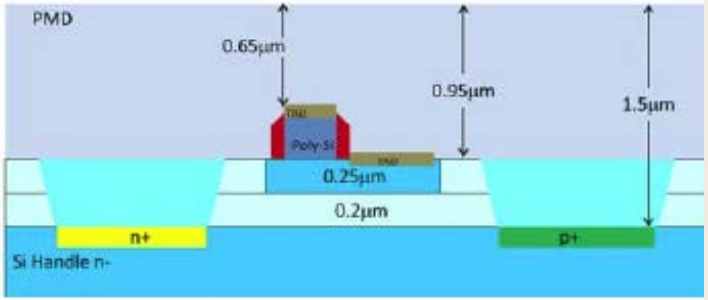


9) After standard CMOS7 processing, plug areas have been doped and contacts made to all diode plug regions

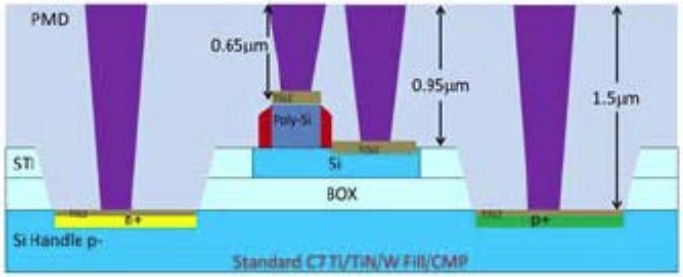




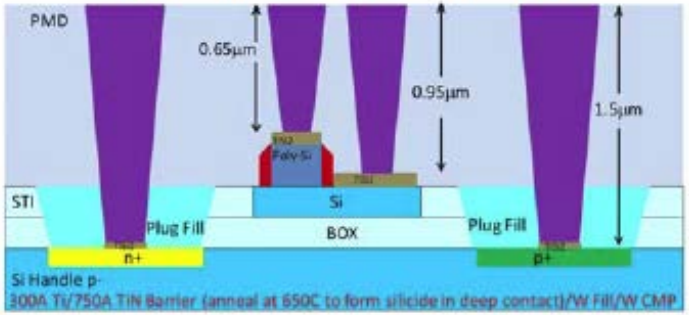
Forming High Quality Implant Contacts in Sandia CMOS7 SOI CMOS Process



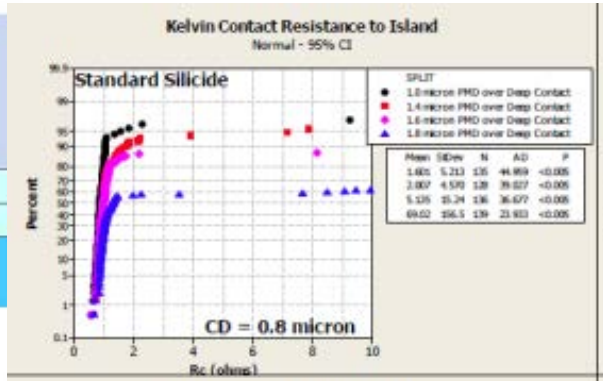
Pre-Metal Dielectric Stack

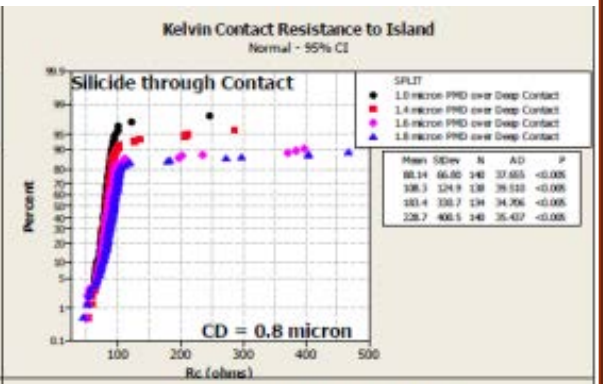


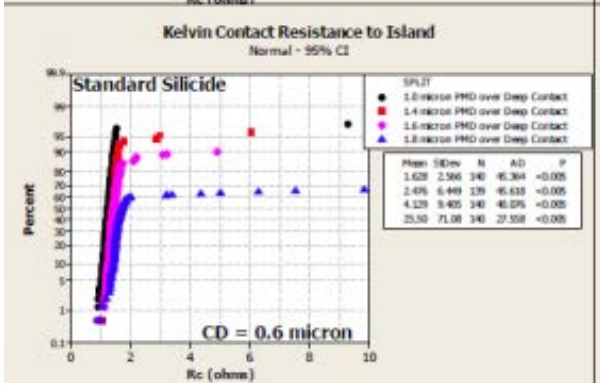
Implant Silicided Deep Contact Option

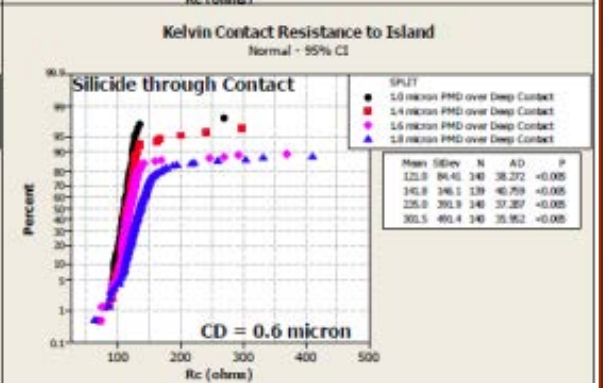


Trench Silicided Deep Contact Option





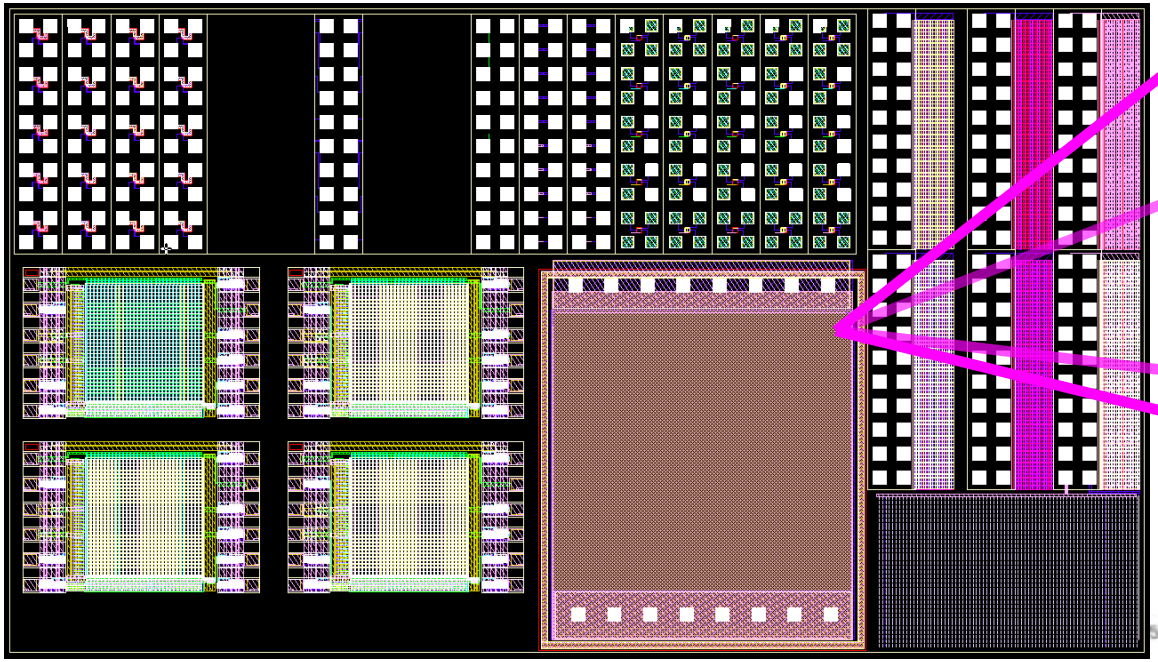


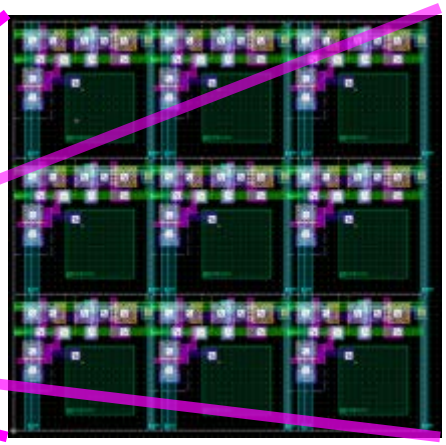


- **Two processes developed**
  1. **BOX etch, silicide, PMD, then contact etch**
  2. **BOX etch, PMD, then contact etch and silicide**
- **Deep silicide process good up to 1.6 µm PMD**

Prototype TBV Imager Structures in SNL CMOS7

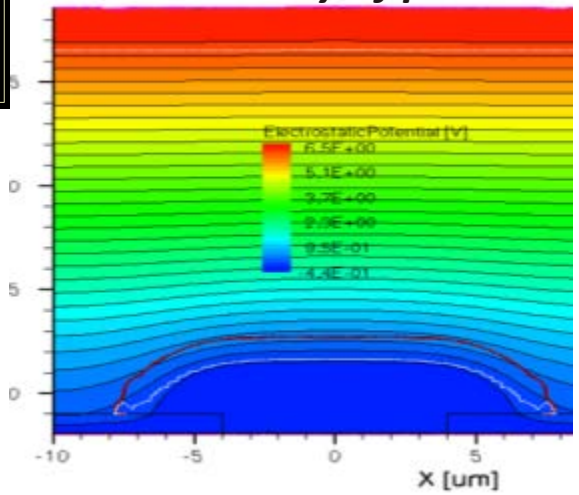
VOXTELOPTO





SFD pixel shown in 3 x 3 array of pixels

Layout of reticle being fabricated using through Si VIAs



Custom implant potential with 6V bias

4 different sensors on 30-µm pixel pitch. All pixels have photodiode area of 9.1 x 19.7-µm (20% fill factor).

a) VX-812a: No channel stop or field plate
b) VX-812b: With channel stop, no field plate
c) VX-812c: With channel stop and 1-µm field plate
d) VX-812d: With channel stop and 3-µm field plate

VX-812

Imager Fabricated in SNL CMOS7 Using TBV (through BOX via)

Imaging a large target on the ceiling of the lab.

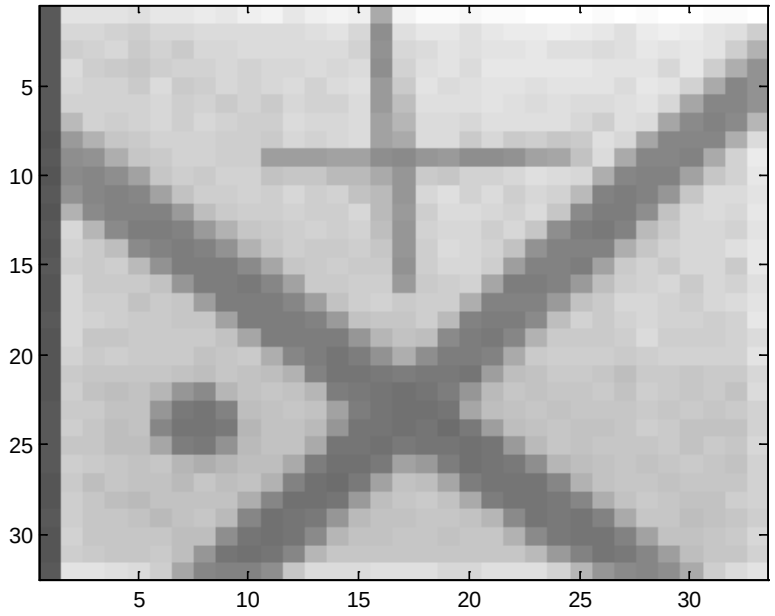


Image with 1 ms integration time (high level of illumination).

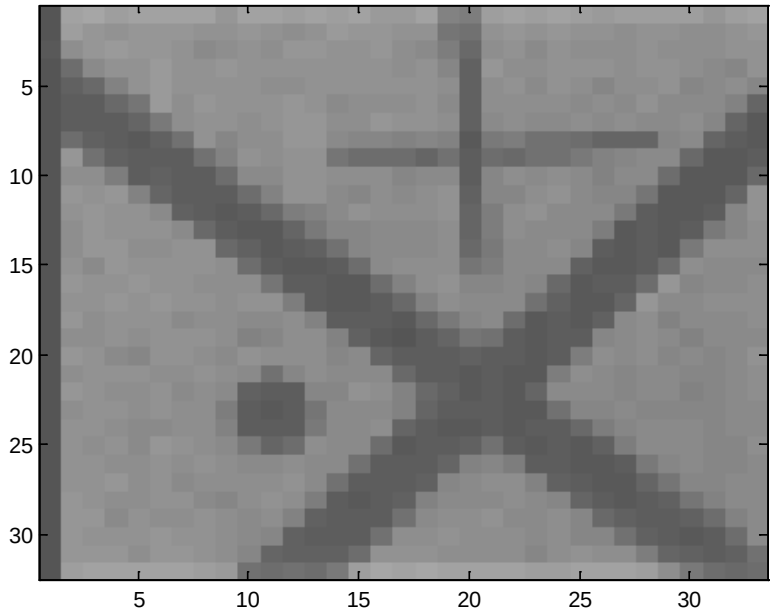
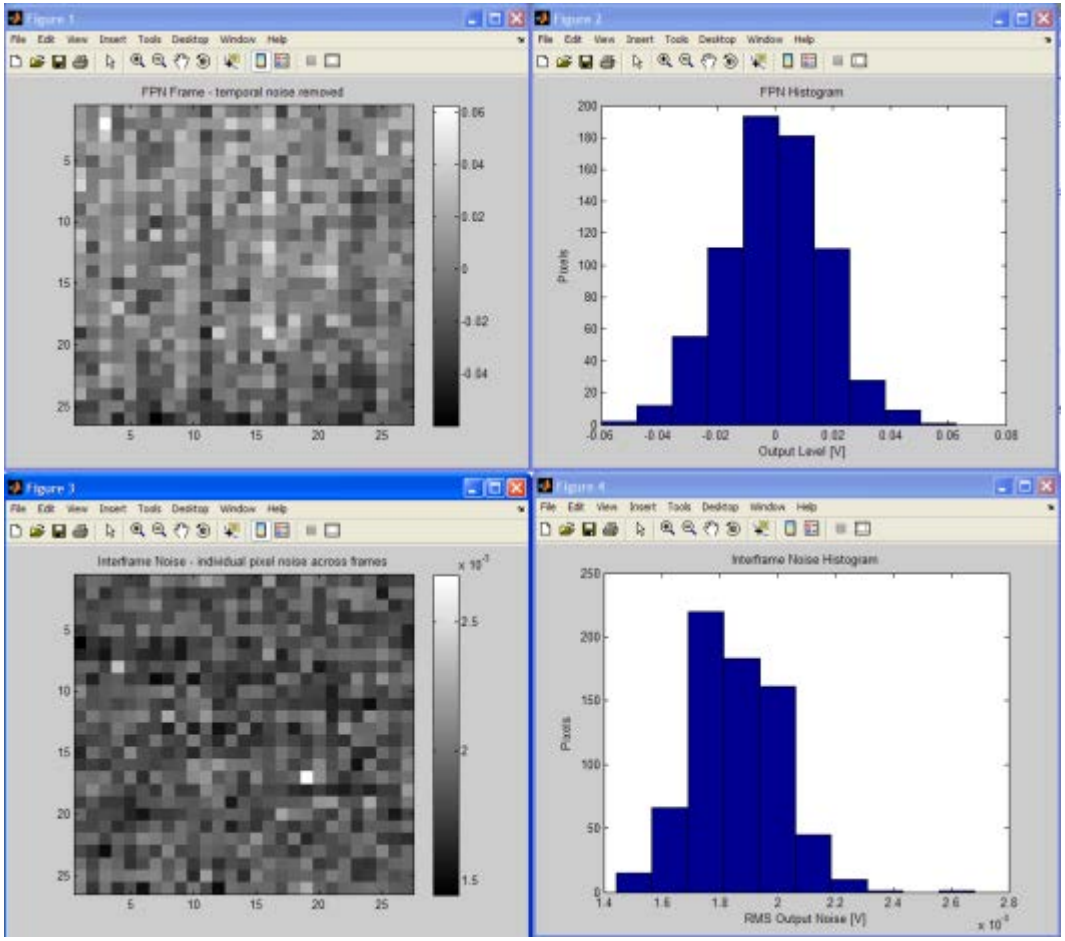


Image with 50 ms integration time (low level of illumination).

- **Edge pixels see more signal as they are collecting charges from the surrounding handle wafer substrate – array does not have a pixel guard ring.**
- **Far left column is row clamp.**

VX-812:
FPN and Read Noise

Captured 100 frames in the dark. Read noise is dominated by scope based camera system. FPN seems realistic for the readout architecture that was used.



Full Well
2.0 V = 525 ke-

Sensor FPN
17.2 mV = 4514 e- (0.9%)

Read Noise
read noise of sensor is ~400 µV or 105 e-)

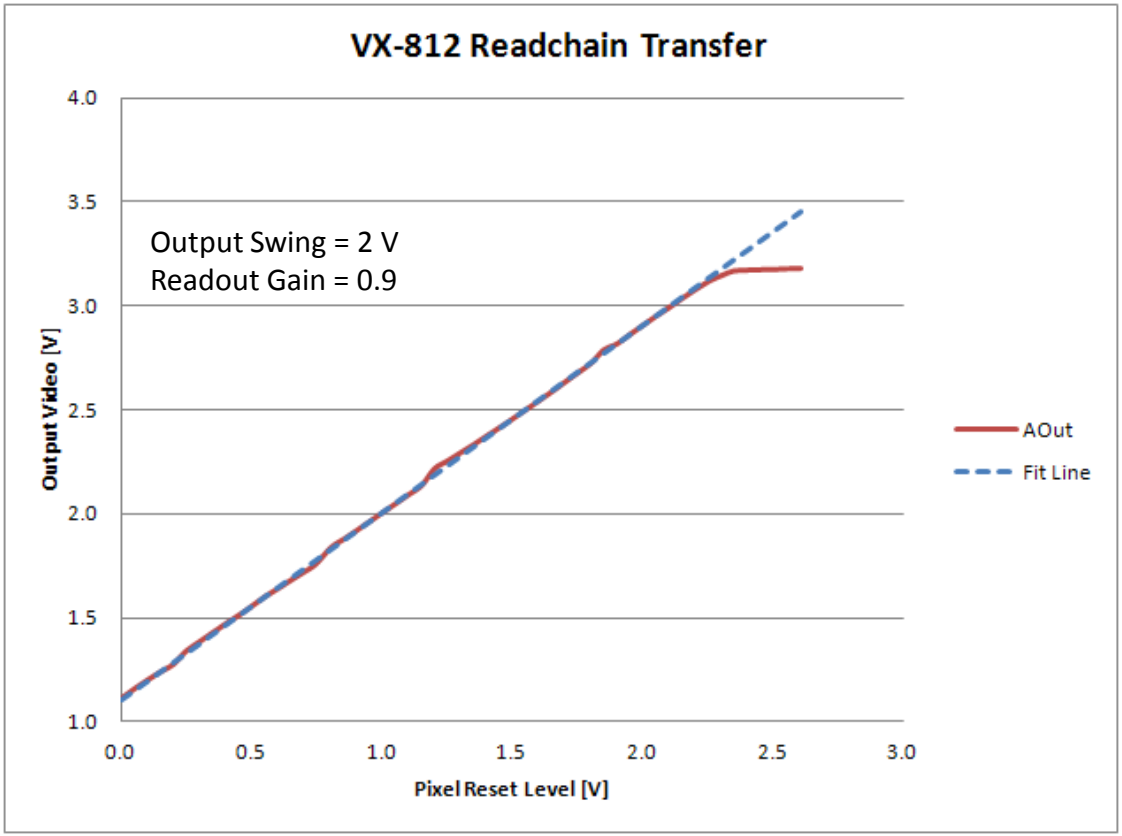
Dynamic Range
12-bits

VX-812:

Dynamic Range/ Readout Transfer Function

VOXTELOPTO

Sweep pixel reset level with short integration time (33 µs) and device in the dark. Data taken using averaging function on scope. Better data could be attained using new camera system if required to get linearity curve.

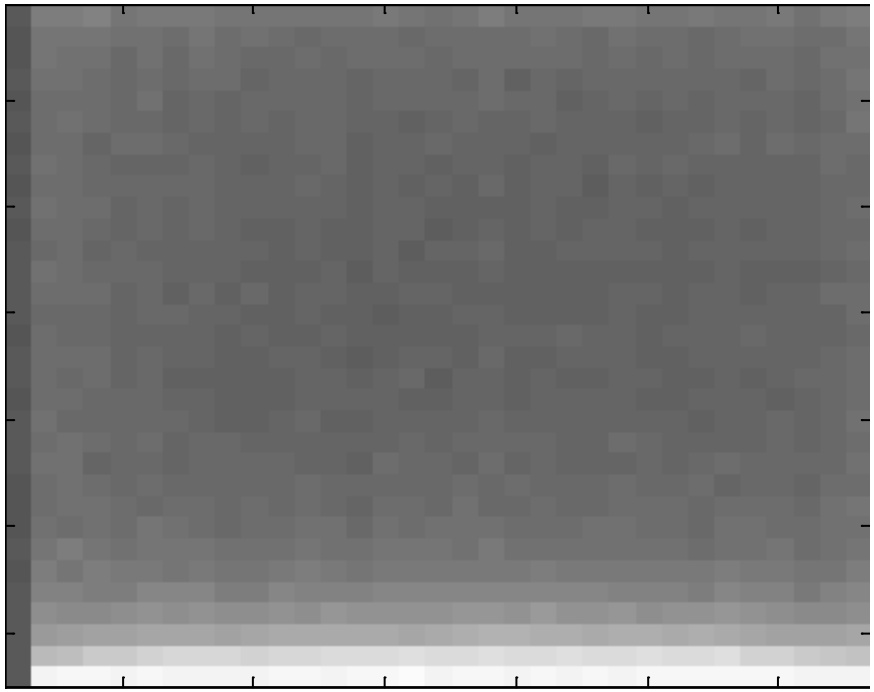


Measured readout swing and gain match simulated results.

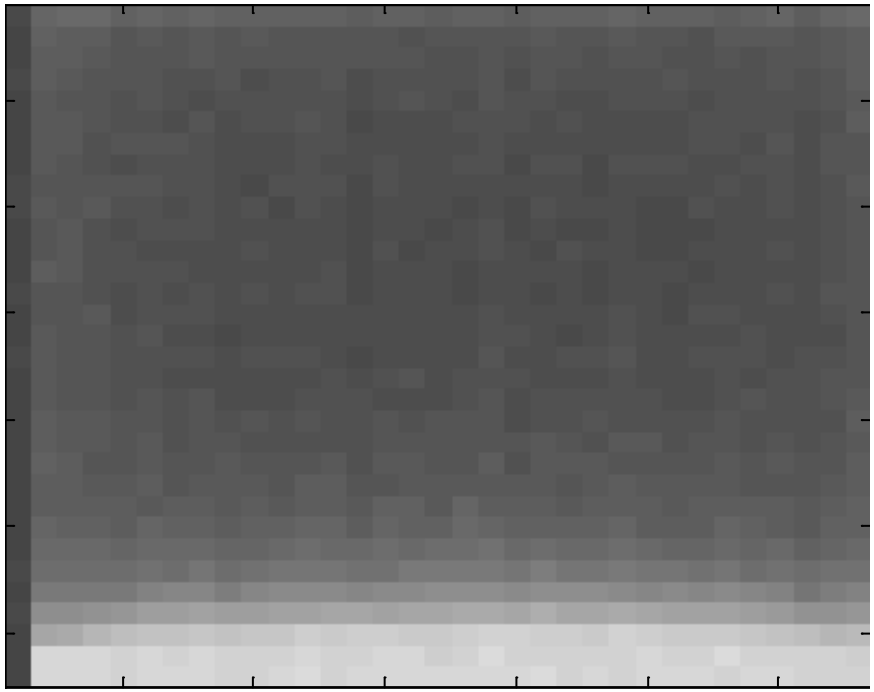
Nominal simulated pixel reset level is 1.8 V (12 bits) -may be able to increase to 2 V to get better range.

VX-812:

Dark Current Non-Uniformity



V_{BIAS} = 0.753 V, 1 ms integration time



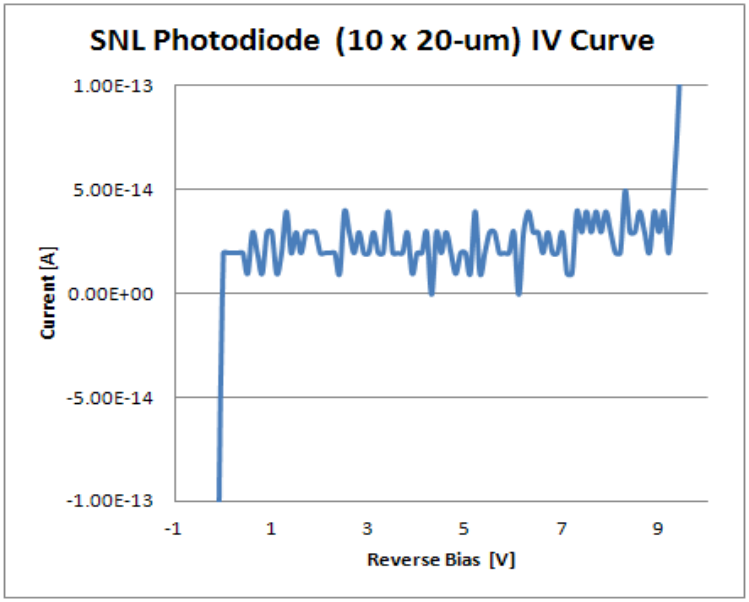
V_{BIAS} = 0.905 V, 1 ms integration time

Sensor FPN

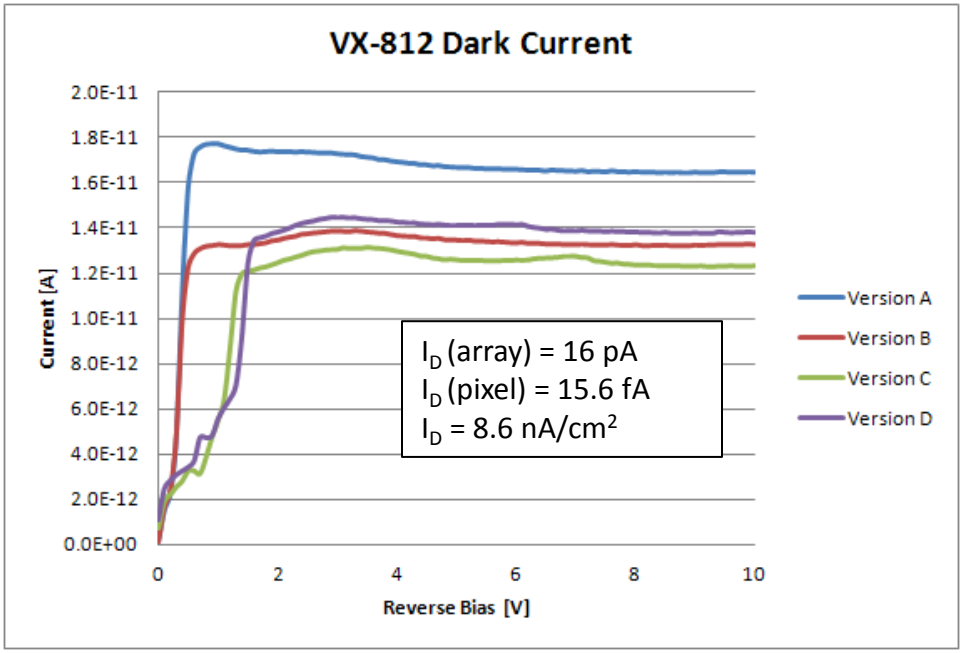
17.2 mV = 4514 e- (0.9%)

VX-812:
Dark Current Measurements

All dark current measurements taken with wafer probe using SPA (semiconductor parameter analyzer).



Single pixel test structure – most likely limited by SPA resolution.

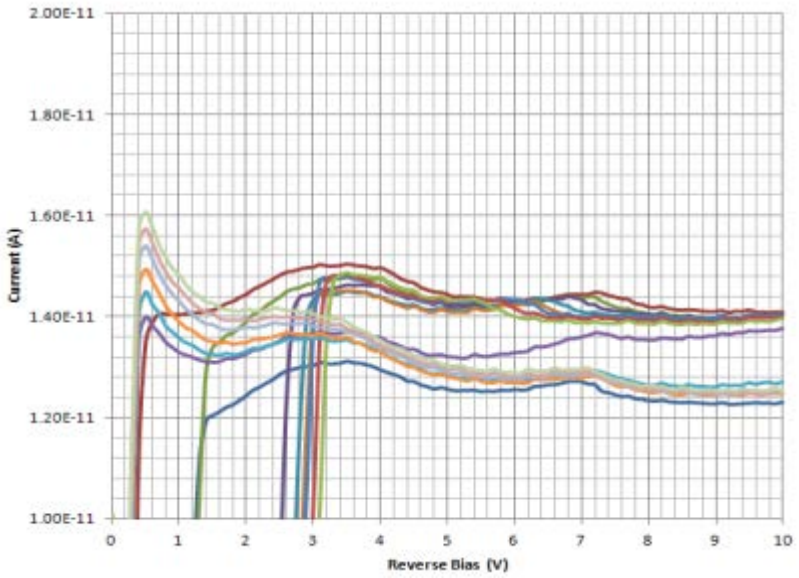


32 x 32 array comparison with floating field plate bias on versions C and D.

Dark current measurements for photodiodes made in standard CMOS7 p+ handle wafers (not optimized for imaging detectors).

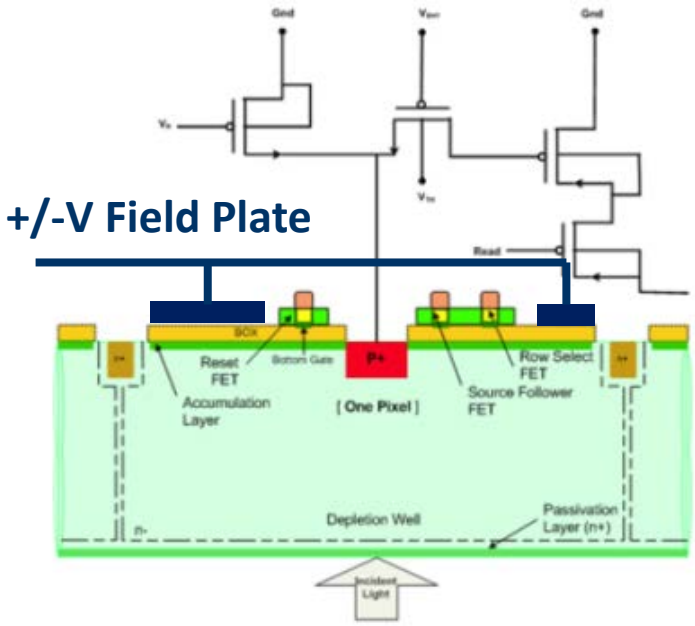
VX-812:

Dark Current Measurements



Field Plate [V]	I_{dark} [nA/cm²]
-20	6.9
-10	7.2
0	7.8
+10	7.7
+20	7.7

Pixel Version	Channel Stop	Field Plate	I_{dark} [nA/cm²]
A	No	No	9.0
B	Yes	No	7.2
C	**Yes**	**1.0-µm**	**6.8**
D	Yes	3.0-µm	8.6



Reverse bias on field plate on BOX seems to reduce dark current by small amount.

Summary of Sandia Monolithic Detector Process Development

VOXTELOPTO

- Deep trench through BOX silicide contact established at Sandia CMOS7 SOI CMOS process
- Test structures and prototype imagers fabricated, characterized, and demonstrated
- Double SOI Wafers specified and procured for future detector processing
- Next generation imager being selected for integration with new process
- Next…discussions of recent rad tolerant SOI CMOS detector designs

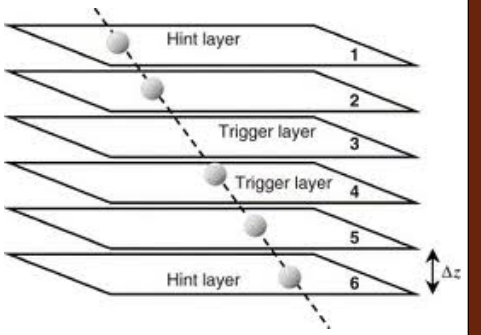
DE-SC0002421:
Semiconductor Tracking Detectors

VOXTEL OPTO

Problem

Existing CCD Trackers are

- too slow,
- too expensive,
- too thick
- data bandwidth intensive

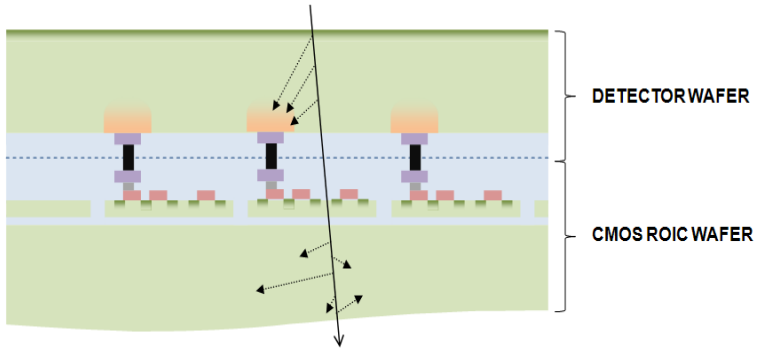


CMOS imagers

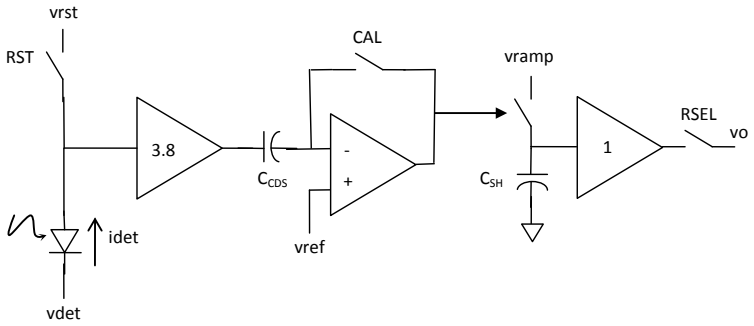
- lack sensitivity
- cannot detect through detective cross section
- Not rad hard

Solution

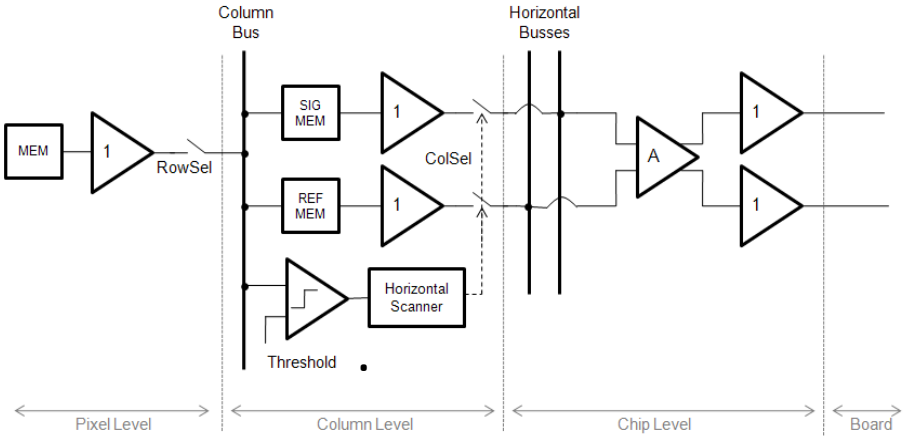
- 3D Wafer stacking of detector layers on CMOS
- SOI CMOS process for radiation tolerance
- Small pixel, thin silicon for occupancy
- Record time of flight and amplitude
- Use sparsified data readout
- Use stitching to photo-compose large imagers
- cannot detect through detective cross section
- Not rad hard



Tracking Detector Pixel Circuits

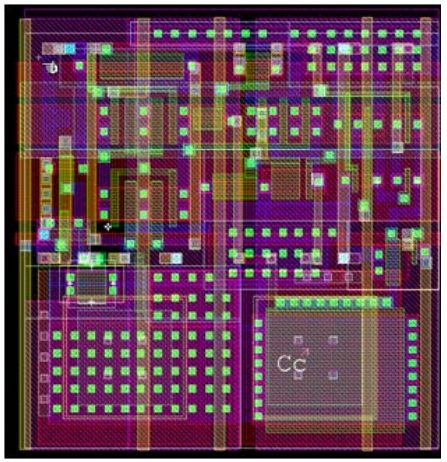


Vertex detector pixel block diagram.



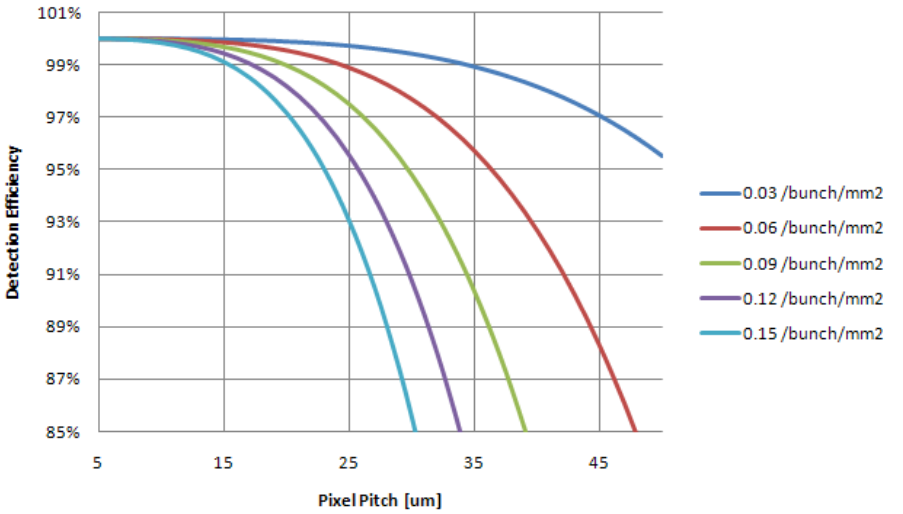
Vertex detector sparse readout architecture

- **Each pixel uses direct integration followed by an auto-calibrated comparator.**
- **output of comparator samples the event ramp signal**
- **Time-of-arrival and amplitude information are read out during the dead time between frames.**
- **Readout uses pixel-, column-, and chip-level processing to reduce fixed-pattern noise sources on the ROIC.**
- **In sparse scanning operation, column read out if column flag indicated pixel "hit"**

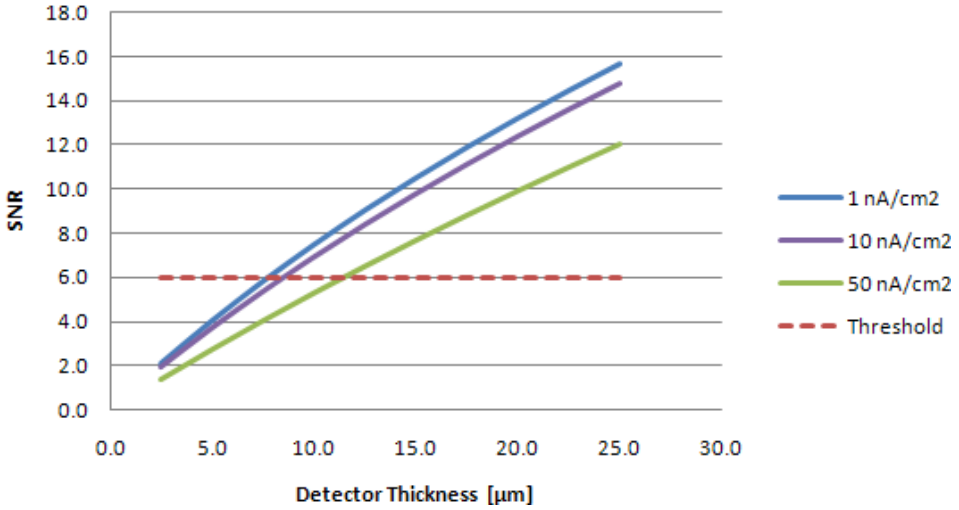


15 µm vertex detector pixel layout. The in-pixel comparator requires 70% of the pixel layout.

Specifying Tracking Focal Plane



Detection efficiency analysis, assuming single event storage per pixel.



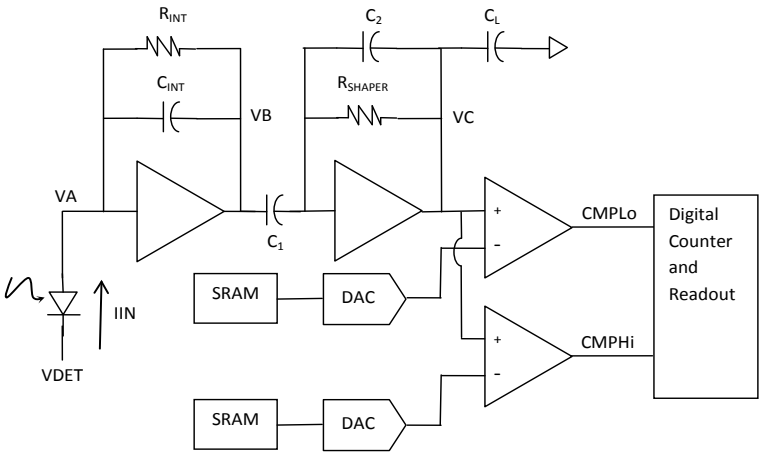
STN calculated as a function of detector thickness assuming read noise of 22 e–, 15 µm pixel pitch, and 1 ms integration (active) time.

- **Pixels smaller than 25 µm have detections efficiencies larger than 95%, even with occupancies in excess of 0.12 events/bunch/mm^2**
- **About 12-um thick detector achieves necessary STN to record event**
  – minimizes dark current

VOXTEL OPTO

Dual Threshold (DT) Photon/Particle Counting (PC) Readout Integrated Circuit

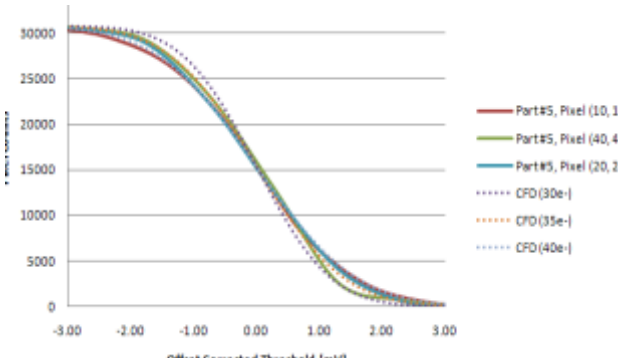
Layout: Pixel and 3 x 3 Pixel Block



Pixel Circuit Layout Showing Multi-counting modes

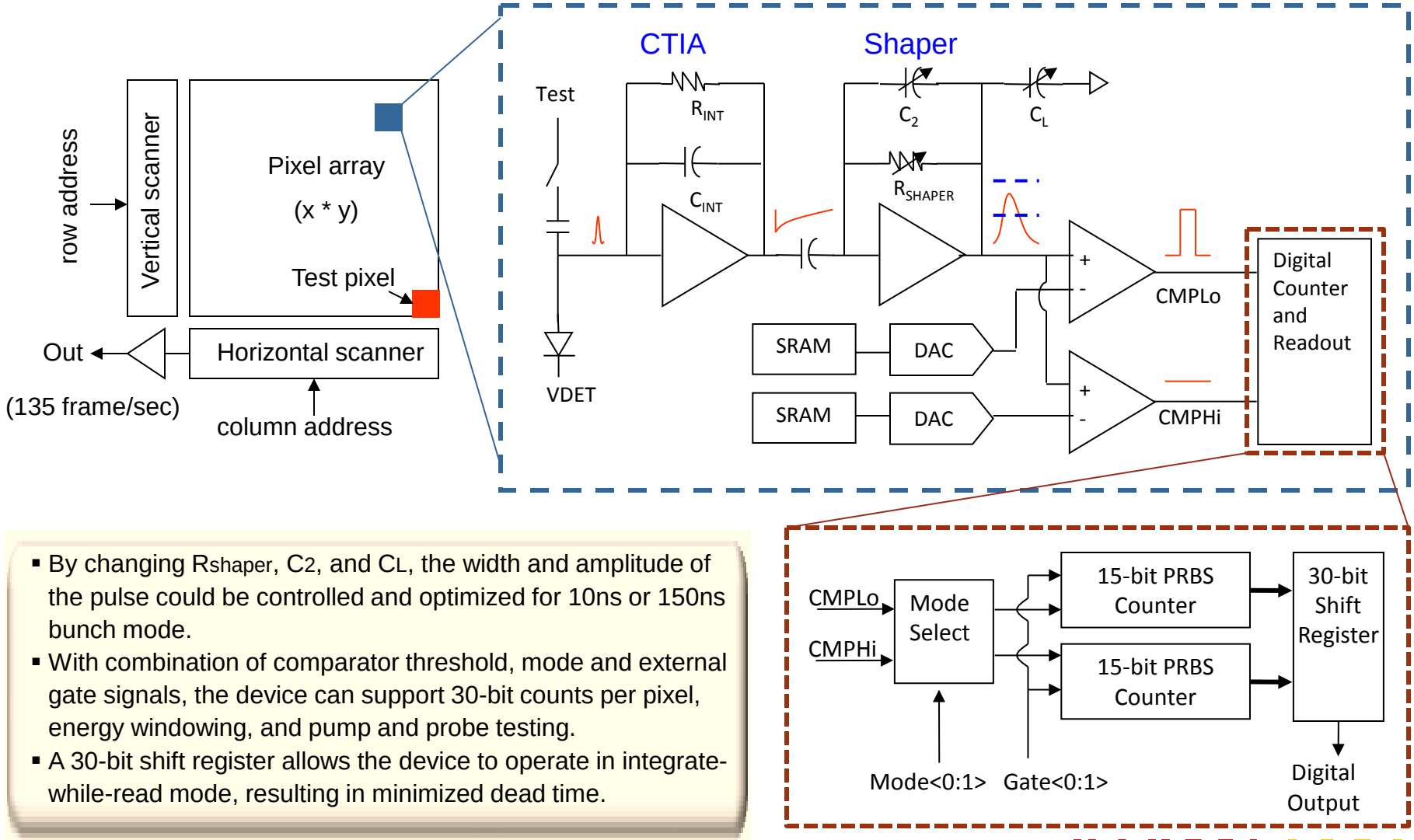
Performance	Pilatus II	DUPRAE (Phase I)	DUPRAE (Phase II)	Units
Technology	250	TSMC 250	TSMC 250	nm
Resolution	44 x 78	48 x 48	80 x 150	col x row
Pixel Size	172 x 172	130 x 130	120 x 120	μm^2
Pixel Count Rate	1	10 &100	1 & 10	MHz
Max. Global Count Rate	100	100,000	100,000	MHz
Threshold Settings	1	2	2	(-)
Programmable Threshold	6	2 x 3	8-column & (2x3)	bits
Counter	20	30 (2 x 15)	30 (2 x 15)	bits
Noise	123	37 (low) / 62 (high)	25 (low) / 60 (high)	e- (RMS)
Energy Resolution	1000	400/ 600	250/600	eV
Min X-ray energy	2.14	2	2	keV
Readout Scheme	Integrate then Read (ITR)	Integrate While Read (IWR) or ITR	IWR or ITR	
Dead Time	2820	2	2	ns
Readout Time	5	5	.05	ms

Competitive Specification



Measured Noise Data (40 e- rms)

DT Sensor Functionality

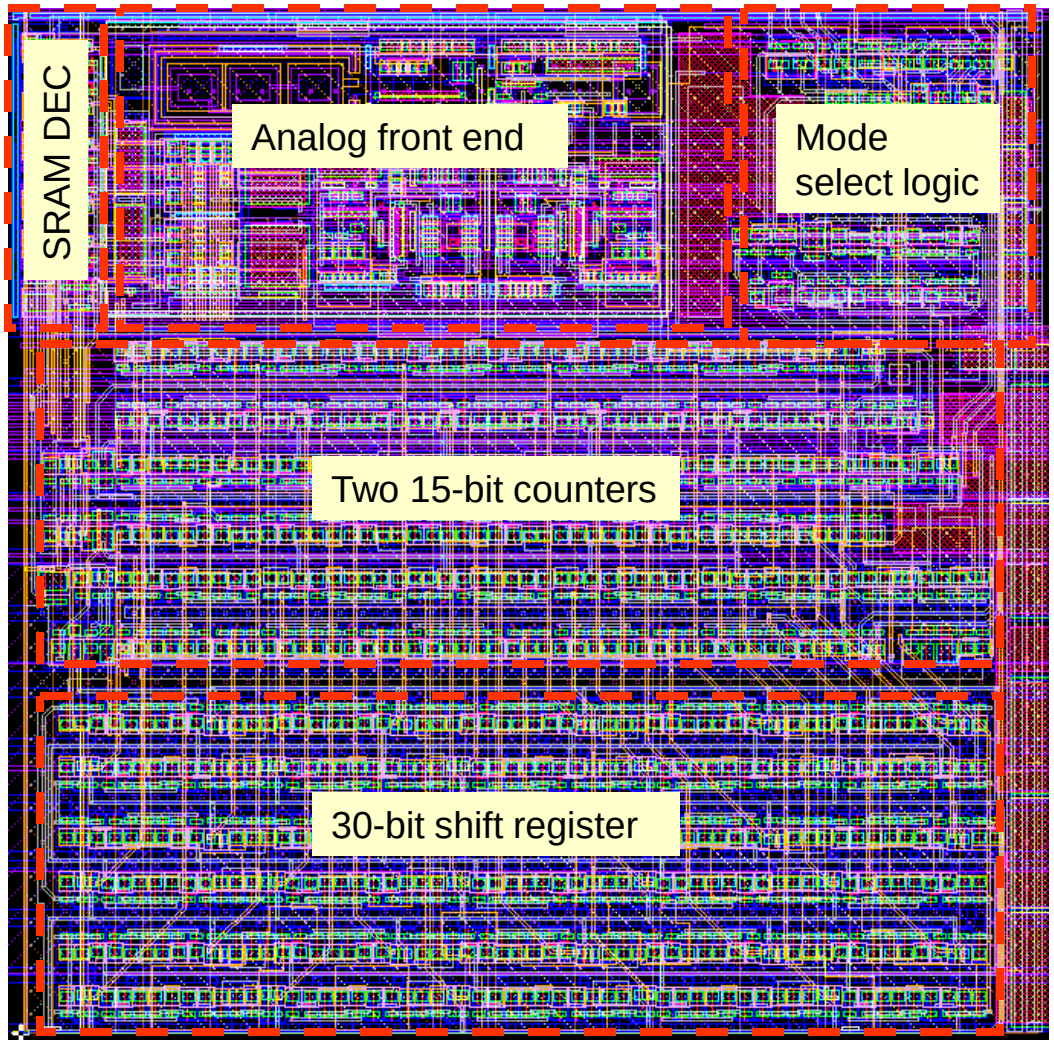


- By changing Rshaper, C2, and CL, the width and amplitude of the pulse could be controlled and optimized for 10ns or 150ns bunch mode.
- With combination of comparator threshold, mode and external gate signals, the device can support 30-bit counts per pixel, energy windowing, and pump and probe testing.
- A 30-bit shift register allows the device to operate in integrate-while-read mode, resulting in minimized dead time.

VOXTEL OPTO

Dual Threshold Detector:

Pixel Layout



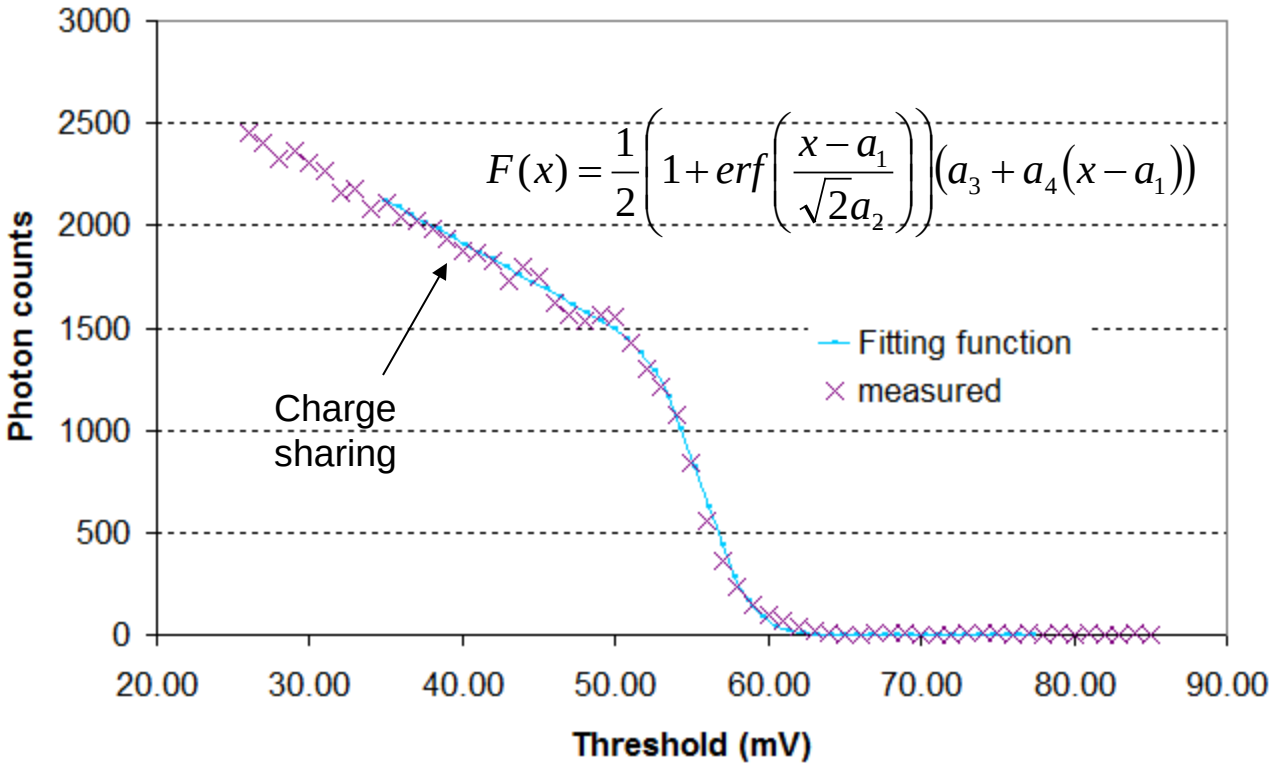
- TSMC 0.25 µm CMOS
- 130 µm by 130 µm
- 20% analog, 80% digital

VOXTEL OPTO

Dual Threshold Detector:

Threshold Scan with Iron-55

X-ray Source:
Fe55 (5.9keV)

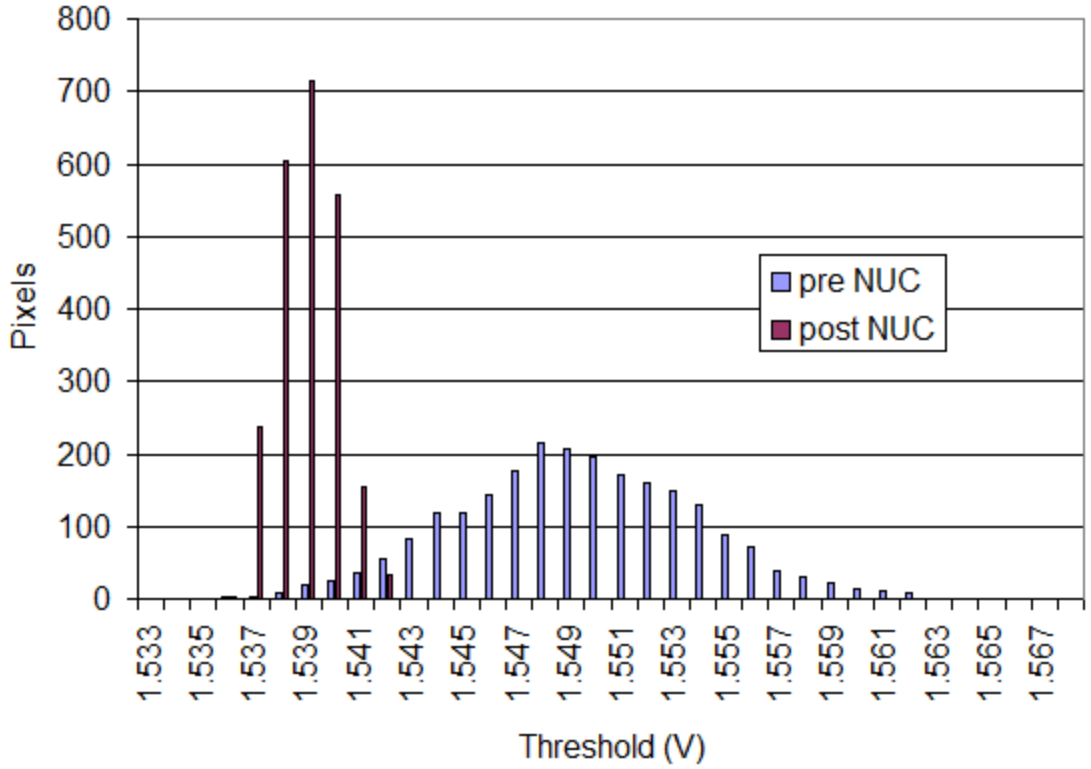


Conversion gain and noise numbers have been calculated from this threshold scan measurement. In 150ns mode the conversion gain is 32 µV/e- and the noise (detector + pixel circuit + x-ray source) is 77.5 e- or 283eV.

VOXTELOPTO

Dual Threshold Detector:

Non-Uniformity Correction

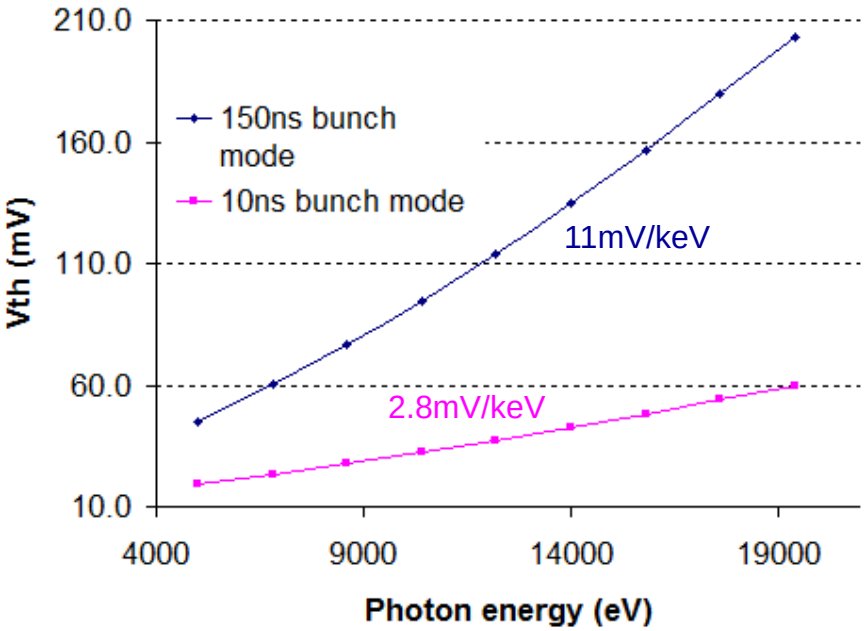


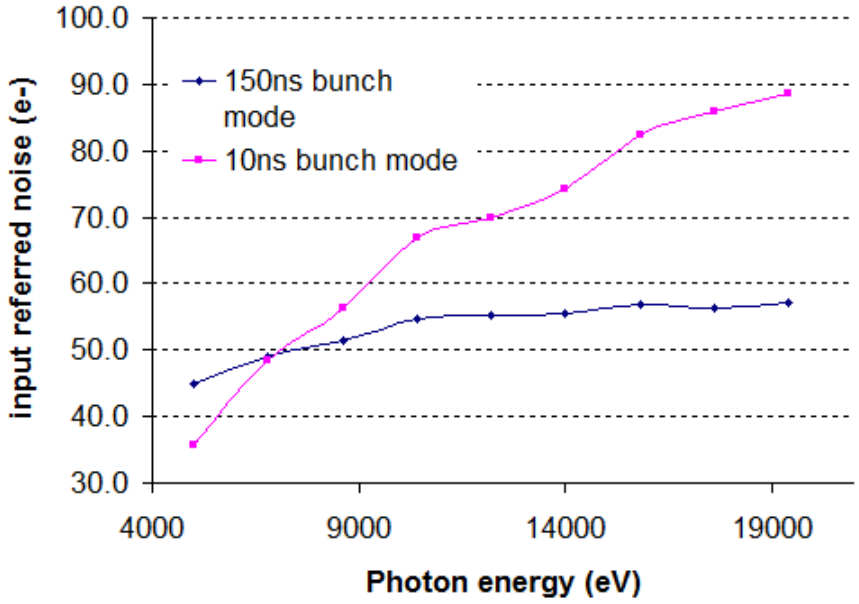
- Threshold distribution across the array when 5.9keV equivalent test charge is injected to each pixel.
- Distribution of threshold without NUC is 4.54 mV or 502 eV. Using the 3-bit in-pixel calibration of the comparator threshold, the non-uniformity is reduced to 1.15 mV or 127 eV.

VOXTELOPTO

Dual Threshold Detector:

Energy response





- Test pulse charge are injected to a pixel
  - 150 ns bunch mode: charge pulse with 22 ns pulse width and 1 MHz repetition rate.
  - 10 ns bunch mode: charge pulse with 5 ns pulse width and 1 MHz repetition rate.
- 6.5% and 5.6% non-linearity on 150 ns and 10 ns bunch mode respectively across 5k~20keV.
- Input referred noise increases with photon energy especially for 10 ns bunch mode.

VOXTELOPTO

DT-PC Sensor Summary and Future Developments

Summary of 1st Generation ROIC/FPA Design

Sensor Parameter	Units	Specification
Array size	pixels	48 x 48
Active area	mm	6.24 x 6.24
Pixel pitch	µm	130
X-ray energy	keV	5 – 20
Detector thickness (Si)	µm	520
Dynamic range	bits	2 x 15 or 30
Conversion gain	uV / e-	31
Read noise	e- / eV	46.7 / 170.5
Threshold dispersion	e- / eV	34.8 / 127.2
Bunch spacing @ >1% loss	ns	110
Power consumption	uW / pixel	300

A 2nd Generation ROIC/FPA Design is Underway

A 3-side buttable ~ 20 mm x 20 mm (e.g. 128 x 128) design is in progress with reduced pixel pitch (100 um).

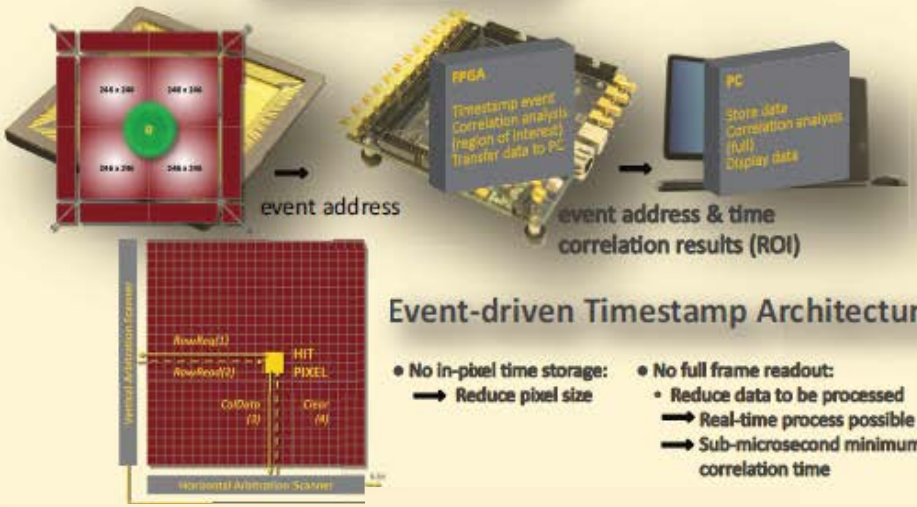
VOXTEL OPTO

Event-Driven FPAs

VOXTEL VX-807: Continuous Asynchronous, Time-resolved, Event-driven, Photon Counting Detector (50 MCPS)

Event-driven Timestamp X-ray Photon Detector (EDTS-XPD)

Camera Architecture



Event-driven Timestamp Architecture

- No in-pixel time storage:
  - ⟶ Reduce pixel size
- No full frame readout:
  - Reduce data to be processed
    - ⟶ Real-time process possible
    - ⟶ Sub-microsecond minimum correlation time

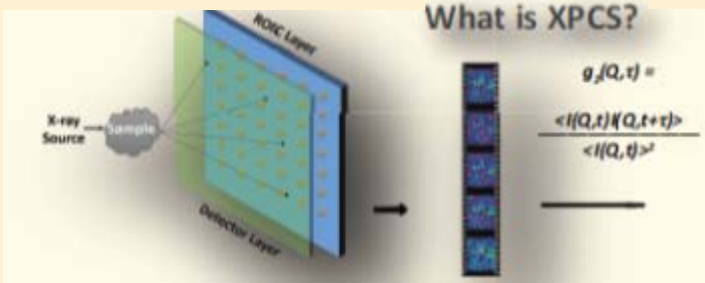
The *analog front end (AFE)* of the pixel is designed for low-noise operation, with the goal of being able to detect soft X-rays in the range of 0.5 to 2.0 keV with minimum temporal noise and threshold dispersion.

The EDTS-XPD *pixel* is implemented on a 40-µm pixel pitch.

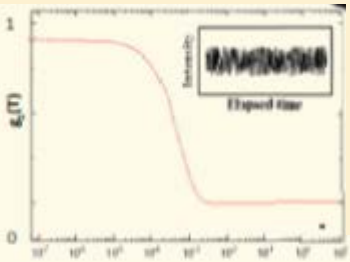
Sensor Specifications

Sensor Parameter	Units	Specification
Resolution	pixels	492 x 492
Area	mm	21.6 x 21.6
Pixel pitch	µm	40
X-ray energy	keV	0.5 – 2.0
Detector thickness	µm	20
Read noise	e- (RMS)	16
Threshold dispersion	e- (RMS)	17
Timing resolution	ns (RMS)	85
Sensor count rate	photons/sec	100e6
Power consumption	watts	3
CMOS process	-	TSMC 0.25 µm

What is XPCS?



$$g_2(Q,\tau) = \frac{\langle I(Q,t)I(Q,t+\tau)\rangle}{\langle I(Q,t)\rangle^2}$$

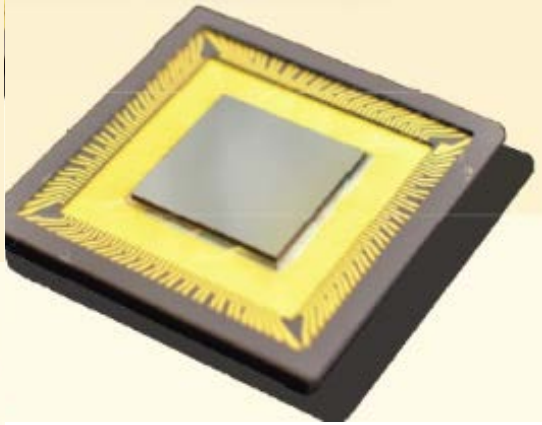


The sample is illuminated with a coherent beam.

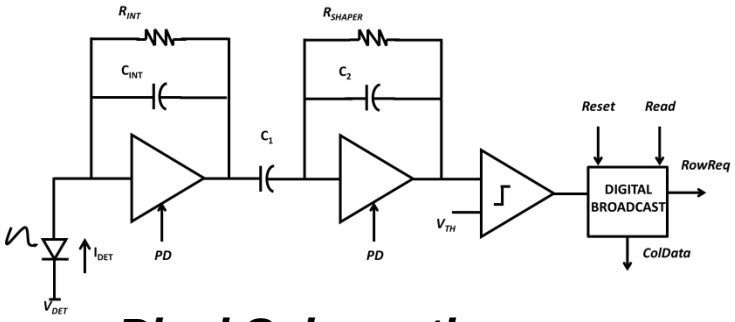
When the coherent X-rays are scattered from a disordered sample, the diffraction pattern has a grainy appearance known as speckle.

The speckle scattering pattern, I(Q, t), is autocorrelated in the time domain.

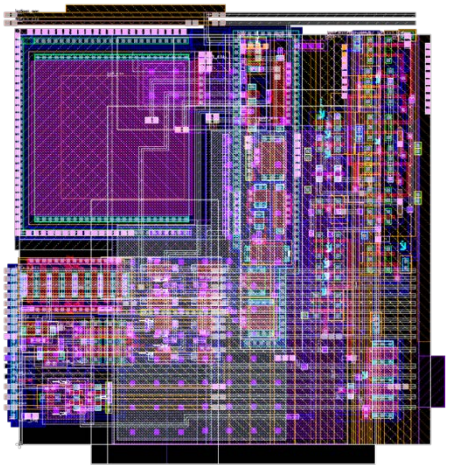
The resultant intensity-intensity function, g2(τ), gives us the dynamic properties of the sample.



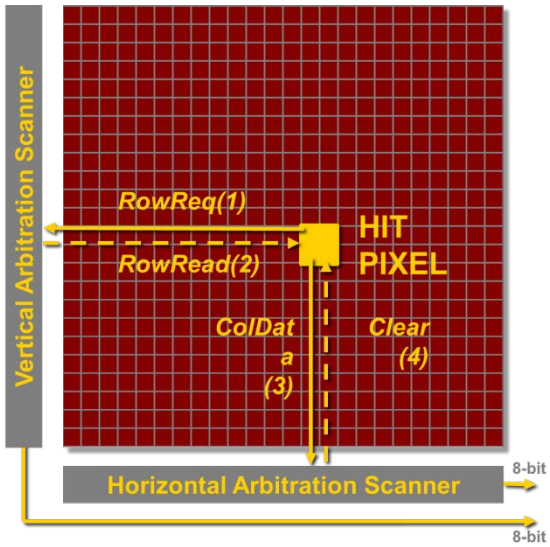
Pixel Circuit Schematic and Layout



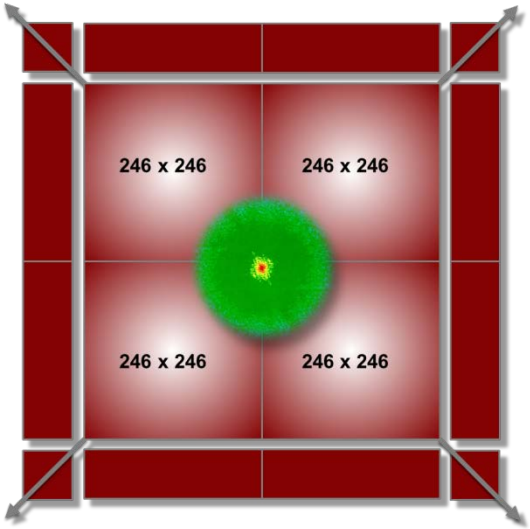
Pixel Schematic



Pixel Layout



Quadrant Arbitration



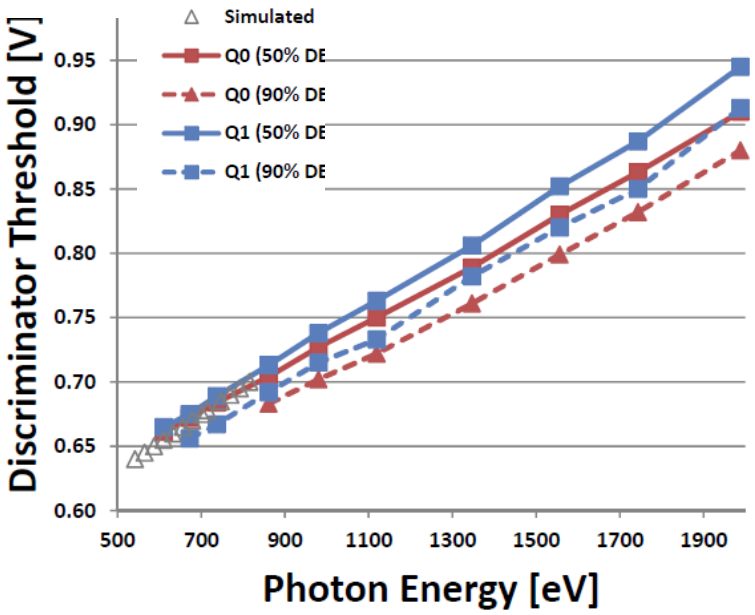
512 x 512 Format

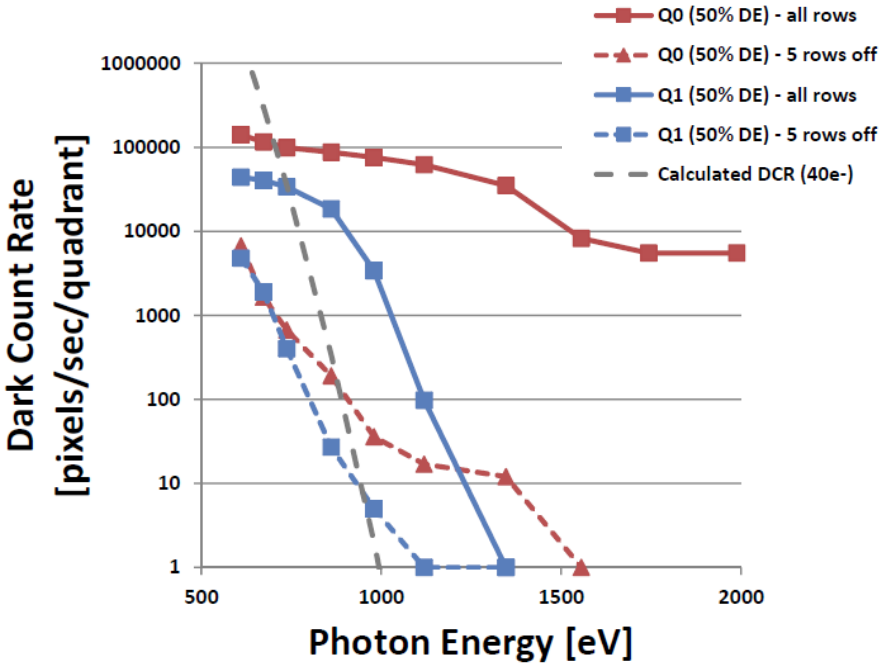
- **CTIA Amplifier with Shaping Amplifier Broadcasts Hit Events (Event driven readout)**
- **Arbitration circuits identify pixel address**
- **Address transmitted off chip to FPGA where it is time stamped to < 64 ns**

Measured Data:

Amplifier Conversion and Dark Counts

VOXTELOPTO

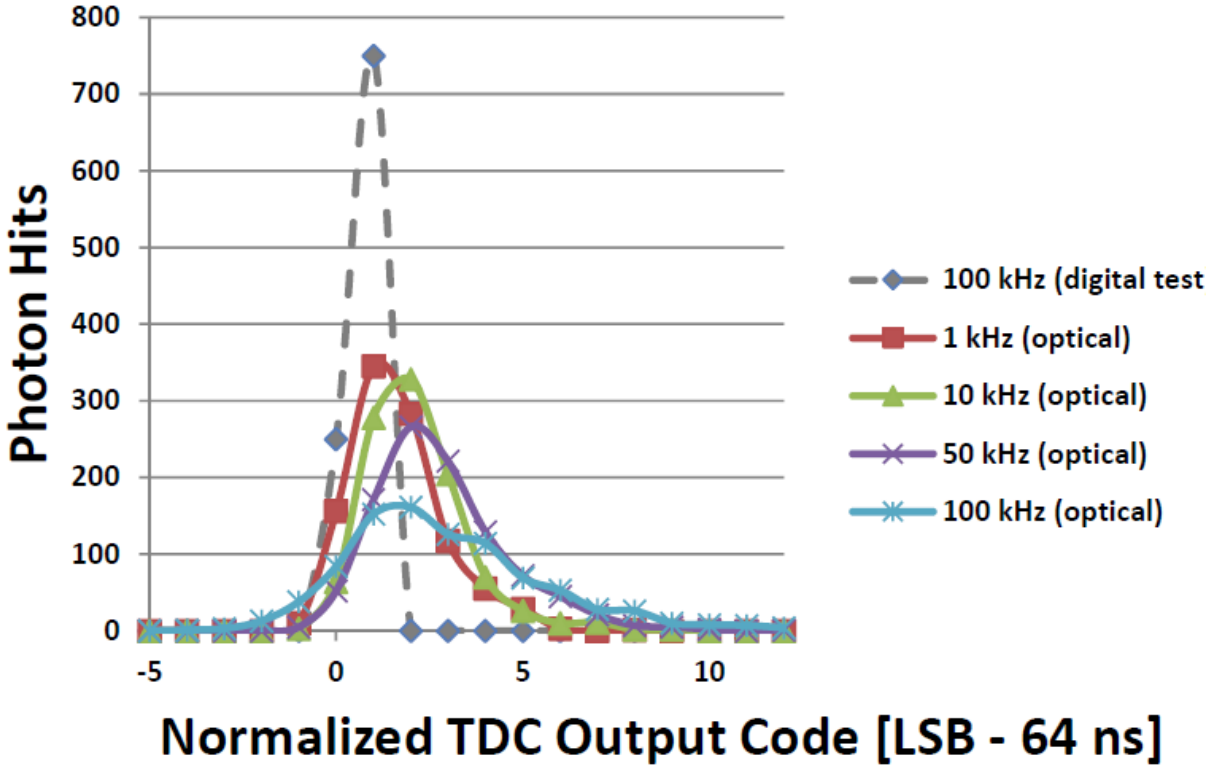




- Conversion gain (noise) is a function of signal amplitude (as CTIA saturates)
- Performance matched simulated performance (roughly linear with energy)
- The dark counts are dominated by a few bad pixels

Measured Data:

Discrimination and Timing



- 64 ns time stamps achieved in each quadrant at rates above 1 MHz
  - allows time correlated spectroscopy

Thank You

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