Pacific MicroCHIP Corp.

An ASIC with a Low Power Multichannel ADC for Energy and Timing Measurements

DoE award number: DE-SC0018566
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OUTLINE

- The company, its specialization/expertise
- Specifications for the multichannel ASIC for energy and timing mesurements
- ASIC core architecture with event-driven backend for detector streaming readout
- Phase IIB project objectives
- Modifications done for the 2nd Gen ASIC
- Assembled parts
- Updated PCB design
- 2nd Gen ASIC testbench setup
- ADC testing results
- Phase IIB project schedule
- Future plans

COMPANY

Pacific MicroCHIP Corp. is incorporated in 2006. It is headquartered in Culver City, California. Main focus – providing IC/ASIC design services and turnkey solutions. The office includes the working space and a laboratory for ASIC testing.

Core expertise:

- Analog (ADC/DAC, CTF, VGA, BG, LDO)
- Mixed Signal (PLL, CDR, SerDes, MDrv, TIA)
- RF (LNA, Mixer/Modulator, PA)
- Digital (RTL, Synthesis, P&R, Timing Closure, DFT, Verifications)
- Layout (CMOS/SiGe) down to 7nm

MULTICHANNEL ADC ASIC SPECIFICATION

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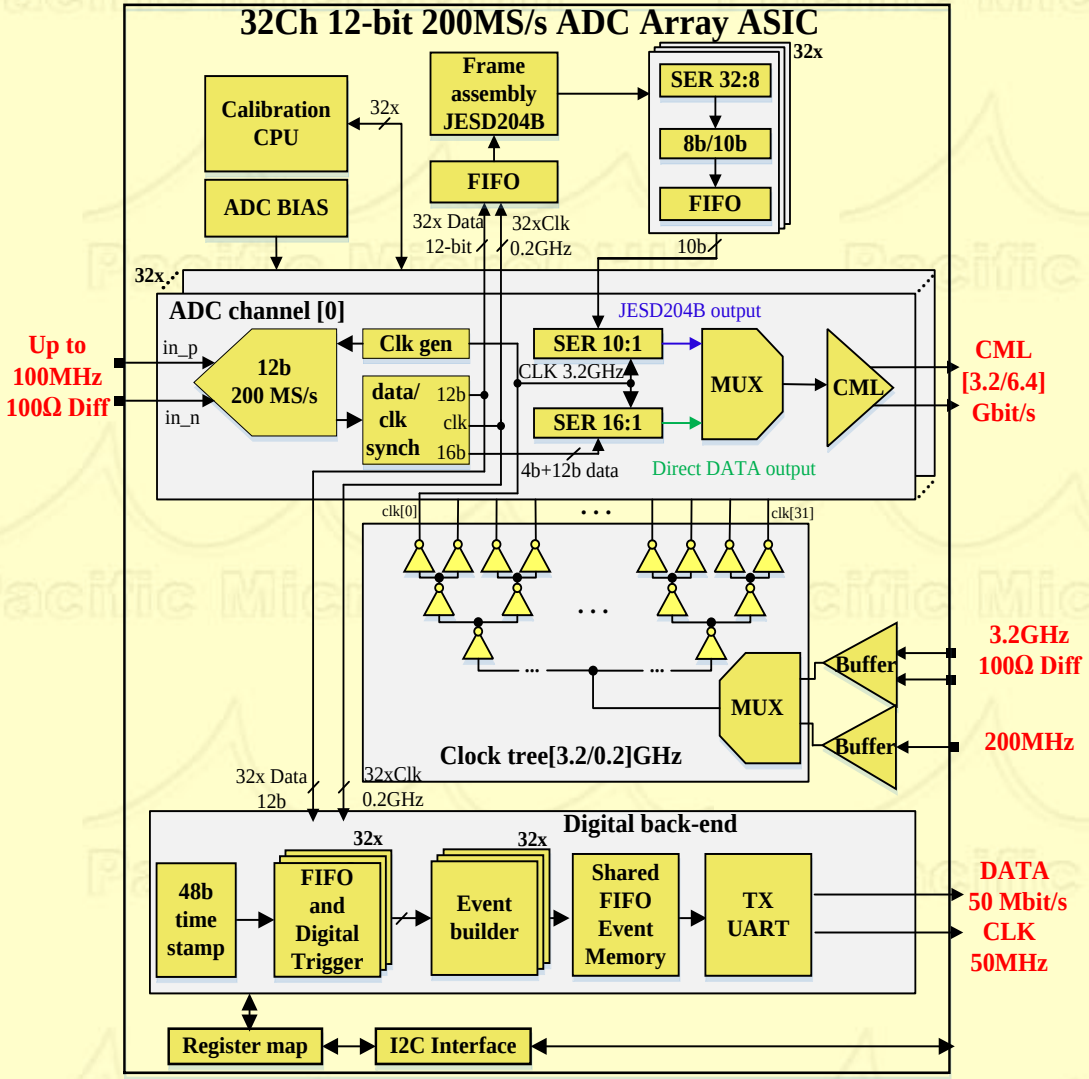
FEATURES:

- 32 independent channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input signal
- ENOB >9-bit
- Programmable input signal bandwidth 0.1-0.3 GHz
- Integrated event-driven digital backend
- JESD204B output data interface
- Extended temperature range
  -40C..+125C
- Low power consumption
- I2C interface for ASIC control



ADC CORE ARCHITECTURE

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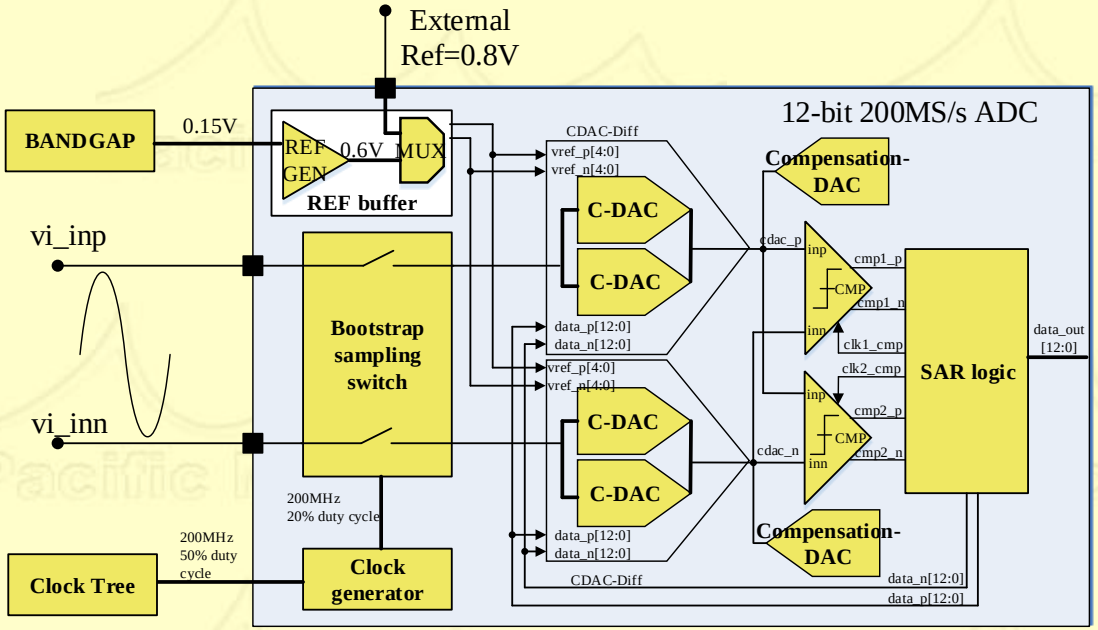
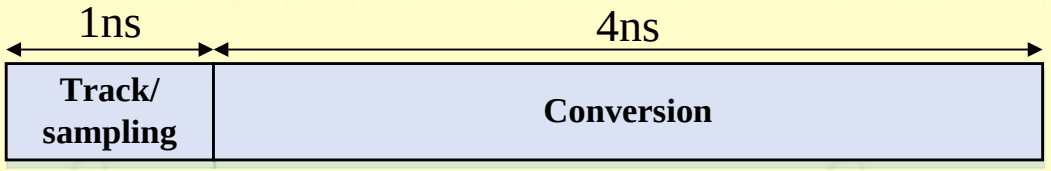
FEATURES:

- 12b SAR ADC architecture
- Segmented 3t-9b CDAC
- Optional external/internal ADC reference voltage source
- Fractional reference voltage
- Dual comparator
- Asynchronous logic
- Built-in FSM for comparator offset compensation
- Built-in FSM for CDAC non-linearity calibration

ADC CORE BLOCK DIAGRAM:



ADC TIMING DIAGRAM:



RAW ADC DATA OUTPUT

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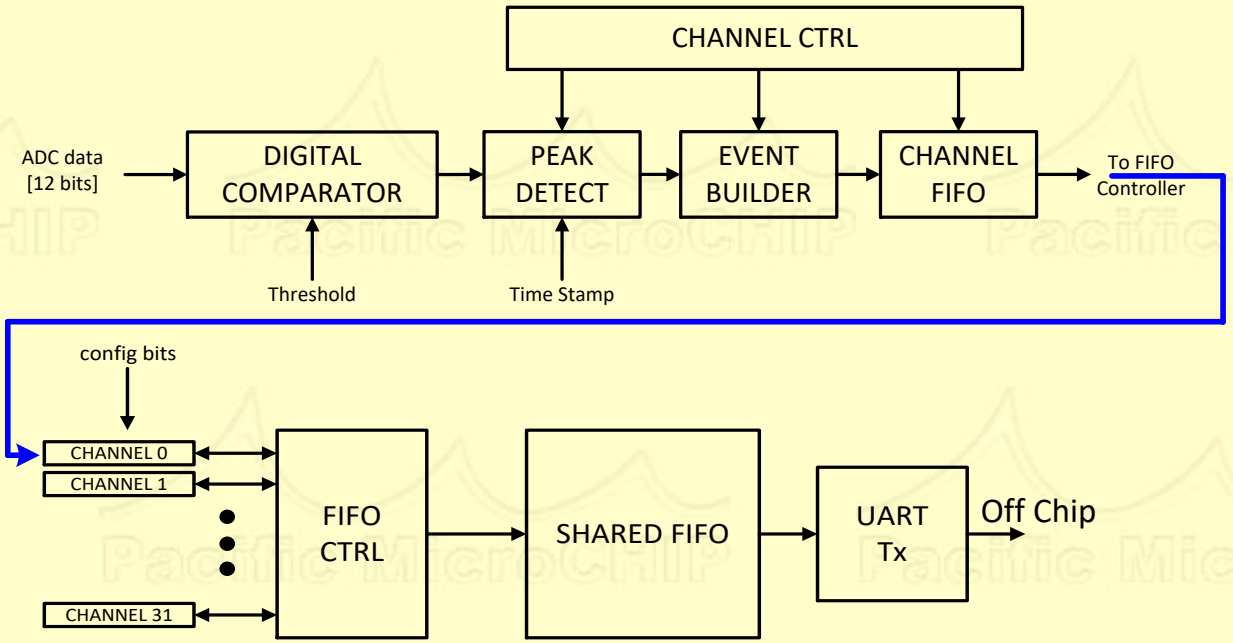
Mode	JESD 204B lanes	ADC per lane	Lane data rate	ADC data rate
Full speed	16	2	6.4Gbps	200MS/s
Half speed	8	4	6.4Gbps	100MS/s
Quarter speed	4	8	6.4Gbps	50MS/s

- Programmable ADC sampling rate of 200/100/50 MS/s
- Constant JESD204B output data rate 6.4Gbit per second
- Shared JESD204B output data interface between 2/4/8 ADCs reduces the number of interface lines, allowing high system integration density

EVENT–DRIVEN BACKEND

- This ADC output is monitored by a digital comparator with a programmable threshold
- When the ADC input exceeds threshold, a time stamp is assigned, and the peak value of the incoming ADC data is recorded.

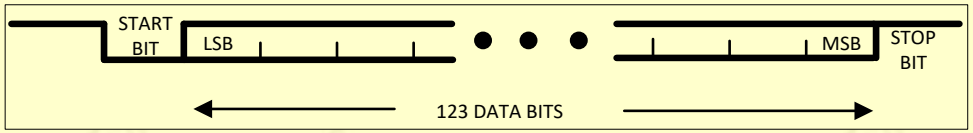


Event-driven digital backend was built in collaboration with LBNL. And we want to thank Dr. Carl Grace for his effort.

- When the event is completed, the relevant information is assembled into a packet by the Event Builder block. When the shared FIFO is ready, events stored in the channel FIFO are read out.

OUTPUT DATA FRAME

Bits	Field Name	Comment
[123]	Parity	Used to monitor integrity of data transmission.
[122]	Event Declaration	0 → test event (see text), 1 → normal
[121:119]	Fixed	Fixed bits - should always read value 3'b011
[118:107]	Window Interval	Determines the number of ADC samples to examine looking for a peak.
[106:102]	Channel ID	5-bit unique identifier.
[101:54]	TOA (Time of Arrival)	The timestamp of where the ADC value passed the threshold. Covers ~16 days at a 200 MHz clock rate.
[53:42]	TOP (Time of peak)	Supports shaper peaking times of up to 20 µs at a 200 MHz clock rate.
[41:30]	TOT (Time over Threshold)	Supports shaper pulse widths of up to 40 µs at a 200 MHz clock rate.
[29:18]	Peak Value	12-bit peak value recorded in the event.
[17:6]	Channel Threshold	12-bit threshold value used during this event.
[5:0]	Shared FIFO usage	For diagnostics and debugging.



50Mbps / 124+2bit / 32ch
≈ 12.4k events per second per channel

EVENT DRIVEN DIGITAL BACKEND TEST RESULTS

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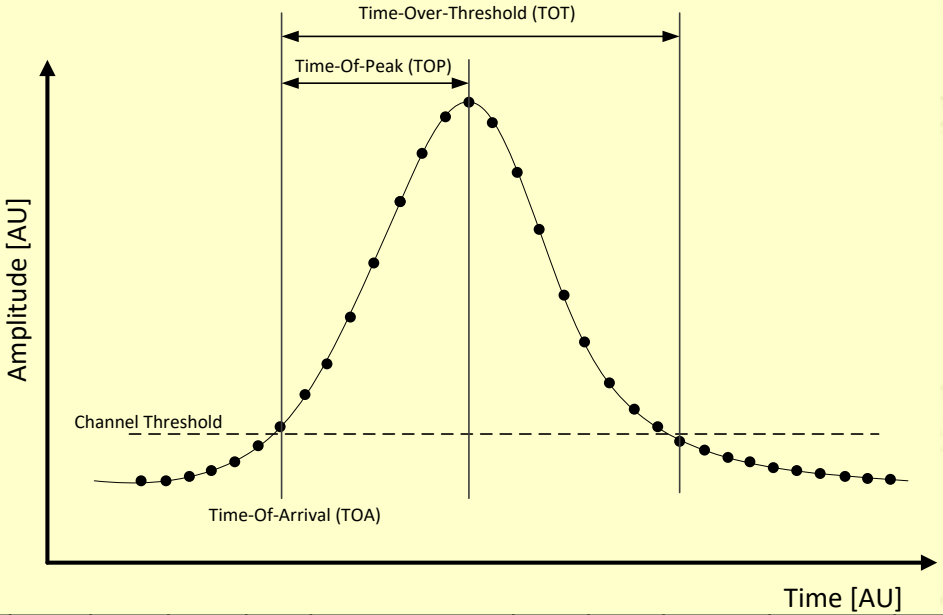
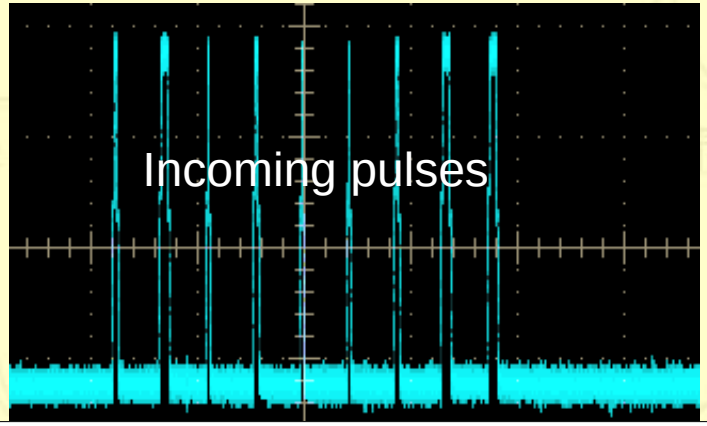
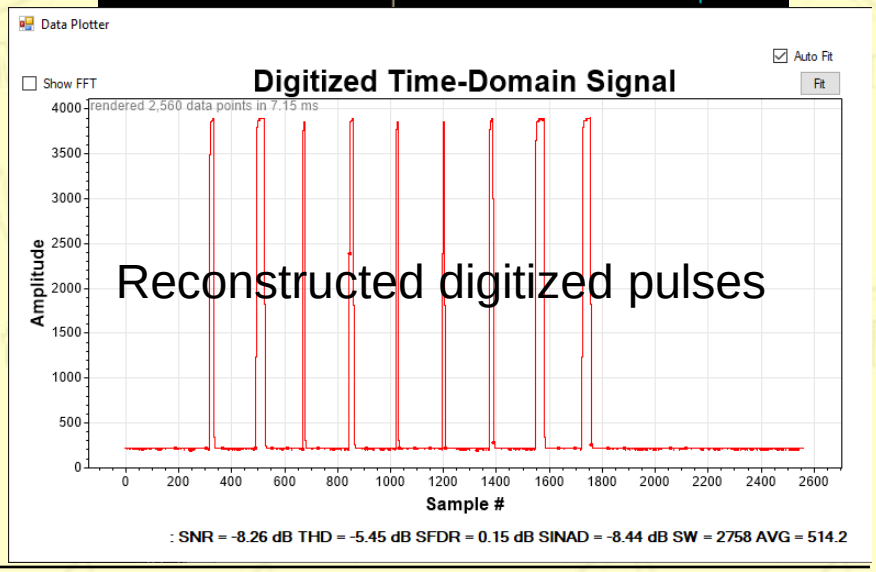
The event-driven backend was designed in collaboration with Dr. Carl Grace of LBNL. It is capable of extracting the TOT, TOP, TOA, and the peak amplitude of incoming pulse signals.







Par0	Event	Fixed	Wind	CH	TOA	TOP	TOT	PEAK	THRESHOLD	SHARED
1	1	3	64	4	578680317105	13	17	3893	1024	0
1	1	3	64	4	578680317281	11	33	3893	1024	0
1	1	3	64	4	578680317457	6	9	3861	1024	1
0	1	3	64	4	578680317633	13	17	3893	1024	1
0	1	3	64	4	578680317809	6	9	3861	1024	2
1	1	3	64	4	578680317985	6	9	3861	1024	3
1	1	3	64	4	578680318161	14	17	3893	1024	3
1	1	3	64	4	578680318337	14	33	3893	1024	4
0	1	3	64	4	578680318513	31	33	3904	1024	5

PHASE IIB PROJECT OBJECTIVE

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The performance parameters of the 1st Gen ASIC are required to be improved in order for the device to be used commercially. Several design mistakes were identified during the chip testing and must also be addressed within Phase IIB in the 2nd Gen ASIC and the evaluation PCB.

Phase IIB objective	Status
Fix issues discovered during 1st Gen ASIC evaluation	Done
Redesign and fabricate the chip (2nd Gen).	Done
Package the chips.	In process
Update the design and fabricate new PCB.	Done
Test and characterize the 2nd Gen ADC ASIC.	In process
Prepare updated datasheet and evaluation board for marketing.	In process
Submit deliverables to the DoE.	Pending

MODIFICATIONS DONE FOR THE 2nd GENERATION ASIC

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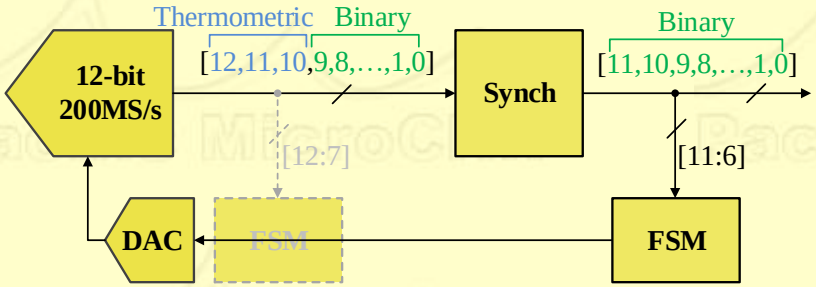
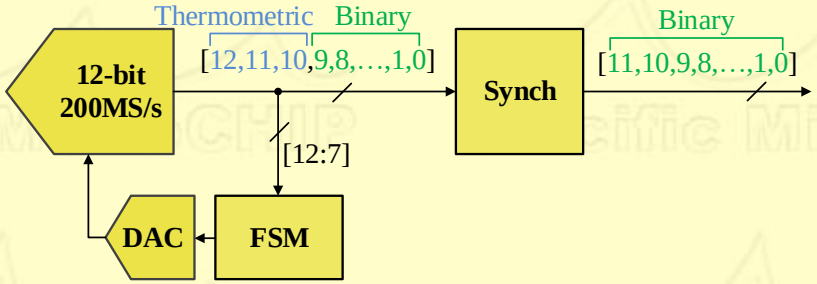
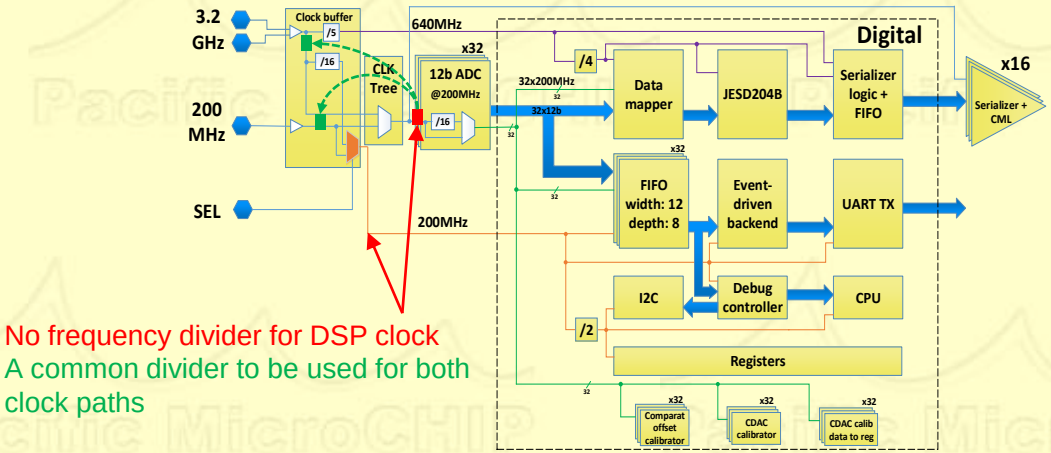
Problem (1st Gen)	Solution (2nd Gen)
Improve the ADC ENOB value	Increased reference voltage, updated comparator design, added CDAC redundancy
Make an offset calibration FSM to account for the 3 MSBs of the ADC output code. 	Dedicated ADC data output for calibration purposes 
An older CPU with a bug was implemented on the ASIC. The bug prevents the CPU from executing the first instruction properly and to read back the program memory through the I2C interface after writing it.	Updated CPU design

MODIFICATIONS DONE FOR THE 2nd GENERATION ASIC

Pacific MicroCHIP Corp.

Problem (1st Gen)	Solution (2nd Gen)
An ADC sampling clock frequency divider is built into the clock distribution network of the ASIC. However, the frequency of the clock going to the DSP is not scaled down proportionally with the divided clock frequency.	 An equivalent frequency divider was added for the digital clock.
DAC feedback loop stability issues (feedback shorted for 2 DACs).	The second modification was to increase the resolution of the DAC from 9bit to 10bit, improve offset cancellation precision by reducing the offset compensation step.

MODIFICATIONS DONE FOR THE 2nd GENERATION ASIC

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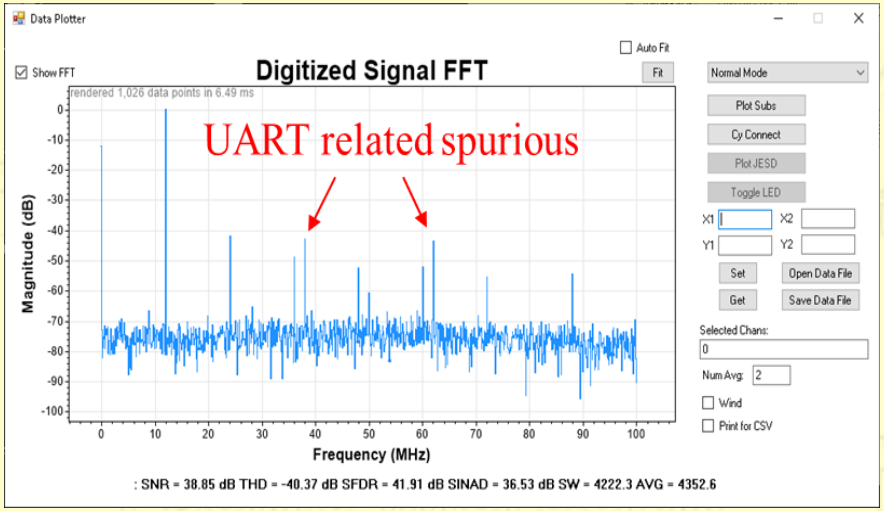
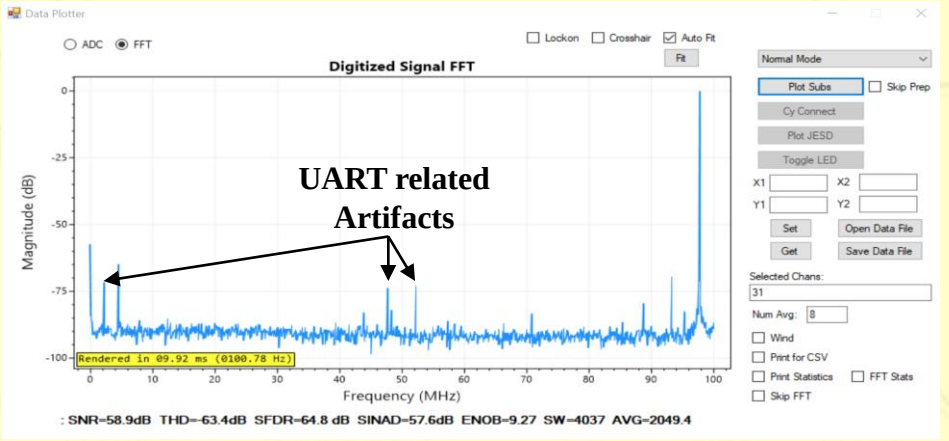
Problem (1st Gen)

It was discovered that two spurs are introduced on the ADC output signal spectrum. These spurs are detected at the input signal frequency ±50MHz (the clock frequency of the UART).

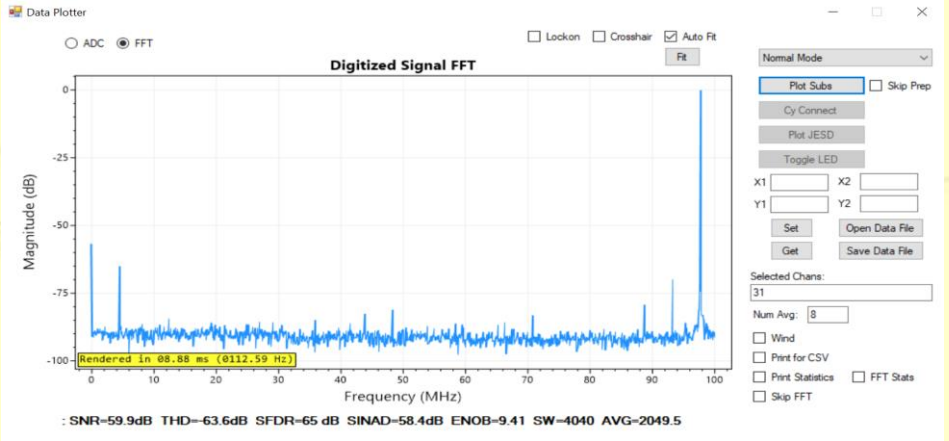


Solution (2nd Gen)

200MHz clock source, UART enabled, UART clock=50MHz



200MHz clock source, UART enabled, UART clock=200MHz



2nd GENERATION CHIP AND ASSEMBLED PART

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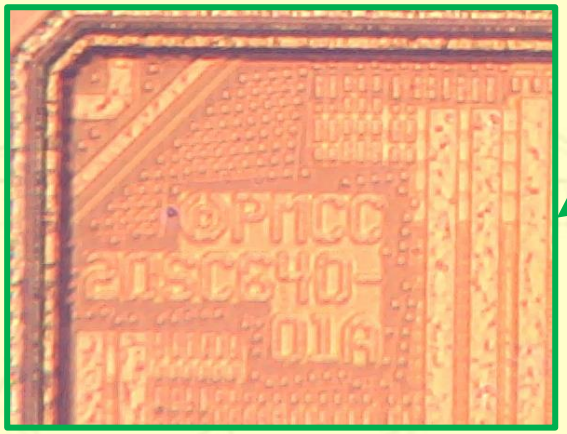
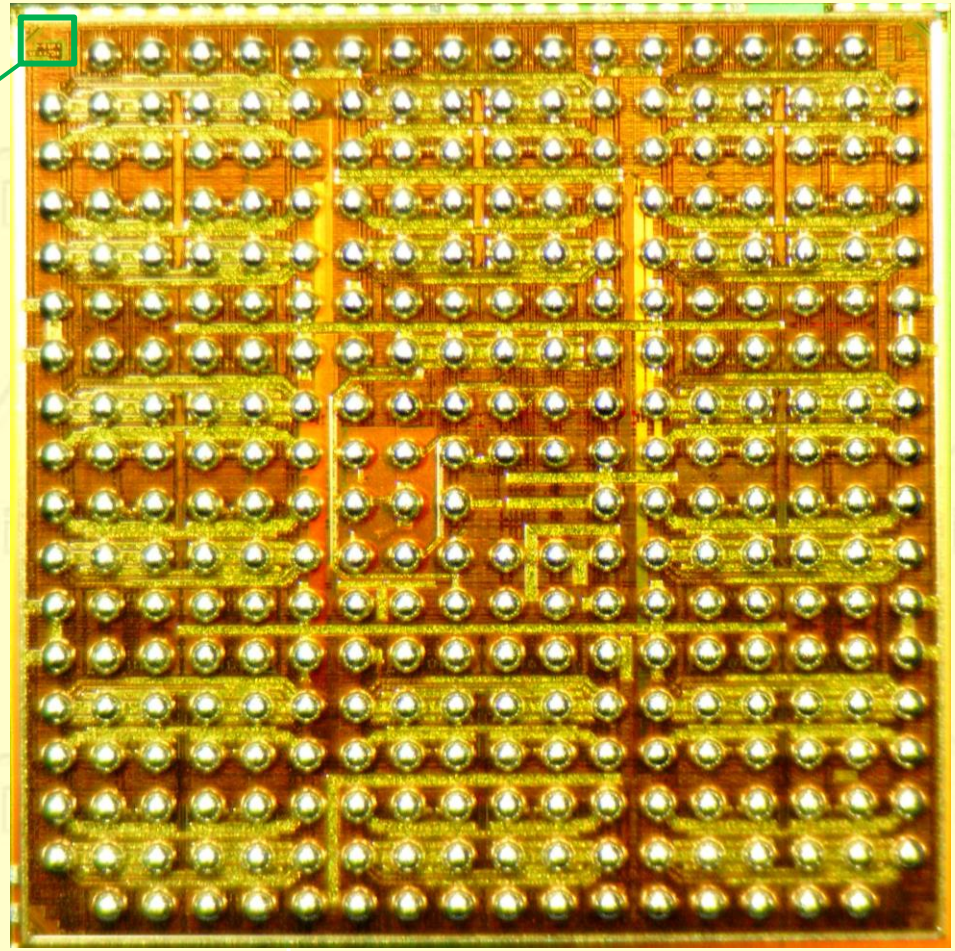
2nd Gen ASIC label @PMCC20SC640-01A



2nd Gen ASIC bumps



P/N: P20640B (P20640A shown since 2nd Gen parts assembling in process)

UPDATED PCB DESIGN

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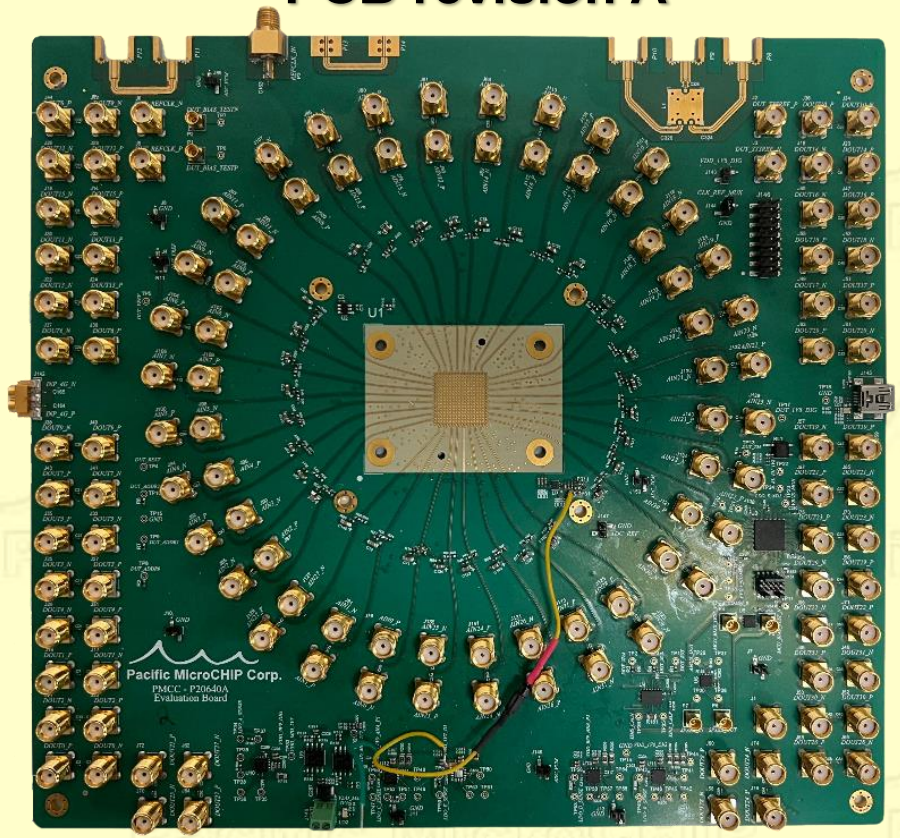
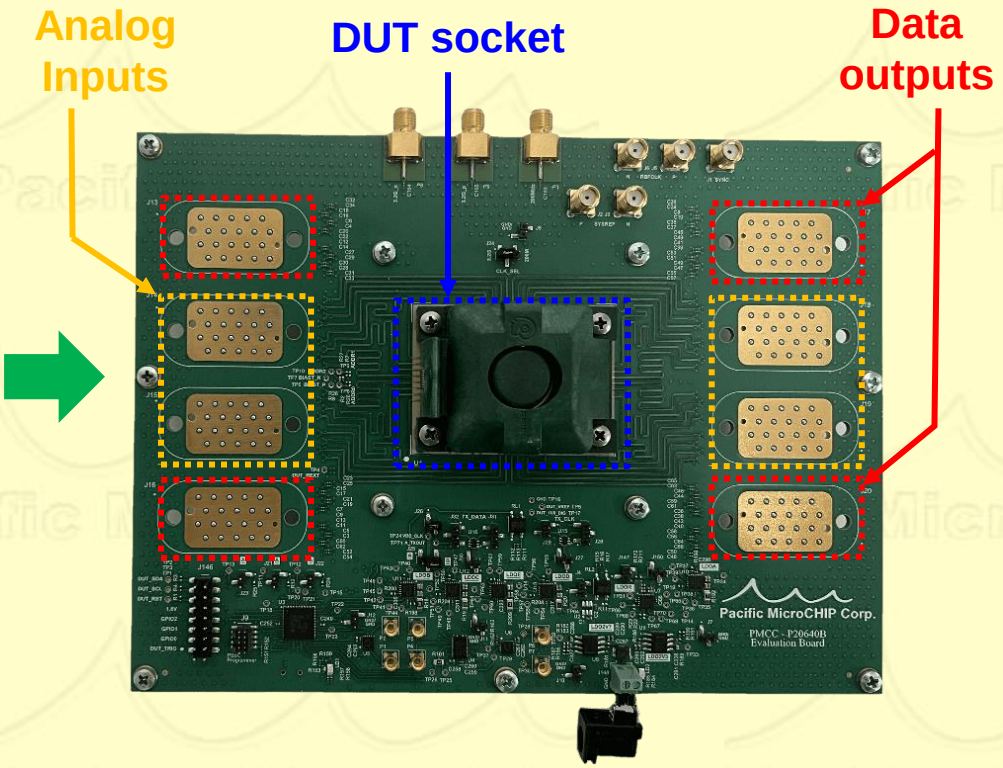
PCB revision A



- SMA connectors used to handle analog input signal / output data
- Dimensions 9.0 x 8.2 inches

PCB revision B



- Samtec's Bulls Eye connectors used to handle analog input signal / output data
- Dimensions 5.6 x 7.7 inches

2nd GEN ASIC TESTBENCH SETUP

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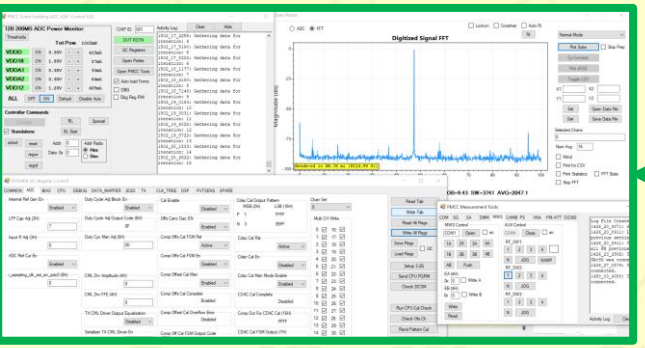
Signal generator

Test PCB

Clock source
200MHz and 3.2GHz

GUI



Power supply

ADC LAYOUT COMPARISON

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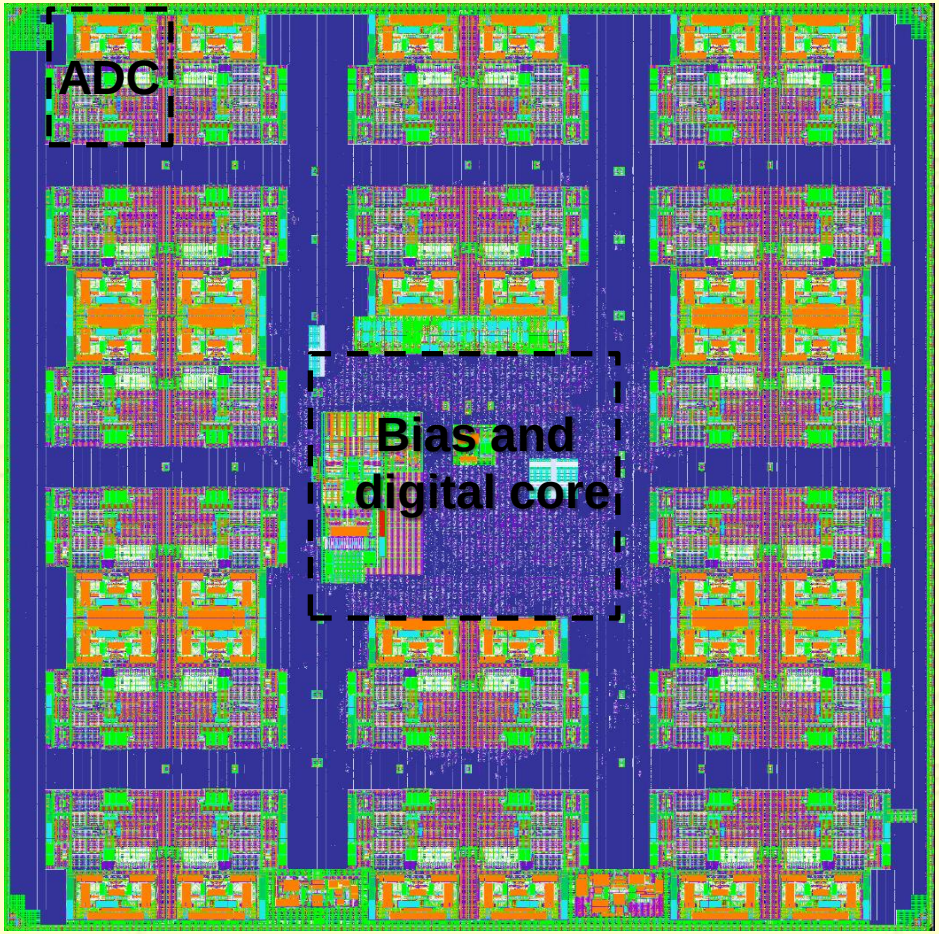
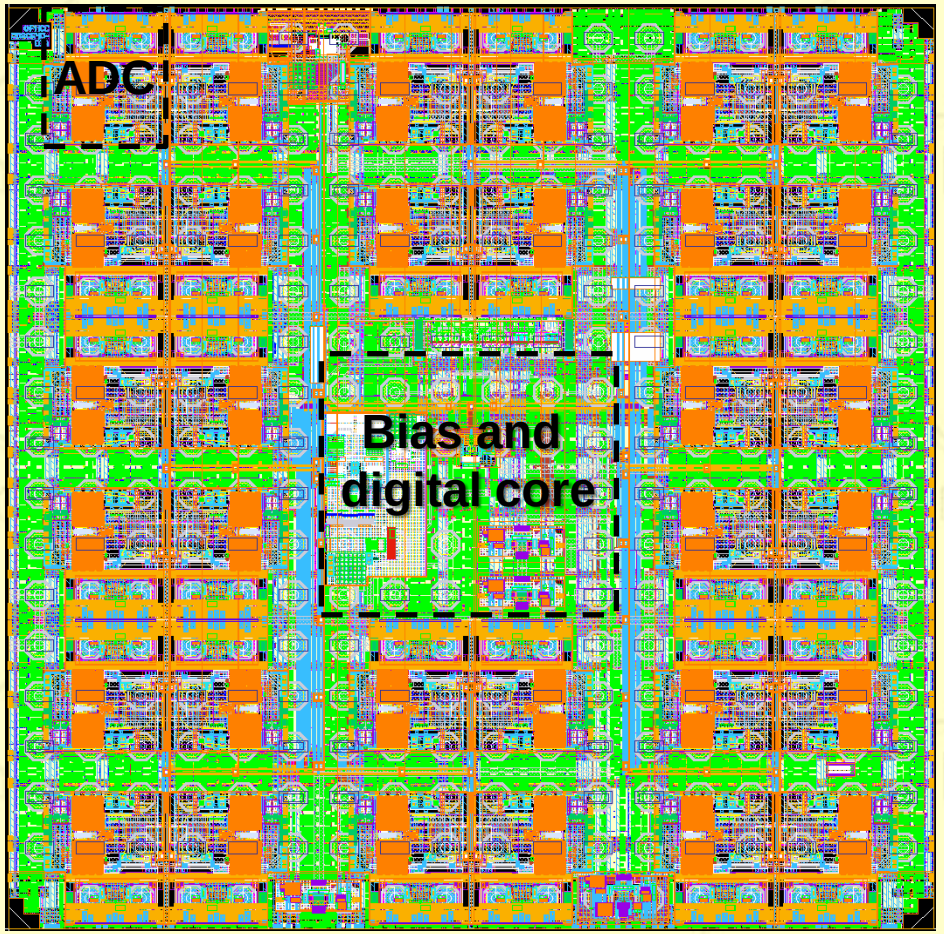
1st Gen ASIC top level layout:



2nd Gen ASIC top level layout:



ADC TESTING RESULTS
PERFORMANCE COMPARISON

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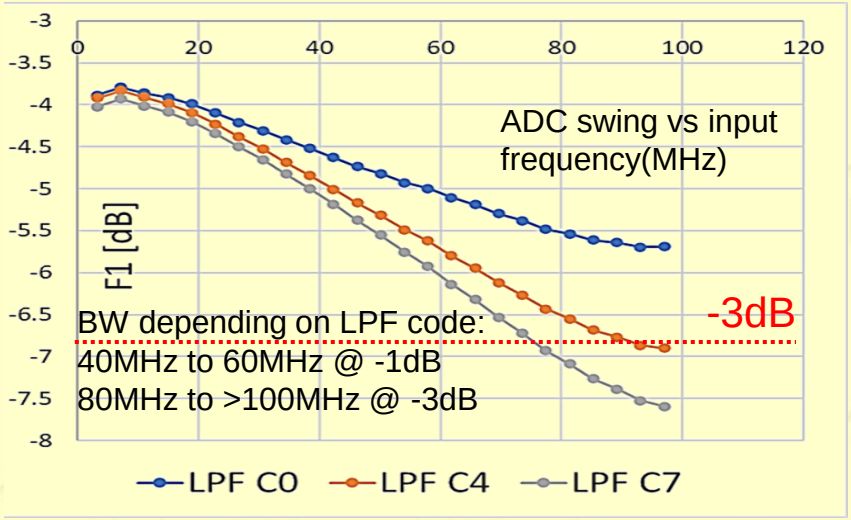
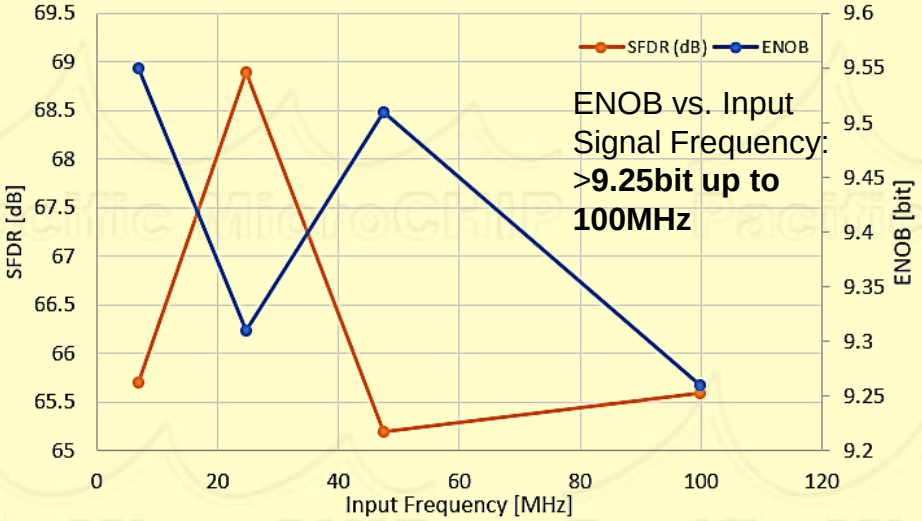
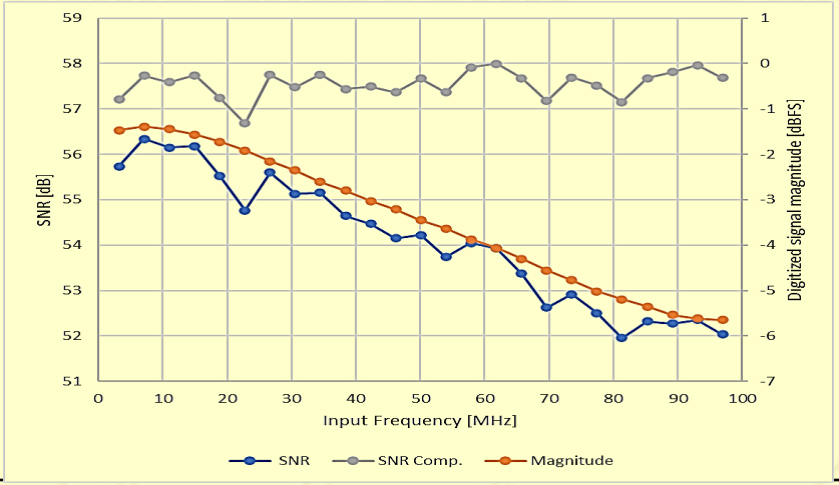
1st Gen ASIC



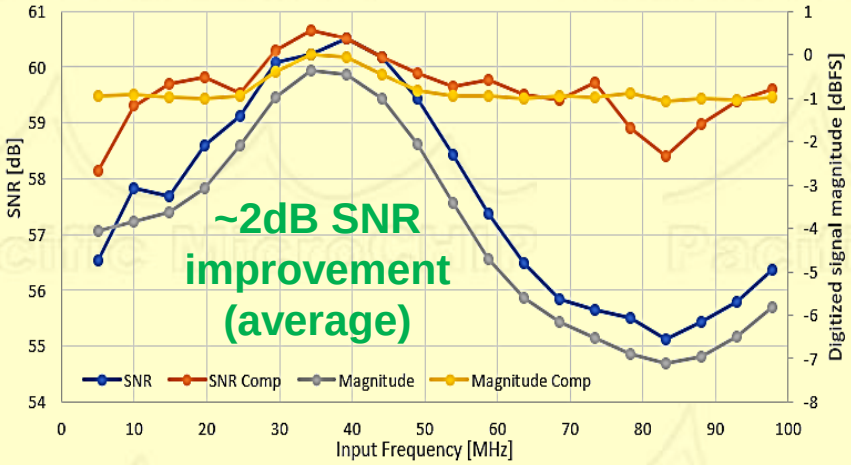
2nd Gen ASIC:



SNR vs. Input Signal Frequency: **>56.5dB up to 100MHz**



SNR vs. Input Signal Frequency: **>58dB up to 100MHz**



ADC POWER CONSUMPTION

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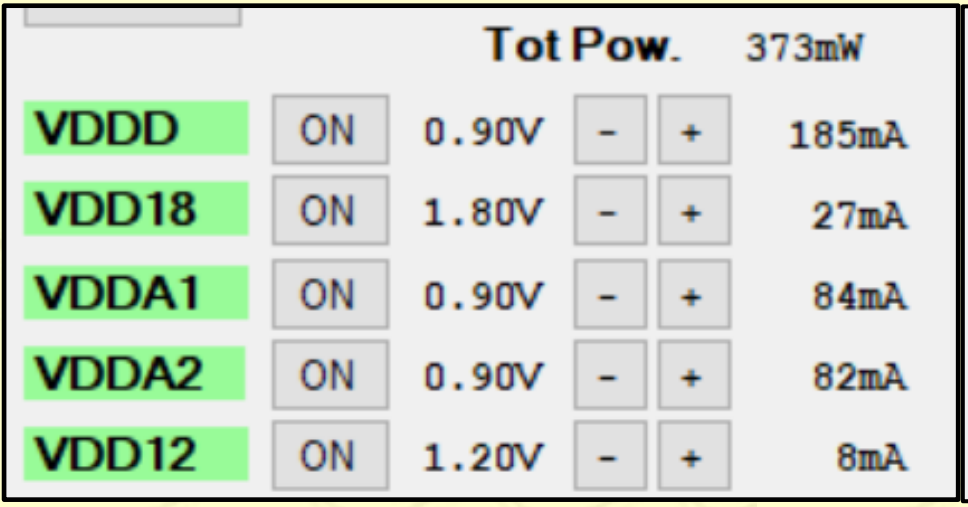
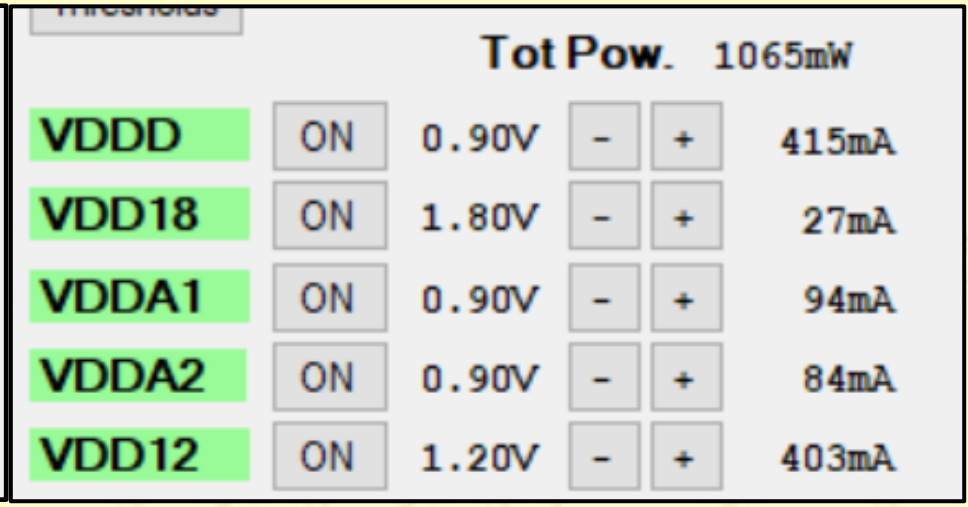
32 ADC channels enabled
JESD204 output data interface **disabled**



Average power **11.7mW / ch**

32 ADC channels enabled
JESD204 output data interface **enabled**

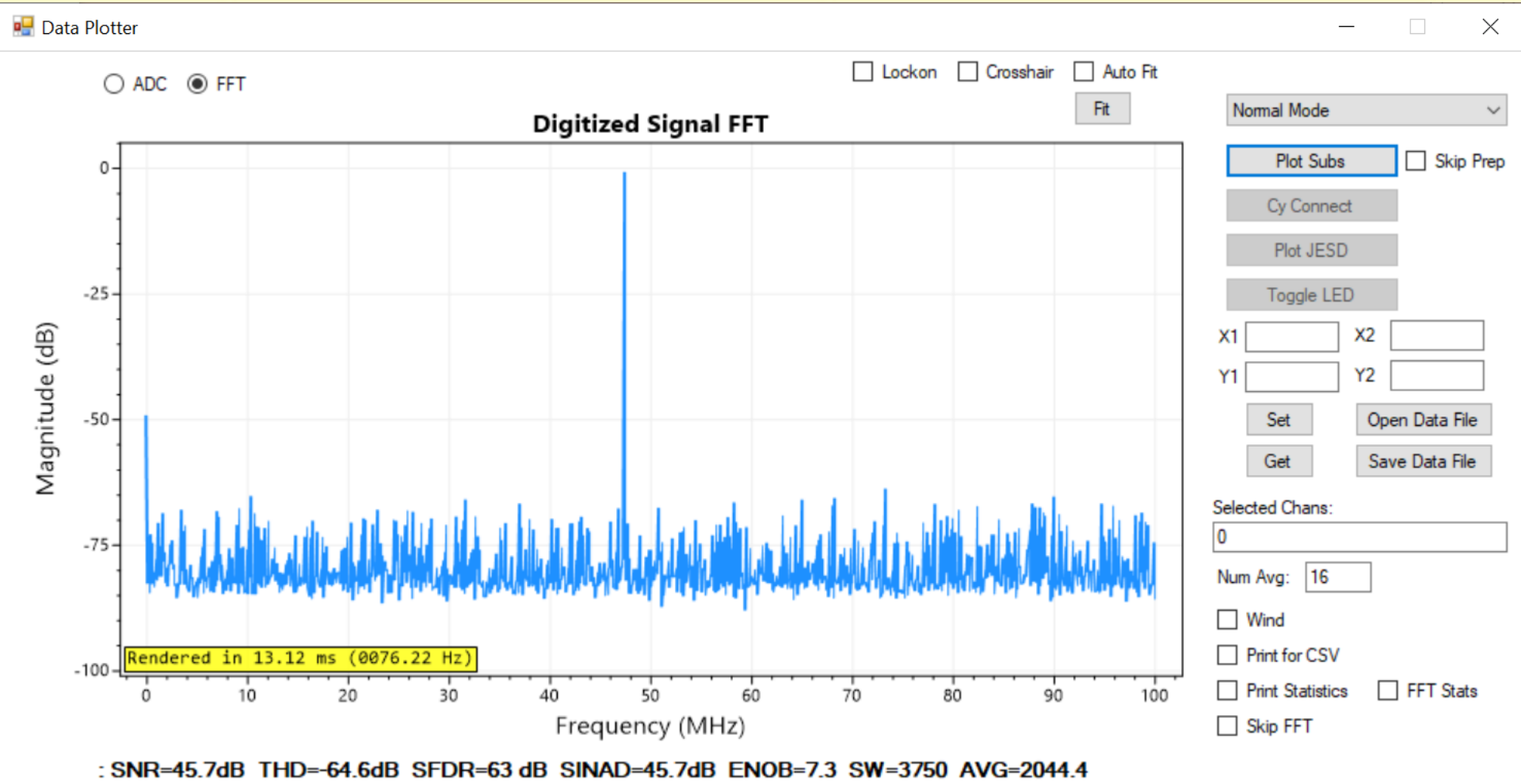


Average power **33.3mW / ch**

TESTING RESULTS:
ADC OUTPUT SPECTRUM CH #0

Pacific MicroCHIP Corp.

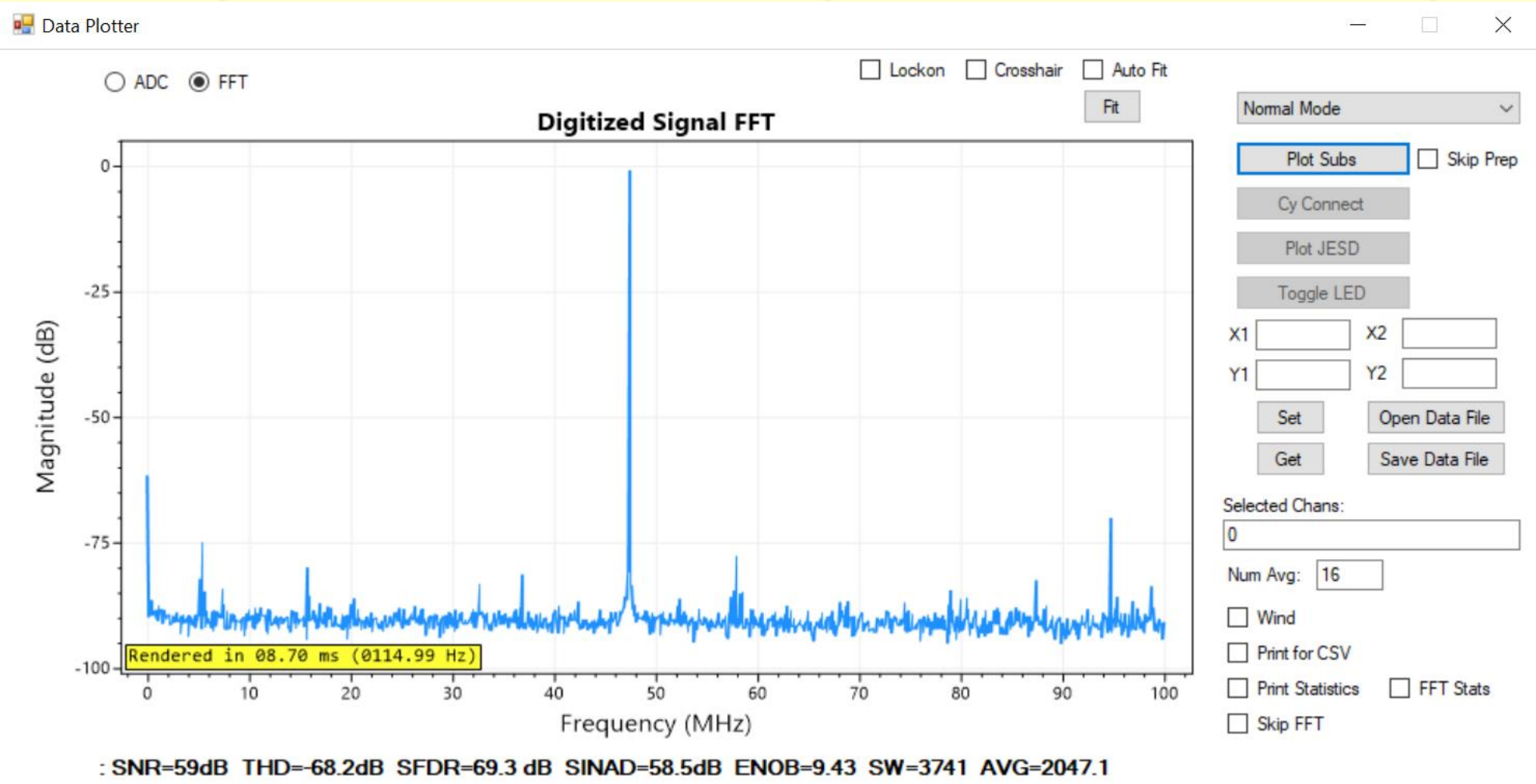
Channel #0 <u>before calibration</u>: SFDR 63dB / ENOB 7.3 / SNR 45.7dB



TESTING RESULTS:
ADC OUTPUT SPECTRUM CH #0

Pacific MicroCHIP Corp.

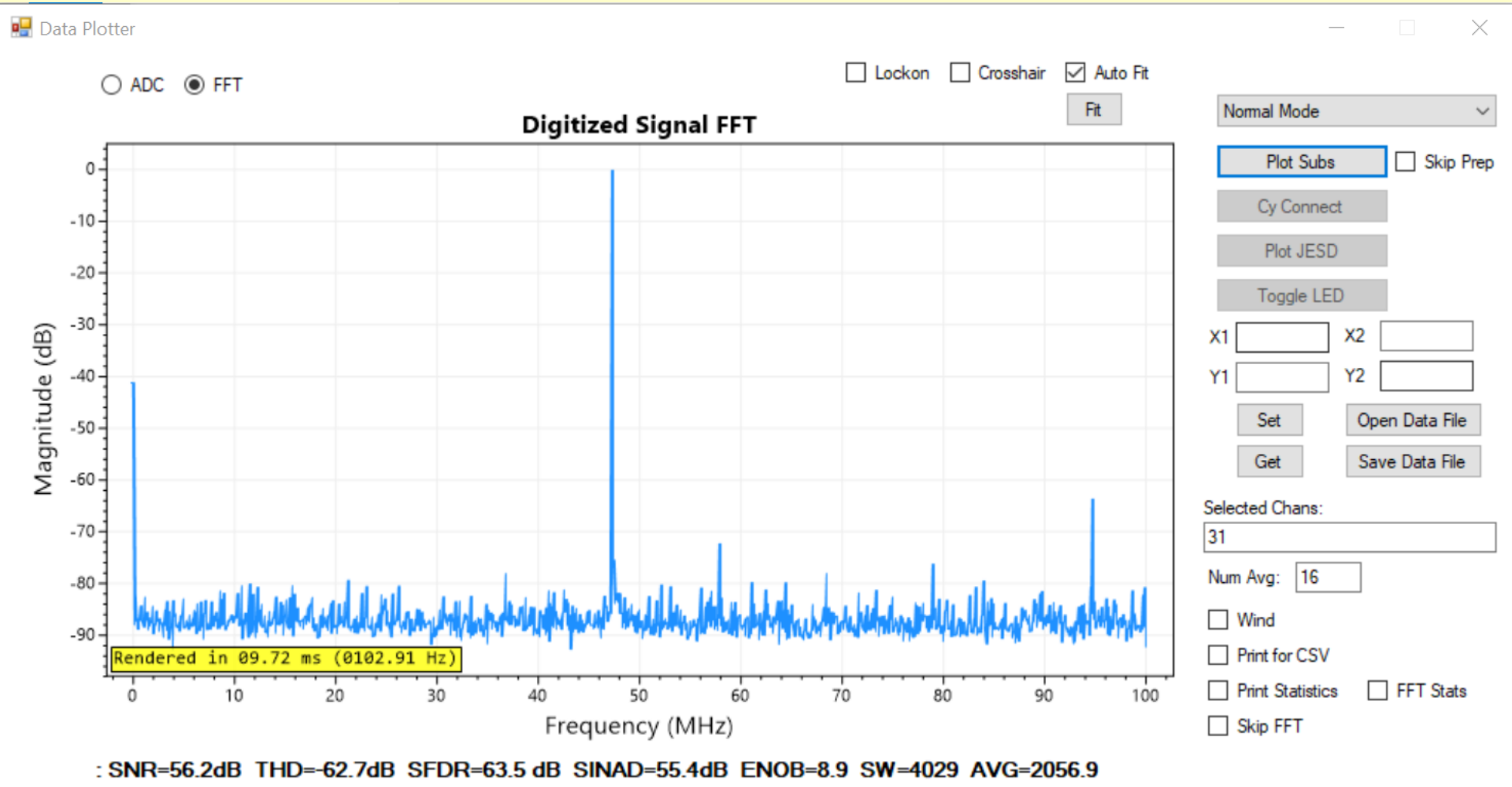
Channel #0 <u>after calibration</u>: SFDR 69.3dB / ENOB 9.43 / SNR 59dB



TESTING RESULTS:
ADC OUTPUT SPECTRUM CH #31

Pacific MicroCHIP Corp.

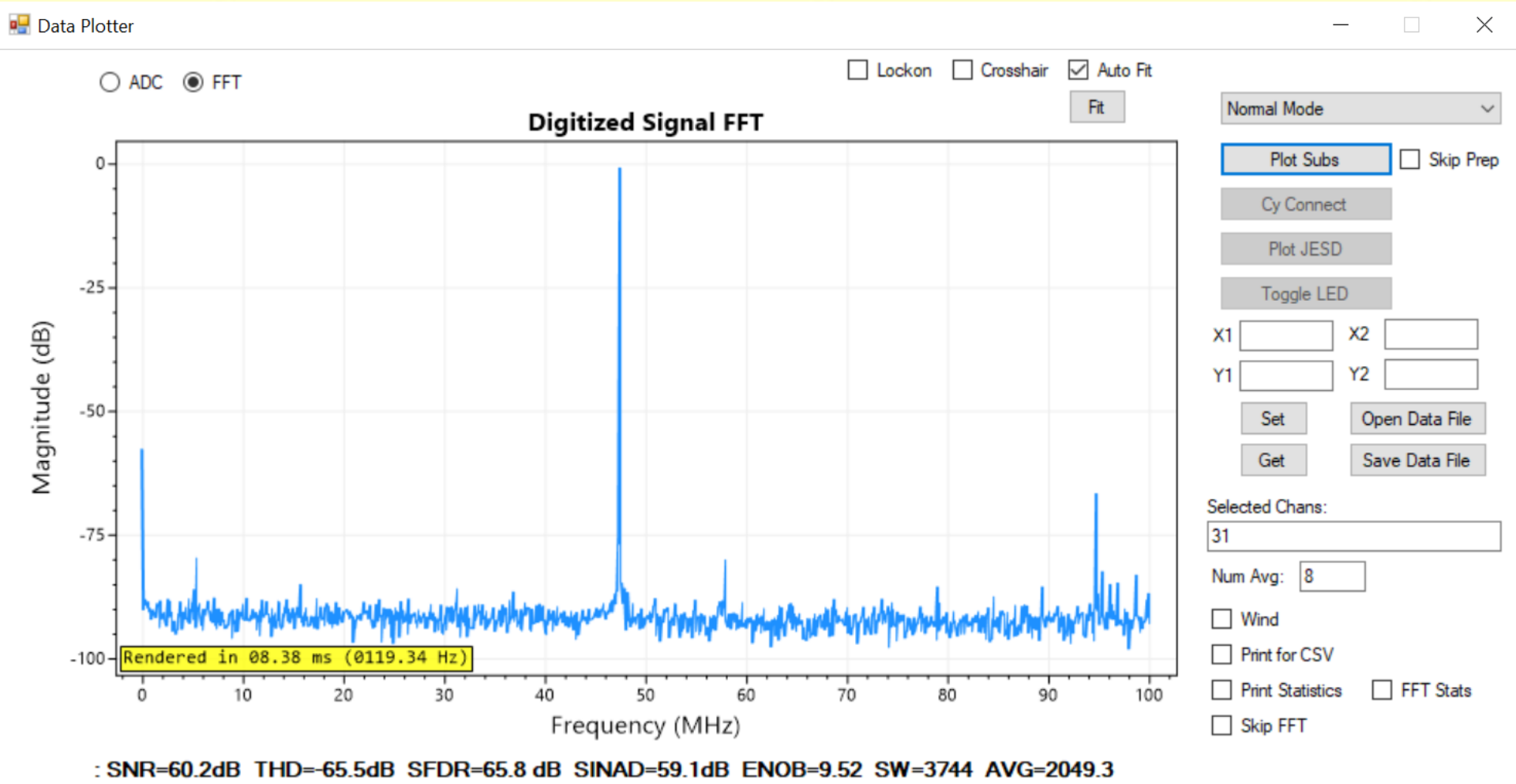
Channel #31 <u>before calibration</u>: SFDR 63.5dB / ENOB 8.9 / SNR 56.2dB



TESTING RESULTS:
ADC OUTPUT SPECTRUM CH #31

Pacific MicroCHIP Corp.

Channel #31 <u>after calibration</u>: SFDR 65.8dB / ENOB 9.52 / SNR 60.2dB



TESTING RESULTS:
ADC PERFORNACE SUMMARY

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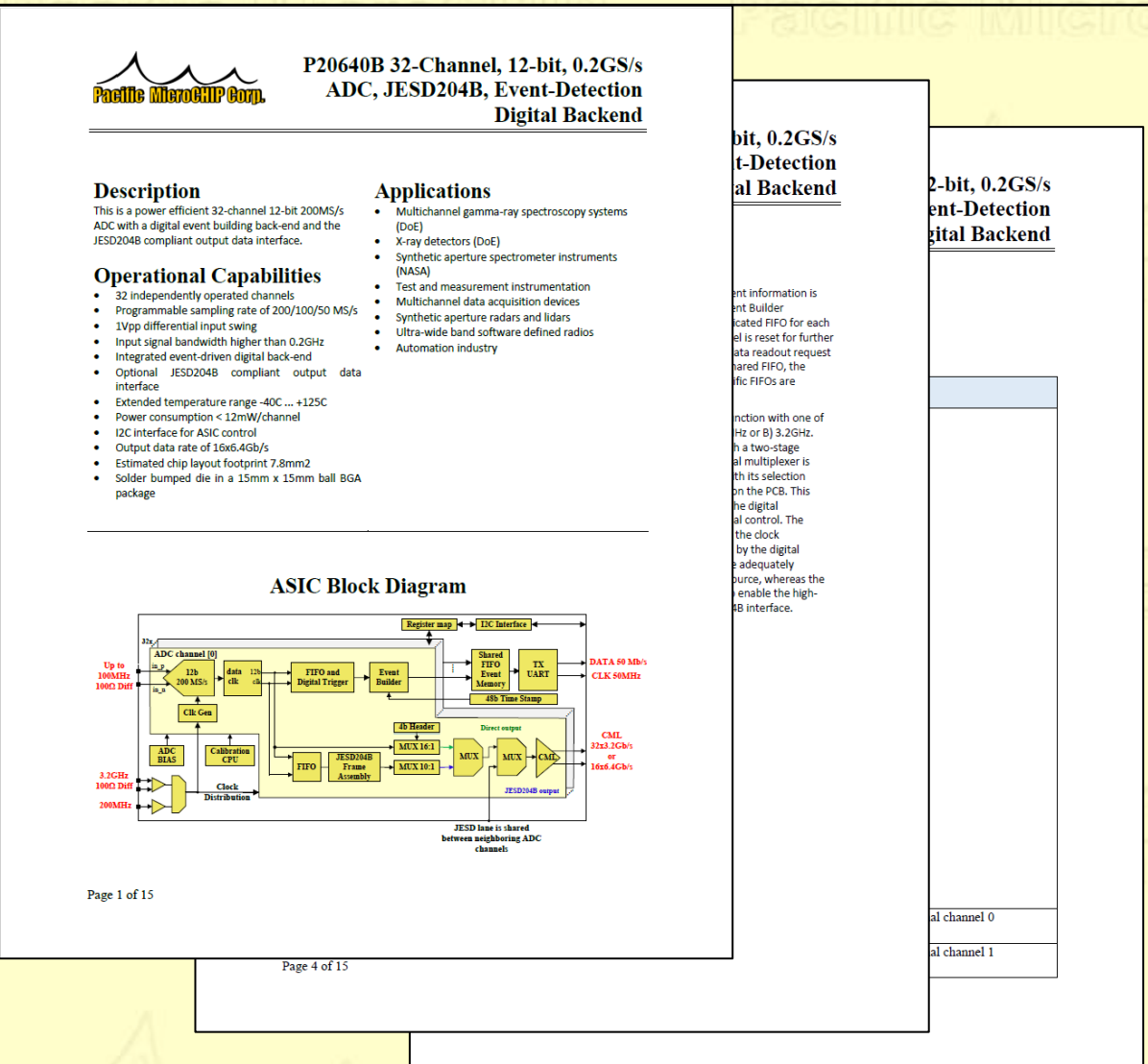
CHANNEL	CALIBRATION CODES						ADC PERFORMANCE			
NUMBER	CMP 1 ofs	CMP 2 ofs	CDAC C14	CDAC C15	CDAC C16	CDAC C17	SNR (dB)	SFDR (dB)	SINAD (dB)	ENOB (Bit)
0	144	20E	2E	2C	32	2F	59.5	67.5	58.7	9.45
1	164	1D3	2D	2D	35	33	58.7	70.7	58.4	9.41
2	1B7	1DB	2F	2D	35	35	60	67.3	58.9	9.5
3	19B	1D0	2B	27	2F	2D	57.9	72.4	57.6	9.28
4	15B	20A	2D	2B	37	37	59.7	67.7	59	9.51
5	144	22D	2F	2D	31	35	60.2	66.2	59.2	9.54
6	195	23C	30	2F	43	43	59.8	66.8	58.6	9.44
7	15A	201	2D	2D	35	31	59.4	65.5	58.4	9.4
8	14A	1BA	2F	2F	35	31	59.5	68.3	58.9	9.49
9	1B8	218	36	34	38	40	56.4	74.2	56.2	9.04
10	161	1B2	2B	27	2B	2D	59.7	67	58.4	9.42
11	15D	22C	2B	23	2B	2B	57.8	68.1	57.2	9.21
12	155	23B	2D	2B	37	33	60.4	67.7	59.5	9.59
13	1C6	236	2F	35	47	45	57.2	66.7	56.6	9.1
14	181	203	2B	25	2F	2F	59.1	67.8	58.4	9.41
15	1A0	1F3	30	31	37	33	56.9	71.1	56.6	9.12
16	192	1D3	30	34	45	43	58.8	62.7	57.3	9.22
17	142	205	2D	2B	33	33	59	70.3	58.6	9.44
18	162	216	2F	2F	35	35	60.4	66.9	59.2	9.54
19	145	203	2D	25	2D	2D	59.9	67.6	59.1	9.52
20	191	1B5	2D	2F	43	41	59.5	67.4	58.7	9.46
21	1A6	1E4'	2D	25	33	31	59	70.9	58.5	9.43
22	204	20E	31	37	45	47	60.7	67	59.3	9.55
23	147	20B	2D	25	2F	2F	58.8	67	58	9.35
24	1B8	205	2F	2F	41	35	59	66.2	58.2	9.37
25	1A5	202	2E	2E	35	33	61.1	66.6	59.9	9.67
26	182	203	32	33	43	43	59.9	66	58.9	9.5
27	192	1E1'	2B	27	2F	2D	59.6	67.5	58.9	9.49
28	186	1C3	2D	27	2B	2B	60.8	67	59.7	9.62
29	183	21E	2D	27	2D	2B	60.5	66.5	59.3	9.55
30	183	205	33	37	49	49	60.3	65.9	58.6	9.44
31	153	1E3'	2F	31	37	37	61.3	66.9	60.1	9.7

ASIC DATASHEET

Pacific MicroCHIP Corp.



Pacific MicroCHIP Corp.

P20640B 32-Channel, 12-bit, 0.2GS/s ADC, JESD204B, Event-Detection Digital Backend

Description

This is a power efficient 32-channel 12-bit 200MS/s ADC with a digital event building back-end and the JESD204B compliant output data interface.

Operational Capabilities

- 32 independently operated channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input swing
- Input signal bandwidth higher than 0.2GHz
- Integrated event-driven digital back-end
- Optional JESD204B compliant output data interface
- Extended temperature range -40C ... +125C
- Power consumption < 12mW/channel
- I2C interface for ASIC control
- Output data rate of 16x6.4Gb/s
- Estimated chip layout footprint 7.8mm2
- Solder bumped die in a 15mm x 15mm ball BGA package

Applications

- Multichannel gamma-ray spectroscopy systems (DoE)
- X-ray detectors (DoE)
- Synthetic aperture spectrometer instruments (NASA)
- Test and measurement instrumentation
- Multichannel data acquisition devices
- Synthetic aperture radars and lidars
- Ultra-wide band software defined radios
- Automation industry

ASIC Block Diagram

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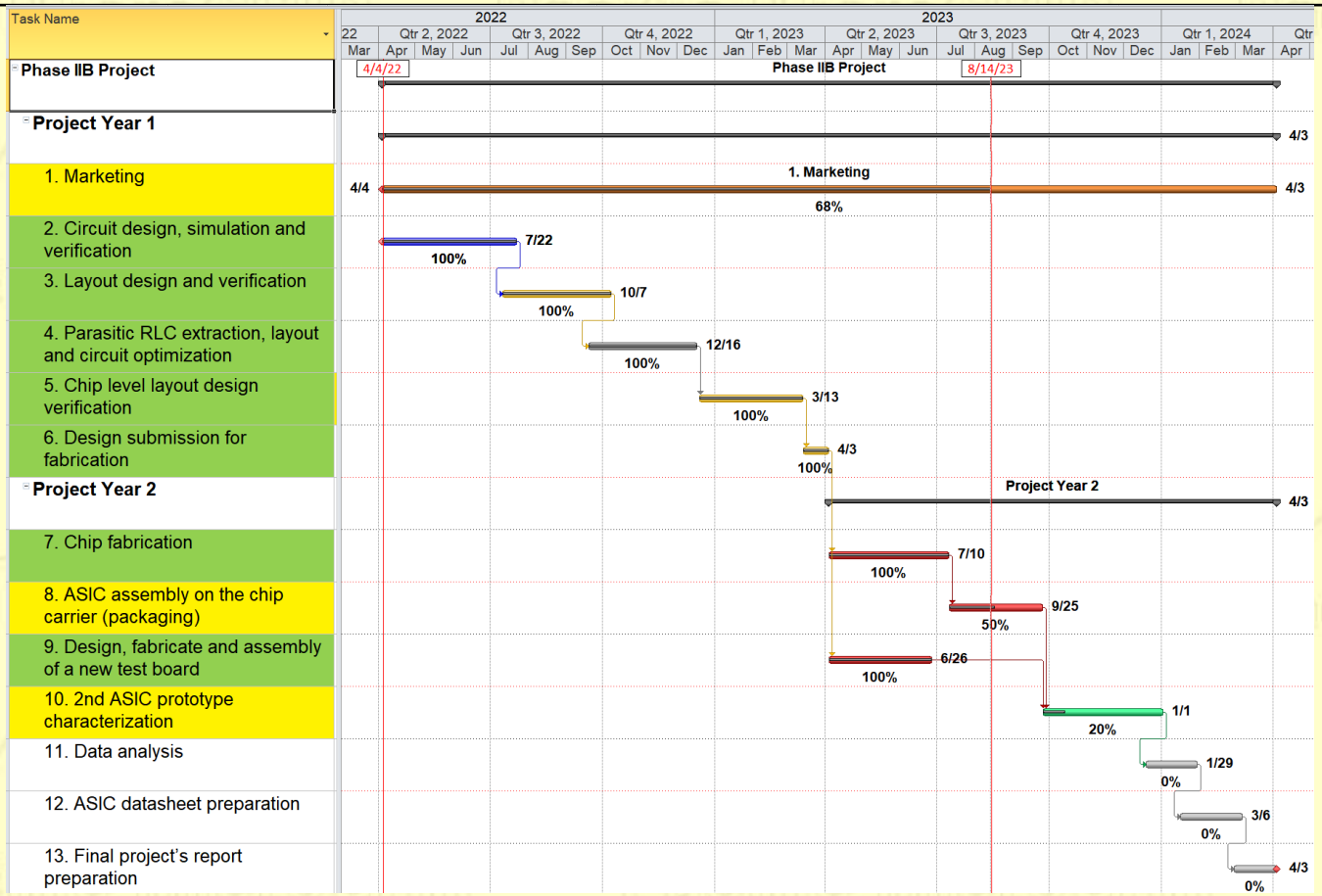
We are in the process of drafting the datasheet for the designed ASIC, which will encompass a comprehensive overview of the ASIC's functionalities, detailed specifications, and recommended setup and calibration procedures.

Anticipate the initial draft to be prepared in September 2023.

PHASE IIB PROJECT SCHEDULE



We are slightly ahead of schedule because we were able to assemble a few parts manually in our lab and start characterization. The project is expected to be completed as planned on March 4, 2024.

FUTURE PLANS

- Test/characterize the produced 2nd Gen ASIC.
- Create ASIC datasheet
- Start shipping the ASIC parts to select customers.

THANK YOU!

Application Ideas for the ADC ASIC are appreciated!