

Low Cost, High-Density Digital Electronics for Nuclear Physics

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- The company and its capabilities.
 - Customers.
- Our products:
 - Digitizers from two up to forty channels.
 - Logic module supporting up to 16 digitizers, total 512 channels.
- Firmware and software.
 - Improved firmware structure (backup slide).
 - Portable remote Web GUI.
- Selected examples of applications of our electronics.
- Manufacturing problems due to the supply chain disruptions.
 - Crucial electronic parts are hardly available.
- Future plans.
- Acknowledgements.

The team:

- Three physicists / engineers, a senior software engineer, and a manager. We regularly work with a local EE consultant.
- We worked with several interns mentioned on the Acknowledgements page.

Our focus:

Digital data acquisition (DAQ) for nuclear physics, high energy physics, astrophysics, etc.

Our capabilities: Development of cutting edge instruments.

- Electronic design.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors, especially Embedded Linux.
- Algorithms for pulse processing.
- Algorithm implementation in FPGAs (VHDL, Verilog) and in embedded processors (Pascal, Python, C).
- Processing data from nuclear detectors of any kind.
- Development of simple detector assemblies using scintillators, PMTs, or SiPMs.



Hardware

Our digitizers, from 2 up to 32 channels

We developed both large (32+ channels) and small digitizers with 2 and 10 channels.

All our units are running Linux inside and use FPGAs for signal processing.



- The pre-prototypes were extensively tested. We are ready for production.
- *The production is on hold because of the electronic part crisis.*
- Remote Web GUI has been developed (next section).

80 μ s waveforms

50 ms waveforms



Previous FemtoDAQ
with BeagleBone



To be retired??

SiPM bias generator
+5V to +90V
in 1.4 mV steps

Logic I/O
coax

Two outputs:
arbitrary wave
generators



Logic I/O, 8 pins

Two inputs: 50 Ω , 1k Ω , 10k Ω
14 or 16 bits, 100 MSPS
Design is ready for 250 MSPS

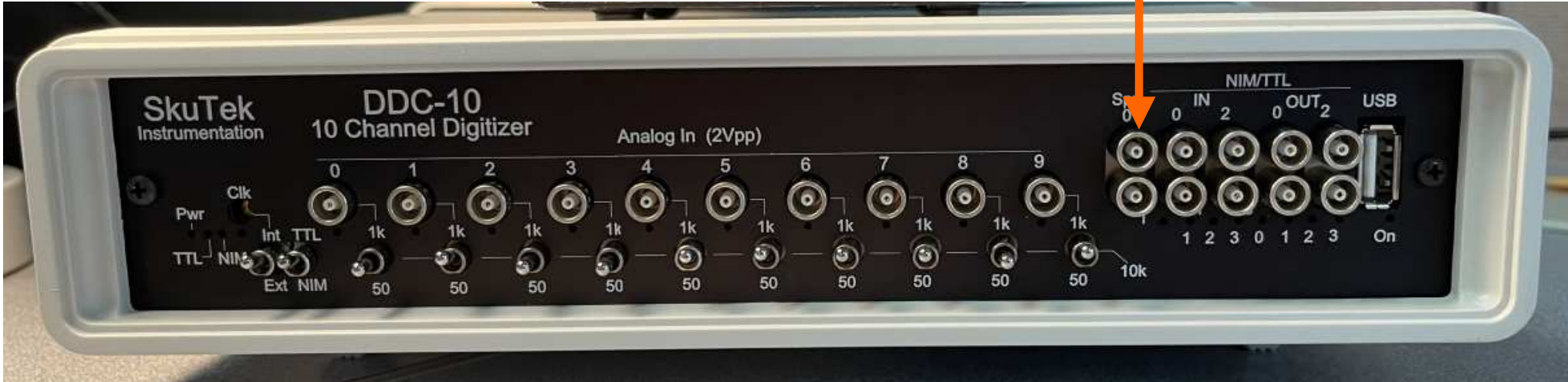
10-Channel DDC-10 (New Edition)

- We delivered the units to Univ. of Maryland, Brown University, and Brookhaven National Laboratory.
- We are ready for production, but...The production is on hold because of the electronic part crisis.

80 μ s waveforms

SiPM bias output in the back
+5V to +90V
in 1.4 mV steps

Two analog outputs:
arbitrary wave generators



Ten analog inputs: 50 Ω , 1 k Ω , 10 k Ω
14 bits, 100 MSPS
Design is ready for 250 MSPS

Four logic inputs
Four logic outputs
Can be switched NIM / TTL

Linux inside



- We are ready for production. The production is on hold because of the **electronic part crisis**.
- We are using the prototypes to develop 10 Gbps streaming readout in collaboration with ANL.



- Thirty two ADC inputs
 - 50 Ω or 1 k Ω , 2 Volt range
 - LEMO coax input
 - 14 bits, 100 MSPS
- Optional external ADC sampling clock
- All logic IO's can be switched between NIM or LVTTTL
- Four logic inputs defined in firmware
 - Default firmware: time stamp reset, veto acquisition
- Four logic outputs defined in firmware
 - Default firmware: trigger out, busy out
- Pulse integration and pulse height measurement in firmware
- **1 Gbps** (copper) UDP streaming from the FPGA (upper RJ-45)
 - Up to ~110 Mbyte/s directly to Data Concentrator computer
- Fast Ethernet access to **on-board Linux** (lower RJ-45)
 - A few tens of Mbyte/s depending on software application
- Optional **streaming** to dedicated logic over HDMI connector

Linux inside

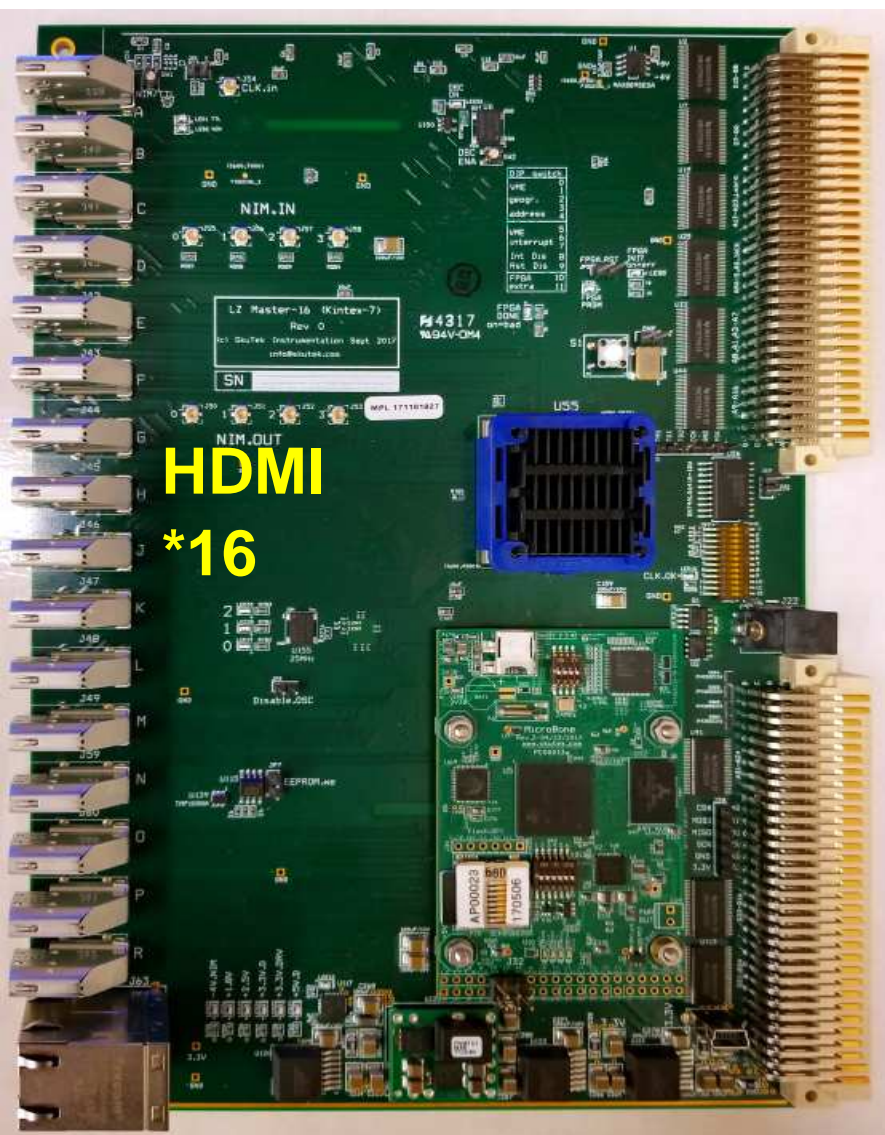
Prototype Digitizer with 40 Channels

We made two such units. The 32-channel digitizer was derived from this one



- 40 ADC channels: **Linux inside**
 - 100 MHz sampling rate
 - ADC chip resolution: 12, 14, or 16 bits
 - 2V input range
 - +/-1V adjustable baseline
- Kintex-7 Xilinx FPGA, two options:
 - XC7K325T: BRAM=1,780 kB (**228 μ s/chan**)
 - XC7K410T: BRAM=3,180 kB (**407 μ s/chan**)
- Temperature, voltage, current monitoring
- Embedded Linux Module with Ethernet, USB-2, and RS-232
- Remotely programmable:
 - Both the FPGA and the Linux Module
 - Internal FPGA signals can be remotely accessed over Internet.

Two dozens are serving as Trigger Builders for LUX-Zeplin DAQ



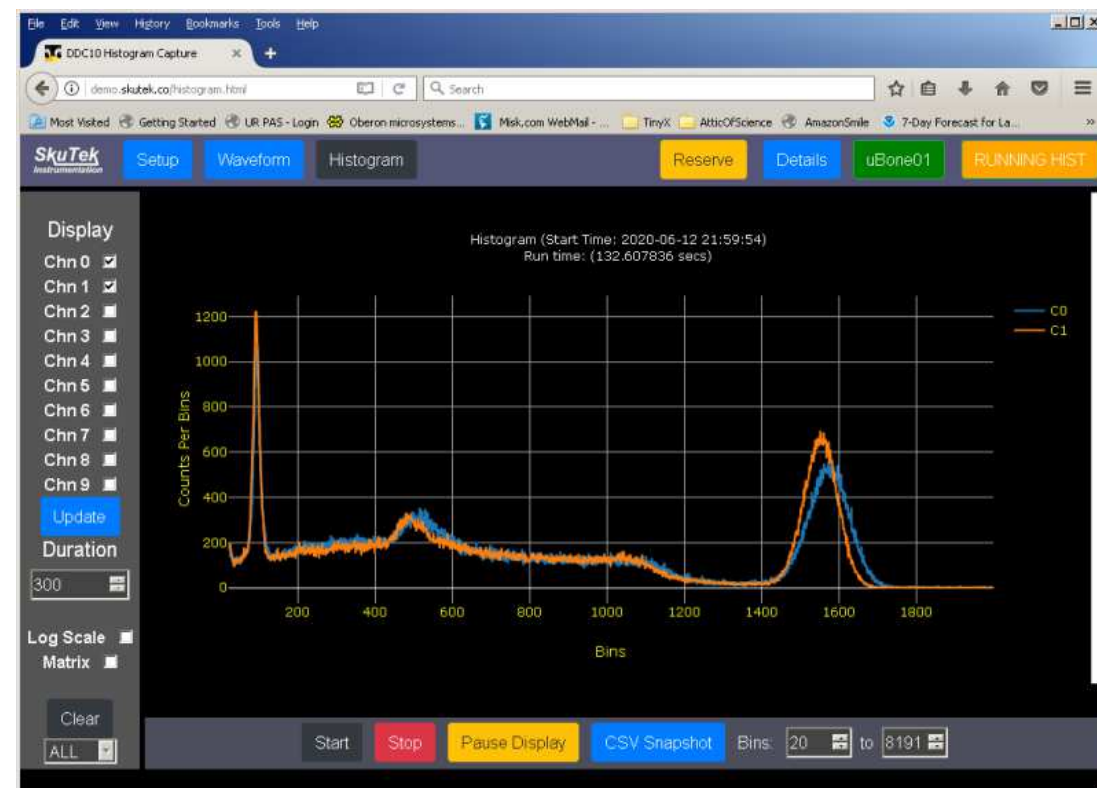
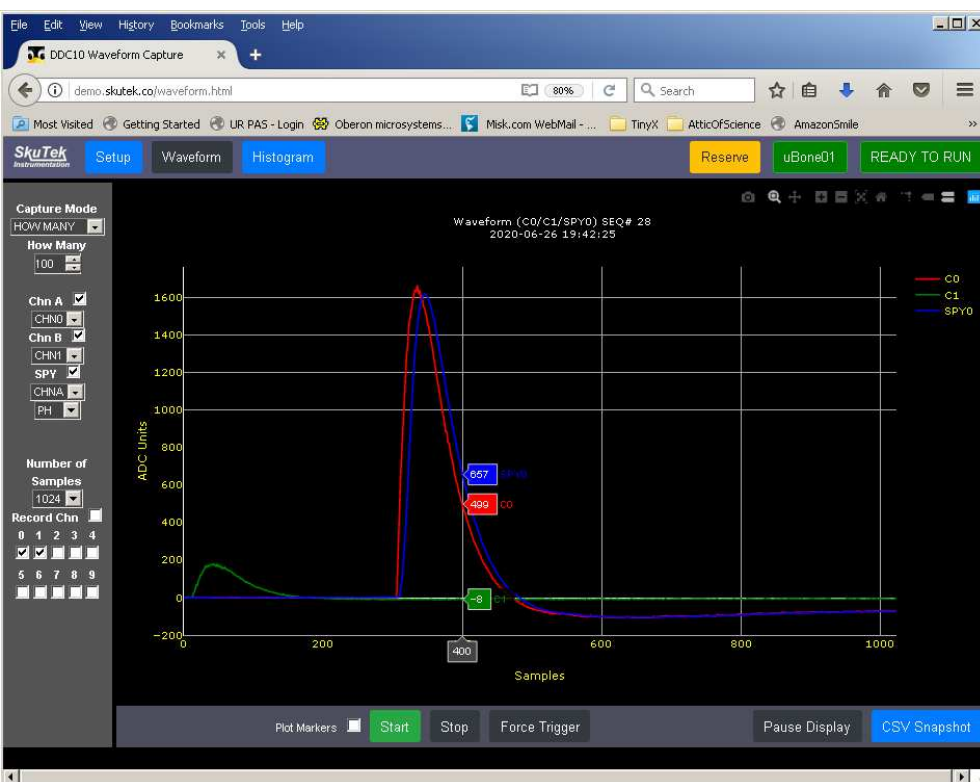
- 16 Fast Serial Links use HDMI cabling
 - Up to ~4 Gbps per connector
- One unit can serve up to $16 \times 32 = 512$ channels
- ADC sampling clock distribution to digitizers
- Kintex-7 Xilinx FPGA, two options:
- XC7K325T (1,780 kB) or XC7K410T (3,180 kB)
- Dual height gigabit RJ-45 (two sockets)
 - 1 Gbps UDP streaming
 - Ethernet access to on-board Linux
- On-board Debian Linux
- Two modes of operations (both used in LZ)
 - Mode 1: Data readout serving up to 16 digitizers
 - Mode 2: Trigger generation for up to 512 channels

Linux inside



Software

- The waveform and histogram displays can be shown in **any browser, any operating system**.
- One can even use **a cell phone**. Not really encouraged, but it works.
- The GUI does **not** require **any software installation** on the remote host. It runs in the browser.
- **Multiple users** can connect to the same instrument.
- We use a “virtual sticky note” to warn against access conflicts.
- In addition to the web GUI, we also offer a C function library and a set of command-line utilities.



Example Applications

By Eryk Druszkiewicz & Dev Ashish Khaitan, University of Rochester, Dept of Physics and Astronomy, Rochester, NY - 14627 (private communication on Aug/12/2022).

DDC-10 digitizers were used for testing different components of the **LUX-ZEPLIN (LZ)** experiment.

- **Brookhaven National Laboratory**, Dr. Minfang Yeh: Developed a DDC-10 and PMT setup to test Gadolinium doped liquid scintillator during production and delivery at LZ.
- **Brandeis University**, Prof. Bjoern Penning: Used a DDC-10 to prototype and QA PMT's delivered for the LZ Outer Detector system.
- **SUNY Albany**, Prof. Matthew Szydagis: Implemented a DDC-10 to record PMT and SiPM signals from Xenon Bubble Chamber.
- **University of California at Davis**, Prof. Many Tripathi: Used a DDC-10 to QA amplifier boards for LZ. Developed custom firmware on the DDC-10 to use with their xenon detector called MiX.
- **University of California at Santa Barbara**, Prof. Harry Nelson: Used a DDC-10 to record PMT signals and carry out digital signal processing to assay Gadolinium doped liquid scintillator for LZ. Used this DDC-10 to develop a low-energy tagged neutron source.
- **University of Maryland**, Profs. Carter Hall and Anwar Bhatti: Used a DDC-10 to test chromatographic separation of impurities from Xe and to test the tritium injection system for LZ.

Radioassay of gadolinium-loaded liquid scintillator for the LUX-Zeplin Outer Detector, using DDC-10

Scott Haselschwardt et al, UC Santa Barbara and Lawrence Berkeley Laboratory
NIMA, Volume 937, 1 September 2019, Pages 148-163

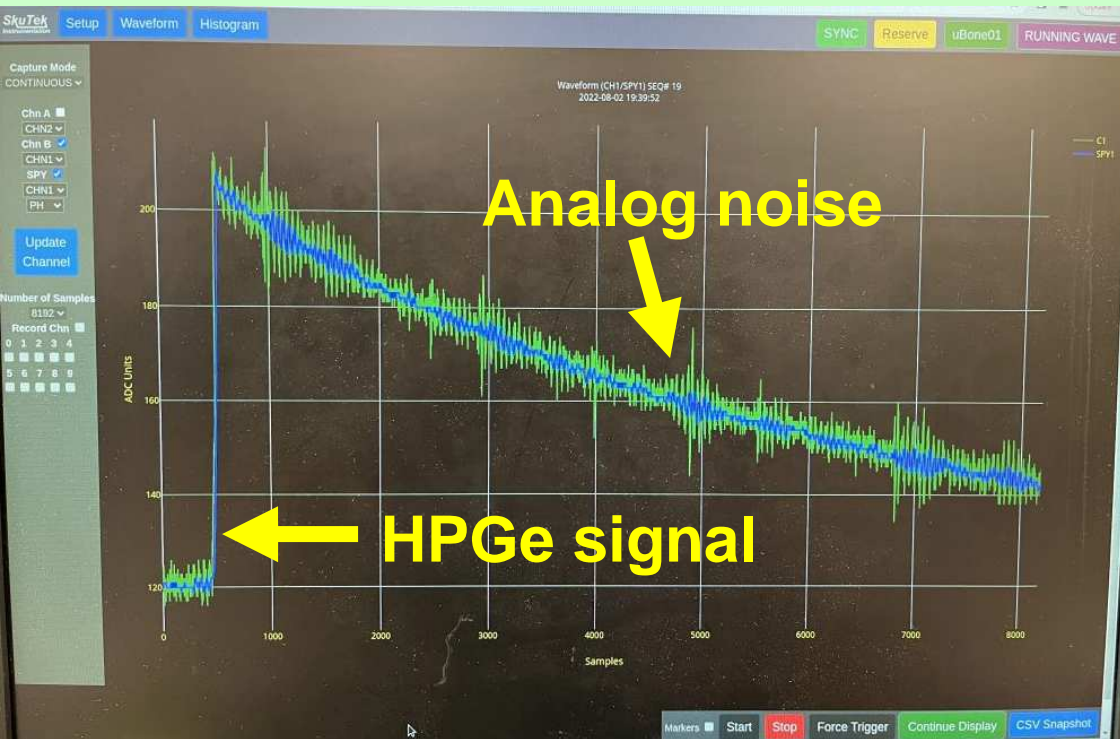
- **The goal:** Measure extremely low activity of the liquid Gd-loaded scintillator to be used in the outer shield of the LUX-Zeplin Dark Matter detector.
- **DDC-10** was used to record the signals from the LUX-Zeplin (LZ) “Screener”, consisting of 23 kg of LAB-based gadolinium-loaded liquid scintillator (GdLS). The scintillator will be used in the LZ Outer Detector to reject neutron events which could mimic a WIMP dark matter signal.
- **Assessment** by Scott Haselschwardt (LBL):
 - **Had we not done this experiment, the LZ Outer Detector would not be performing as it is today.** This would have a noticeable effect on LZ as a whole, as the false veto rate would be such that >5% of LZ lifetime would have to be removed from false coincidences with alpha decays in the Outer Detector.
- **Reference:** Scott Haselschwardt, private communication.

By Eryk Druszkiewicz & Dev Ashish Khaitan, University of Rochester, Dept of Physics and Astronomy, Rochester, NY - 14627 (private communication on Aug/12/2022).

The architecture of the DDC-32 and Logic boards and the tremendous flexibility of the FPGAs was vital during the commissioning of the LZ experiment.

- **Real time signal monitoring.** The summed waveforms are streamed on the LZ web, allowing system operators to remotely monitor raw signals from PMTs.
- **Parallel** zero-suppressed and not suppressed data acquisition modes. This allowed us to verify the performance of the zero suppression algorithm in-situ during commissioning of all 1391 channels in the LZ DAQ.
- **Arbitrary waveform injection** for system testing. This mode was used to commission the LZ triggers by testing system response to known signals.
- **System monitoring** via reduced quantities calculated in the FPGAs. Monitoring the quantities, we are able to verify the operation of the LZ detector in real time.

DDC-10 at the National Nuclear Data Center @ Brookhaven National Laboratory



- **The goal:** Measure signals from a variety of scintillation detectors and High Purity Germanium at the National Nuclear Data Center at BNL.
- **DDC-10** digitizer was delivered to the research group led by Dr. Elizabeth McCutchan.
- Initially, the lead person was Shaofei Zhu. A few weeks ago the research was taken over by Shuya Ota after Shaofei passed away.
- We are assisting the BNL group in using the digitizer and cleaning the signal of analog noise.

- Analog noise is caused by dirty power and / or pickup of noise from a switching power supply or a similar source.
- We are helping BNL write data collection software using our open-source library.

DDC-10 Is Helping Advance Proteomics, @ Brown University

Reference: Excerpted from a letter by Professor Derek Stein, Brown University, December 5, 2021.

- **The goal:** Develop methods to analyze proteins that will require unusually high data rates and time resolution.
- **The method:** Fragment a single protein and subsequently measure the molecular fragments by mass spectrometry. By precisely determining the mass and arrival time of each fragment, we aim to recover structural information about the protein. Our ultimate goal is to sequence the primary sequence of amino acids directly from single proteins.
- **Skutek instrument:** The Brown group currently uses a Skutek digitizer because it is unique in its ability to simultaneously monitor multiple mass channels with high bandwidth, pre-process detection signals, and precisely determine the times of ion detection events.
- Skutek is assisting the Brown group, providing them with answers to their questions and updates of the software.

Supply Chain Crisis

Part Supply Crisis Example

Aug/07/2022 @ Digikey. Searching for available **FPGAs** from Xilinx

<u>Family</u>	<u>prefix</u>	<u># of parts</u>	<u># of available parts</u>
Spartan-6 LX	xc6s..	233 parts	none available
Spartan-6 LXT	xc6s..	1 part	none available
Spartan-7	xc7s...	97 parts	none available
Artix-7	xc7a...	237 parts	none available
Kintex-7	xc7k...	147 parts	none available
Zynq-7	xa7z...	8 parts	none available

- Some assembly companies offer “send us your overstock boards and we will desolder the parts and send them back to you”.
- It is not a long term solution. We do not have overstock, anyway.

Summary

• Digitizers.

- We developed digitizers covering a range from 2 to 40 channels per digitizer.
- The low end 2-channel devices comprise FemtoDAQ Classic using BeagleBone, and **FemtoDAQ+** using our own MicroBone Single Board Computer.
- FemtoDAQ+ will offer **significantly better performance** than the previous FemtoDAQ.
- We keep adding software to the 10-channel digitizer according to user feedback.
- 32-channel devices were used to build the Data Acquisition for LUX-Zeplin.
- After substantial modifications, the 32-channel digitizer is now used in our collaboration with Argonne National Laboratory.
 - We added fast streaming to the design, **1 Gbps** by default, and **10 Gbps** as an option,
- 40-channel digitizer is our highest density prototype for those applications where 32 channels per board are not sufficient. (E.g., highly segmented detectors.)

• Logic module.

- In addition to the digitizers, we developed a **Logic Module** serving up to **512 channels**.
- The Logic Module was used in LZ DAQ in two ways, for readout and for trigger.

- Firmware:

- We organized the firmware around Application Firmware, Register Interface, Software Driver, and UI.
- The Register Interface uses the General Purpose Memory Controller of the AM3358 chip.
 - GPMC was one of the main motivations to transition from FemtoDAQ to FemtoDAQ+.

- Software:

- We adopted a unified web-based [JavaScript](#) technology for instrument setup and control.
- Running the GUI [does not require installing any software](#) on the target host.
- The GUI is using JavaScript which can run in [any browser](#), even on a cell phone.
- GUI can setup the instrument and save the configuration.
- Regular event files can be written to the SD card or to an NFS mounted disk.
- In addition to web GUI, we also offer a function library and a set of command line utilities.
- All software is offered to our customers in Open Source.

- **Continue** development of firmware and software for our digitizers.
- **Adopt** the web-based control technology in all our products.
- **Develop** high performance event streaming.
- **Contribute** to Nuclear Physics experiments and institutions.
- **Help support** the DOE mission.
- **Survive** the part supply crisis till electronic parts are available again.

Joanna Klima, Gregory Kick, David Miller, James Vitkus, Jeffrey Maggio

Past employee: David Hunter

Consultant: Eryk Druszkiewicz

Interns:

Mandy Nevins, Jeffrey Saylor, Dinesh Anand Bashkaran, Brian Kroetz, Vedant Karia, Edmond Tan, Soner Seckiner

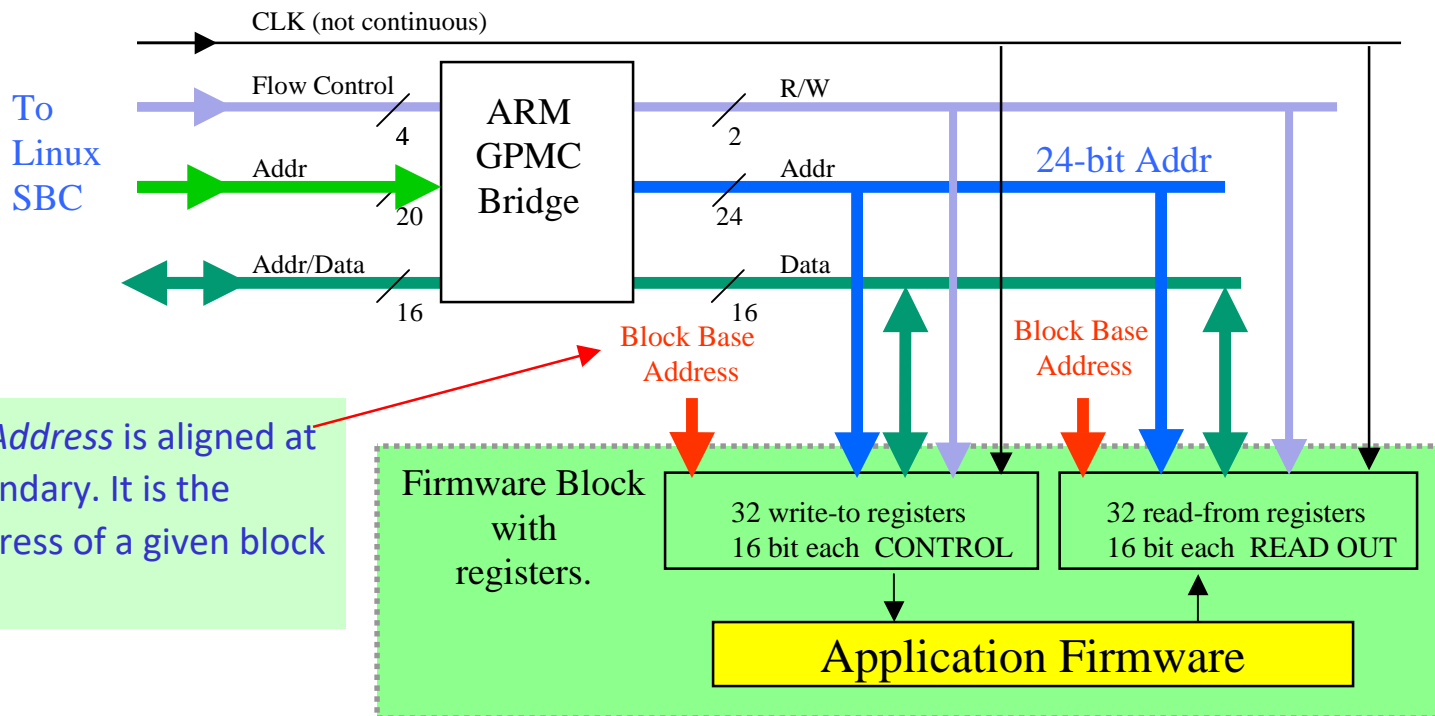
Special thanks to Michelle Shinn and Manouchehr Farkhondeh

Backup slides

We organize the FW and SW into *Features* offered by the instrument to the user.

The *Instrument Feature* consists of Application Logic, the register interface, SBC software, and remote control.

- Internally in the FPGA, the *Feature* is a Firmware Module with Registers for control and read out.
- Registers have *addresses* in the Linux memory space.
- The *Base Address* defines where the registers start in the Linux memory space.
- The *Feature* is interfaced to Linux SBC using the ARM General Purpose Memory Controller (GPMC).
- GPMC is a memory bus between the SBC and the FPGA.



Block Base Address is aligned at 64 byte boundary. It is the starting address of a given block of registers.

- A **family of digitizers**, from 2 up to 40 channels per unit, 14 or 16 bits @ 100 MSPS.
 - The versions with 250 MSPS are under development. The boards are assembled.
 - The digitizers with more than 16 channels will stay at 100 MSPS because of power.
- The 32-channel digitizer will be compatible with the GRETA / GRETINA / DGS environment.
 - This project is presented separately.
- **Small digitizers** are targeting small labs, education, and T&M markets.
- **Very low noise**: RMS about 160 microvolts, that is ~ 1.3 LSB @ 14 bits.
- Setup, monitoring, and diagnostic with on-board **Linux** Single Board Computer (SBC).
 - SBC can also perform **readout** at the rate ~ a few megabytes per second.
 - SBC can write **formatted event files** directly to NFS mounted disks.
 - SBC can monitor the detector signals with **low latency** in nearly **real time**.
 - SBC can show an **interactive display** of waveforms and histograms **in any browser**.
- A **variety of options** for the control software and GUI to be executed by the Linux SBC.
 - SSH, command line, Python, Jupyter, and Remote Python Call (RPyC).
 - JavaScript GUI compatible with any browser, any host platform (**even a cell phone**).