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IP Access Gateway

Continuous Acquisition TDC FPGA synchronized over packet networks

Award DE-SC0017156

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IP Access Gateway System

- Integrates Frontend, Backend, and computing subsystems into a software defined, in band time synchronized network through COTS HW, and IP based protocols;
- Provides ubiquitous timing synchronization with a precision range of 10pS or better and immediate event reconstruction.

Functional blocks:

- Continuously timestamping TDC engines, configurable for either accuracy or density (Ex: 16 channels at 500fS v. 256 channels at 8pS).
- Any combination of configurations coexist on the same FPGA device.
- The network interface – multiples of 10/25/100 GE optical links;
- Packet Switch.

Features

- ETDC determines the timing of both the rising and the falling edge of a pulse associated with an event;
- Minimum pulse width is 500pS;
- Sustained, continuous minimal pulse period = 1nS (2x 0.5nS);
- Maximum sustained rate is more than 2G timestamps corresponding to 1GHz signals (as limited by the IO bandwidth);
- IPAG uses the General Timing Synchronization (GTS) protocol and algorithms to synchronize numerically the timestamps;
- The numerical synchronization does not change local clocks, which eliminates transient errors and instability;
- Can provides ADC equivalent functionality for pulse width modulation (PWM) circuit with high tolerance to radiation;
- SW defined operation;
- Seamless interface and retiming of timestamps data from third party detectors.

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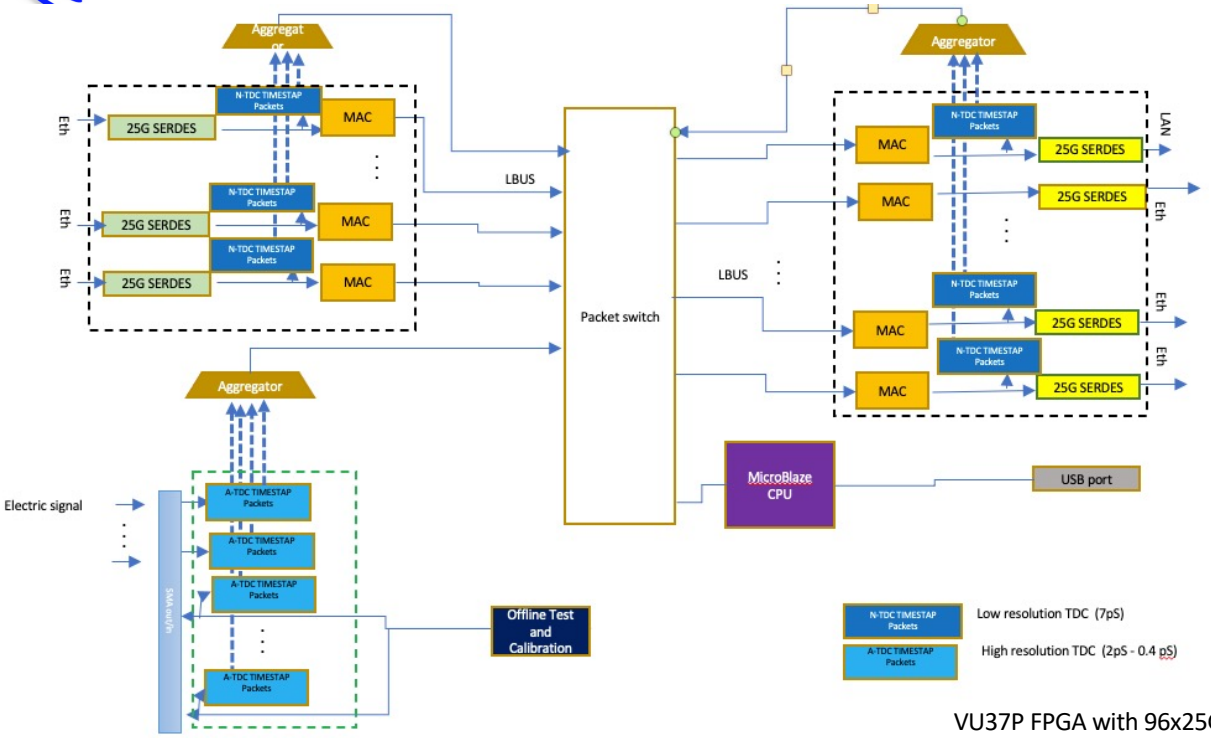
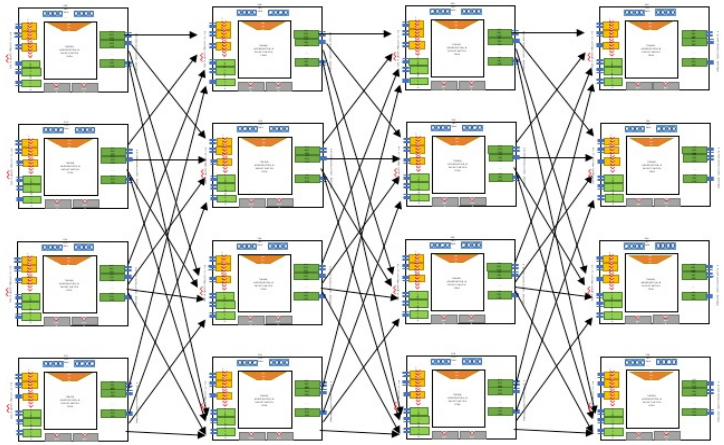
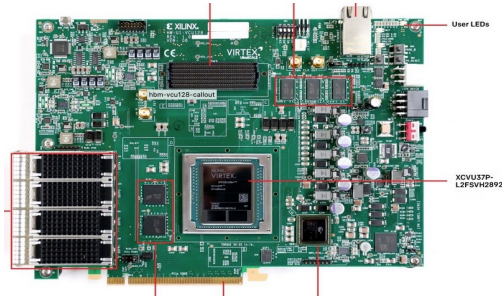
IPAG FPGA Functional Block Diagram





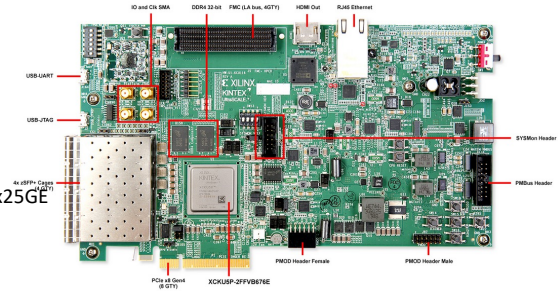
Higher count 25GE ports FPGAs can function as distributed switch with numerical time synchronization.

VU37P FPGA with 96x25G ports



16x25GE

KU5 FPGA with 16x 25G ports



4x25GE

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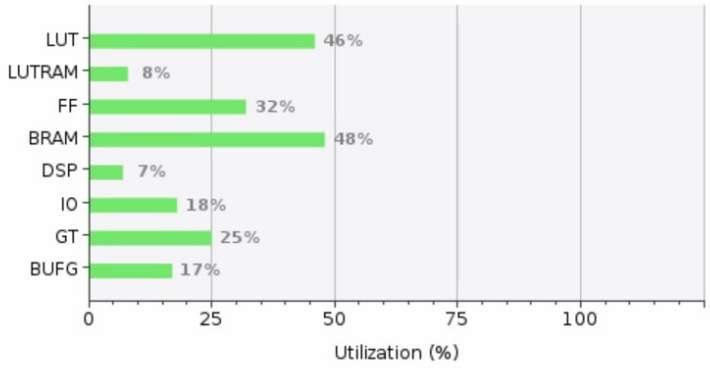
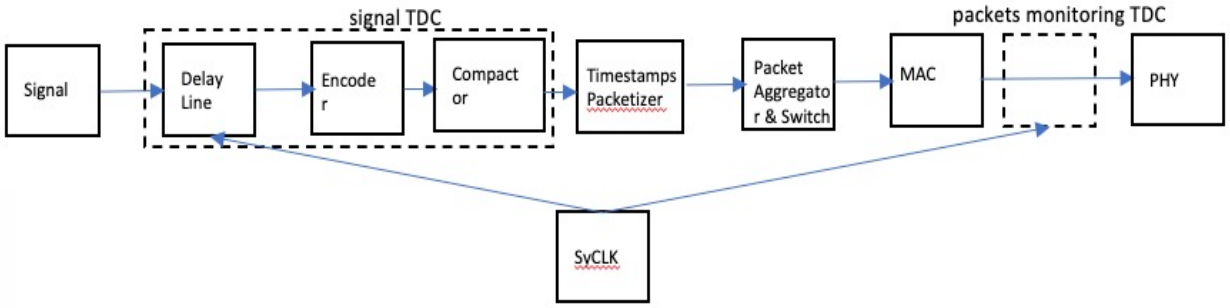
IPAG processing flow diagram

Ultrascale Kintex KU5p FPGA Implementation

total 32 TDC- 8pS, > 2 G ts/s
4x 25GE MAC
ILA
4 packers
UART control interface

Resource	Utilization	Available	Utilization %
LUT	98788	216960	45.53
LUTRAM	7836	99840	7.85
FF	140614	433920	32.41
BRAM	228	480	47.50
DSP	130	1824	7.13
IO	50	280	17.86
GT	4	16	25.00
BUFG	43	256	16.80





Our TDC comprises a Tapped Delay Line implemented in a high-speed Carry Chain (CC). A stable system clock (SCK) with a known frequency of 600MHz takes continuous snapshots of the signal traveling through the CC. The snapshot pattern is further analyzed by an encoder block, capable to generate up to four timestamps per SCK, corresponding to four transitions of the input signals. The estimated positions of the taps of the TDL where transitions happen are encoded into binary numbers. Noisy transitions are interpreted probabilistically. Linearity and phase corrections are applied to the timestamp. The accuracy requires the use of the low jitter global clock (GC) pins and distribution lines. Regular IO pins with higher jitter have lower precision.
The GTS protocol further determines the phase and frequency error of the local SCK and its counter relative to the timing of the root node, and retimes accordingly the local timestamps from FE.

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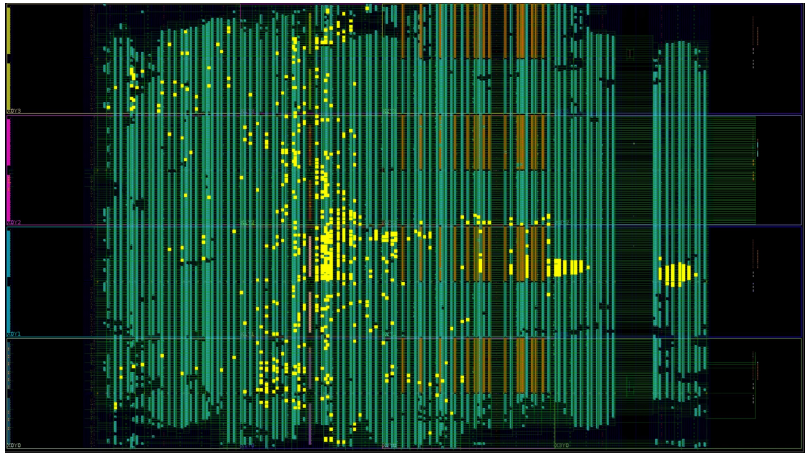
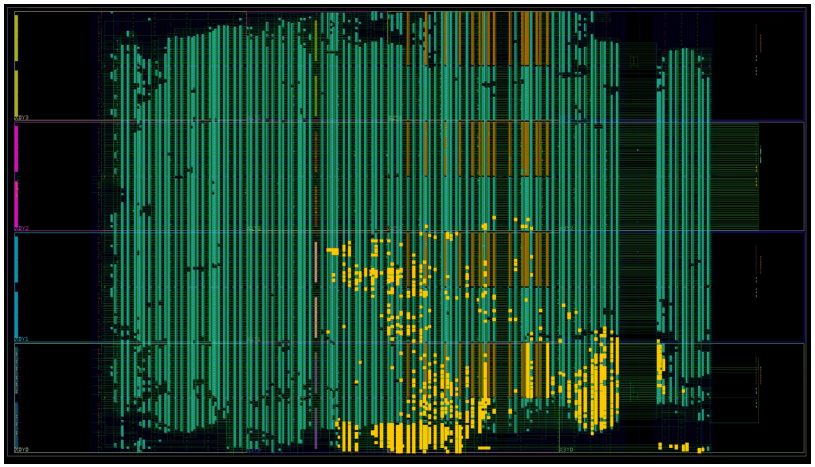
Automatically Placed and Routed, 600MHz FPGA
(no manual placement other than TDL)

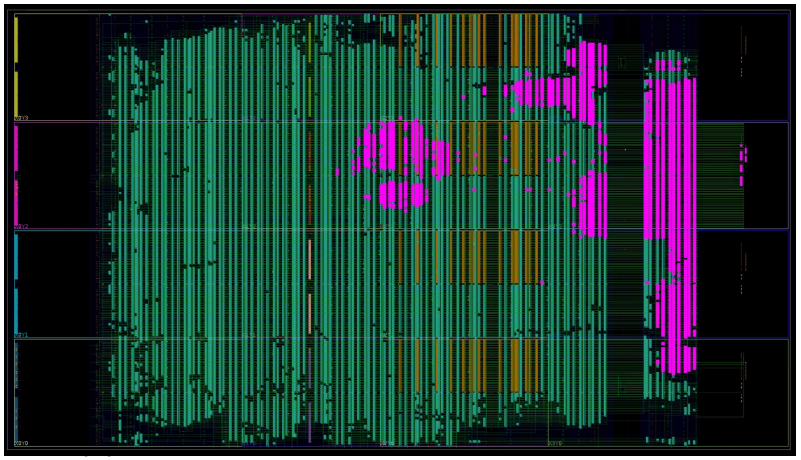
Packet Generator



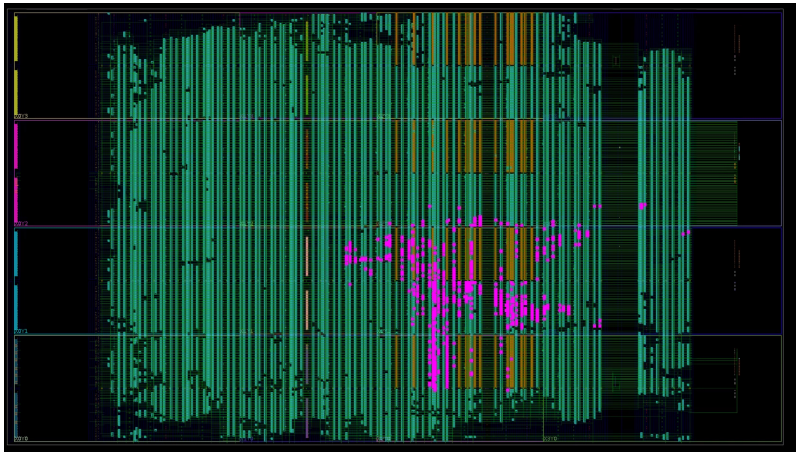
Signal TDC



4x 25GE MAC



Packet TDC



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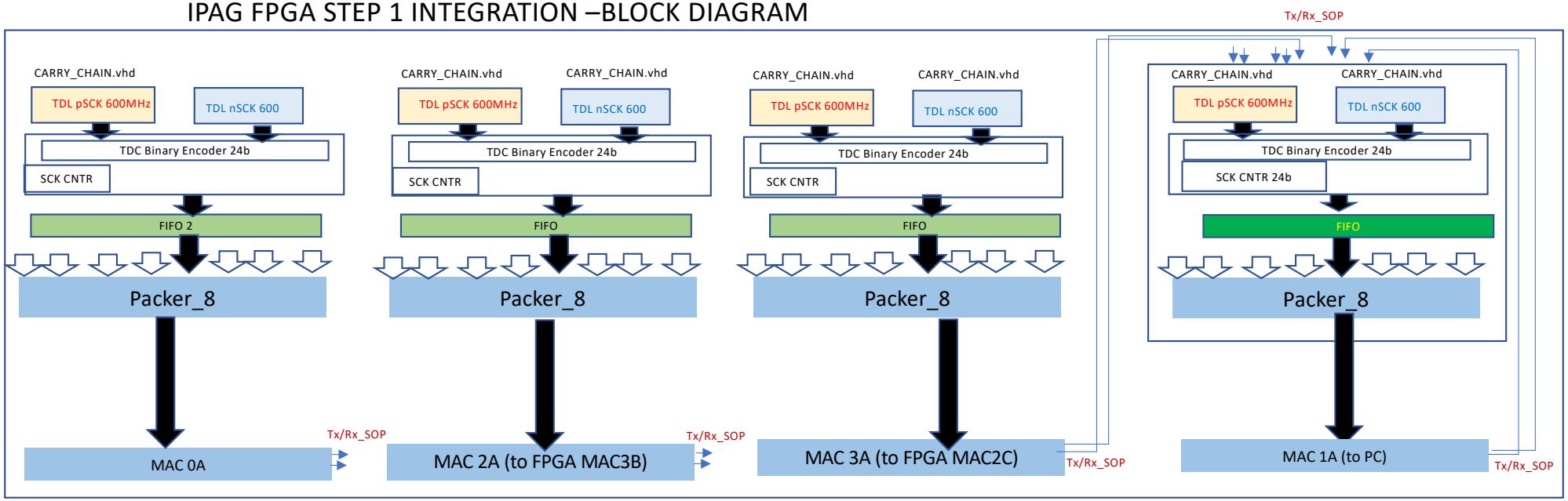
Network TDC 32b record format for production

Signal TDC 32b record format for production

Network TDC 64b record format for current integration tests

Signal TDC 64b record format for current integration tests

IPAG FPGA STEP 1 INTEGRATION –BLOCK DIAGRAM



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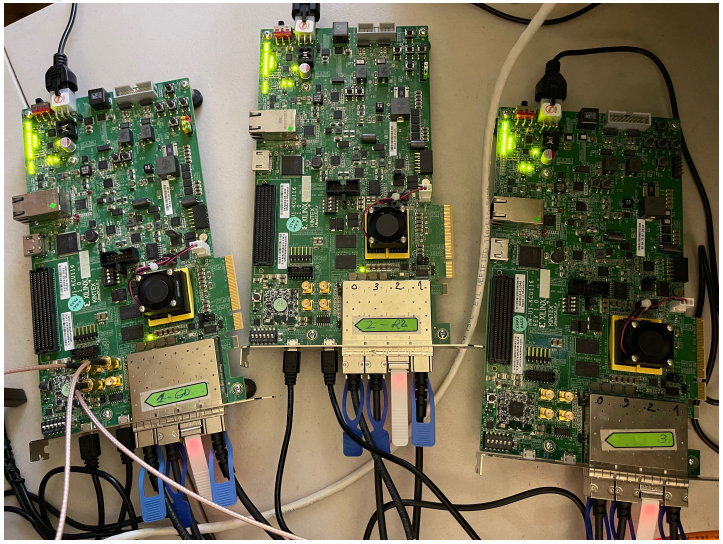

25GE line rate, 32 TDC stress test, and integration with GTS numerical protocol

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GTS - In Band Numerical synchronization for DWDM Continuous Readout Network

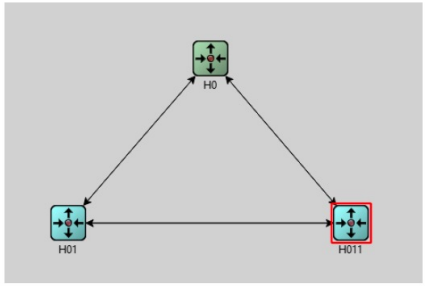
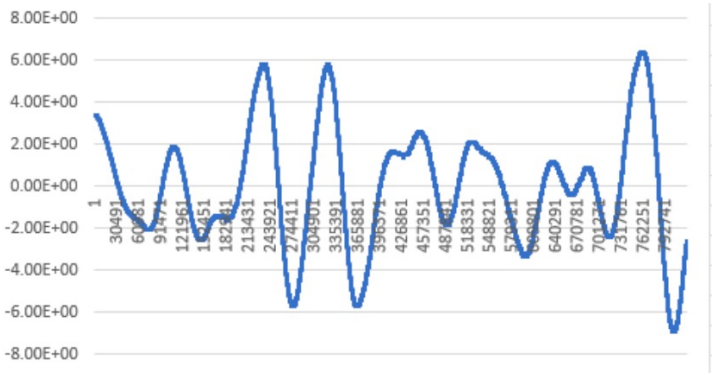
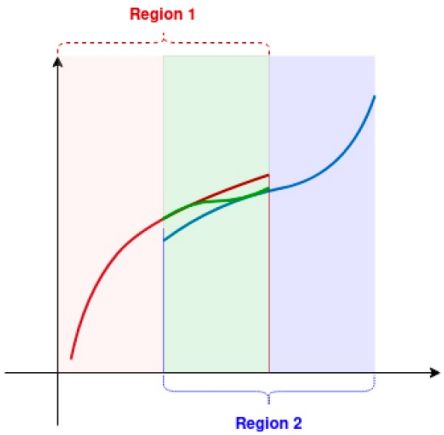


Figure 4.1: Closed Loop: Triangle network system



GTS simulated synchronization error (unit is 10E-13s) for the following timing corruption: Timing of node H01 has a frequency drift of 0.2%. Timing of node H011 has a sine wave drift with amplitude of 3uS and a period of 0.5Hz.



The GTS protocol determines with picosecond accuracy the relation between time domain of ports connected through a link. The timestamps generated by network packets traveling between the linked ports are sent through metadata packets to a processing node and matched according to the CRC. A propagation delay (PD) is calculated for each packet and synchronization relation is extracted from the PDs in a certain time interval. A mending function ensures continuity between adjacent intervals.

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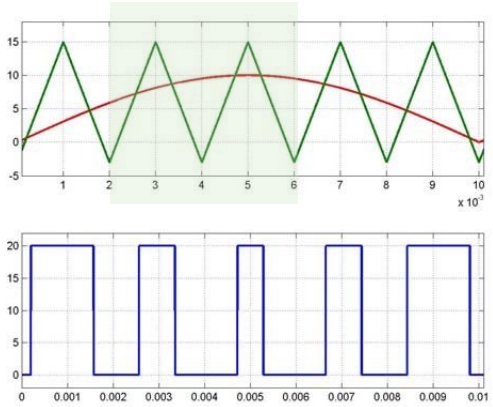
Application Example
PWM Timestamped ADC

ADC – TDC reciprocity.
Numerical average of PWM timestamps provides signal amplitude.
IPAG FPGA provides both timing, and fast ADC in multiple combinations.
FMC mezzanine VITA cards provide HW adaptation for PWM.



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Thank you !

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