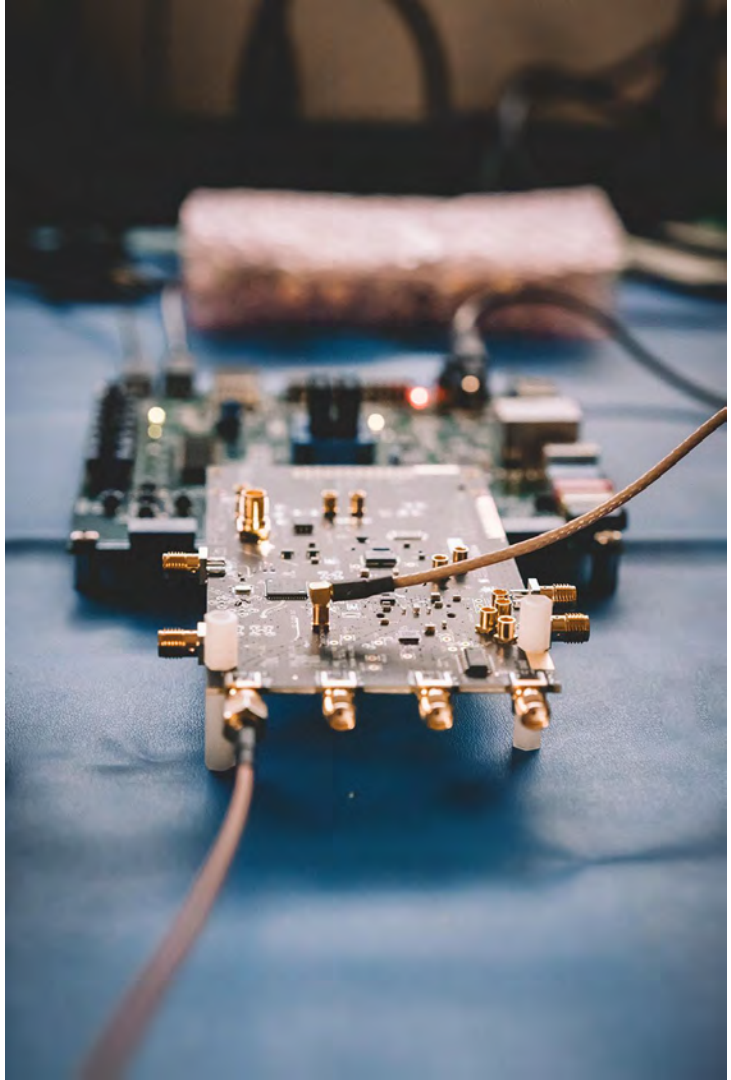


NALU SCIENTIFIC
ENABLING INNOVATION

Design and development of the All-in-One Digitizer System-on-chip "AODS"

A low-cost, low power, low-noise and low channel-count Application Specific Integrated Circuit (ASIC) with a high dynamic range option.

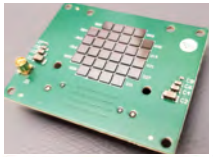
Aug 24, 2022
Isar Mostafanezhad, Ph.D.
Founder and CEO at Nalu Scientific LLC

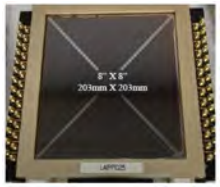
Work funded by DE-SC0019527

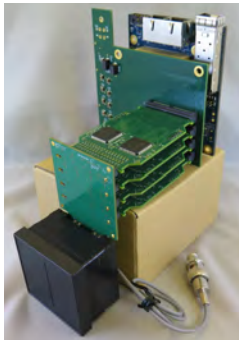
NCE: 12/31/22

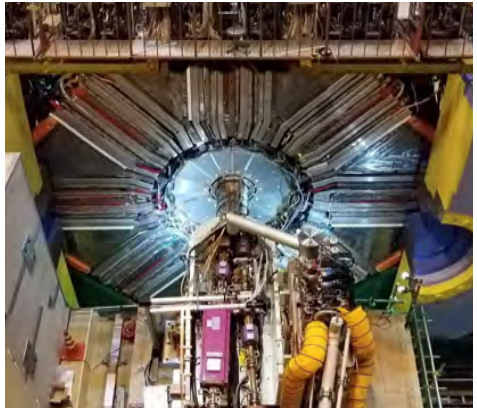
NALU SCIENTIFIC
ENABLING INNOVATION

WAVEFORM DIGITIZER SoCs
FOR PRECISE TIME OF FLIGHT ESTIMATION









1. Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

2. Integration:

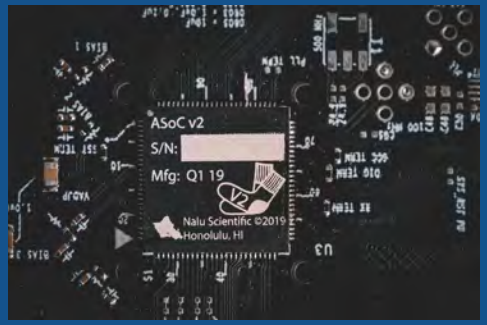
- SiPM
- PMT
- LAPPD
- Detector arrays

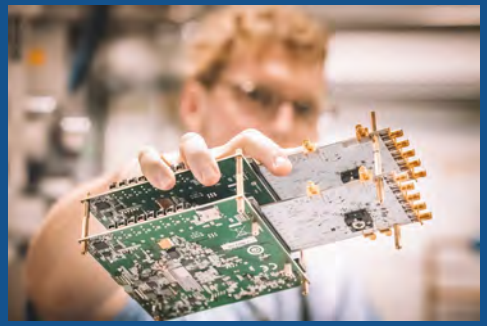
3a. Main application:

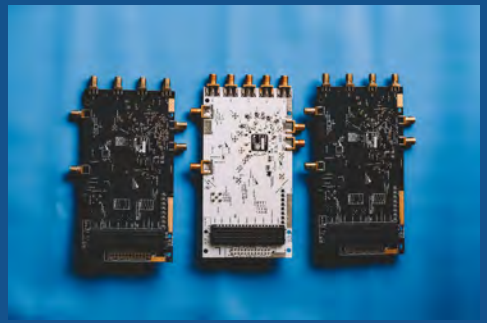
- NP/HEP experiments
- Astro particle physics

3b. Other applications:

- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging







ABOUT NALU SCIENTIFIC

Fast Growing Startup in Honolulu, Hawai'i

- Located at the Manoa Innovation Center near U. of Hawaii
- 20 staff members-diverse background
- Access to advanced design tools
- Rapid prototyping and testing lab

Technical Expertise

IC design:	Analog + digital System-on-Chip (SoC)
Hardware design:	Complex multi-layer PCBs
Firmware design:	FPGAs, CPUs
Software design:	GUI, analysis, documentation

Scientific Expertise - NP/HEP subject matter experts

- Physicists (3x)
- Electronics for large scientific instruments

Exclusive Distributor Agreement for North America

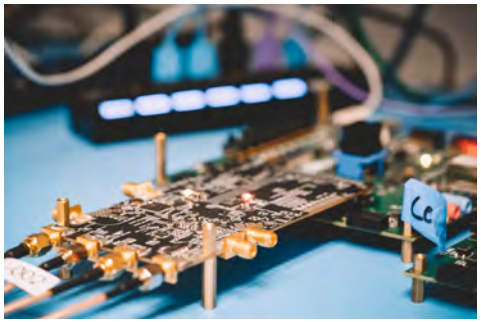
- Sales of ASICs, eval boards
- Enhanced OEM opportunities

CAEN Technologies Inc.

Nalu = 'wave' in native Hawaiian language

Current SoC-ASIC Projects

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-3	0.6	2k	64	80-120	Rev 1 avail
AARDVARC	8-14	2.5	32k	4	10	Rev 3 avail
AODS	1-2	1	8k	1-4	100-200	Rev 2 avail
UDC	8-10	1.5-2	4k	16/32	10	Rev 1 avail

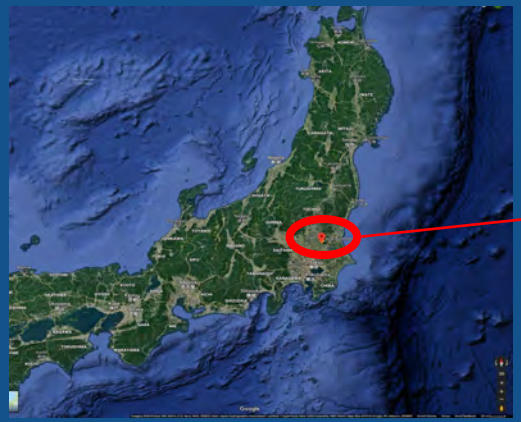


- **ASoC**: Analog to digital converter System-on-Chip
- **HDSoC**: SiPM specialized readout chip with bias and control
  - Baseline readout for EIC hpDIRC
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option

Work funded by DOE SBIRs. University of Hawaii as subcontractor.

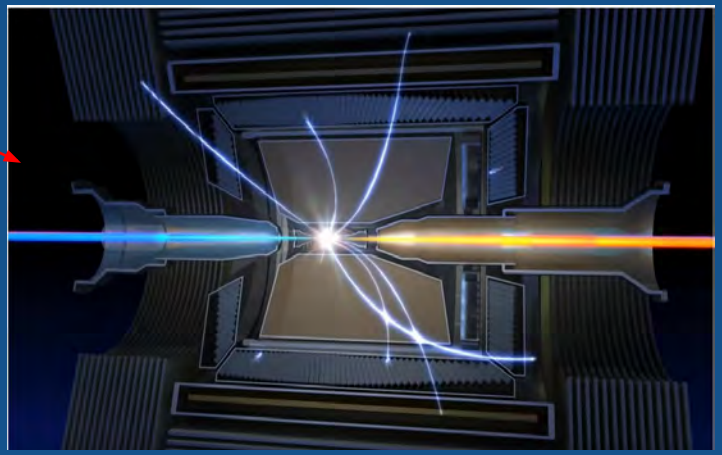
WHERE WE STARTED

A Search for New Physics – The Belle II Experiment



Tsukuba City
Located 60 mi north of Tokyo

High Energy Accelerator Research Facility (KEK)
in Tsukuba



Interaction point inside the electron/positron collider
Source: KEK Youtube channel

AODS Project Highlights

Low channel count, low cost, digitizer with daisy chain and high dynamic range options.

Overall technical objective:

Functional AODS chip fabricated, tested, characterized and documented:

a. On-chip generated clocks and their associations
b. On-chip signal processing capabilities for Phase I (a simplified DSP)
c. On-chip calibration circuitry
d. Digital transceivers and failsafe mechanisms for daisy-chain operation

Parameter	Specification
Sample rate	1-2 GSa/s
Analog Bandwidth	500MHz
No. bits	12
Supply Voltage	2.5V
Dynamic Range	60 dB
Virtual dynamic Range	90 dB
Timing accuracy	<100ps
Gain Response	As low as 32 ns
Input noise	1mV
Gain stages	0dB,15dB, 30dB, (45dB)
Analog buffer	16384 samples
Integration	SoC
Serial Rate	500Mbps

Phase II technical objectives:

1. AODS Design: it will be based on the experience gained from Phase I and will benefit from a top-down approach that will provide basis for further verification. Analog front end will guarantee programmable gain, termination and high dynamic range. Digital back end will provide dynamic range integration, digital signal processing and communication (daisy chaining) features.
2. AODS Verification: based on previously defined specifications will be separately performed on analog and digital portions and the overall chip
3. AODS Prototype Fabrication: will use well tested 250 nm technology to reduce the risk
4. AODS Evaluation PCB Design: will emphasize extensive testing of all the novel AODS features
5. Firmware/Software and testing : design and development of firmware and software to allow extensive testing of all AODS features, as well as basis for standalone use of evaluation boards by potential users.

AODS V2 DESIGN DETAILS

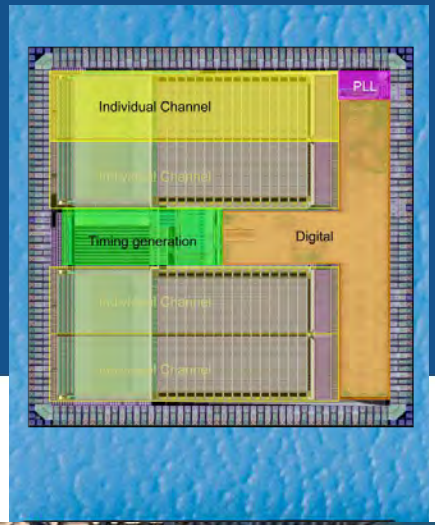
Compact, high performance waveform digitizer

- Mid performance digitizer: 1-2 Gsa/s
- Highly integrated
- Commercially available, low cost, patented design
- 5mm x 5mm die size

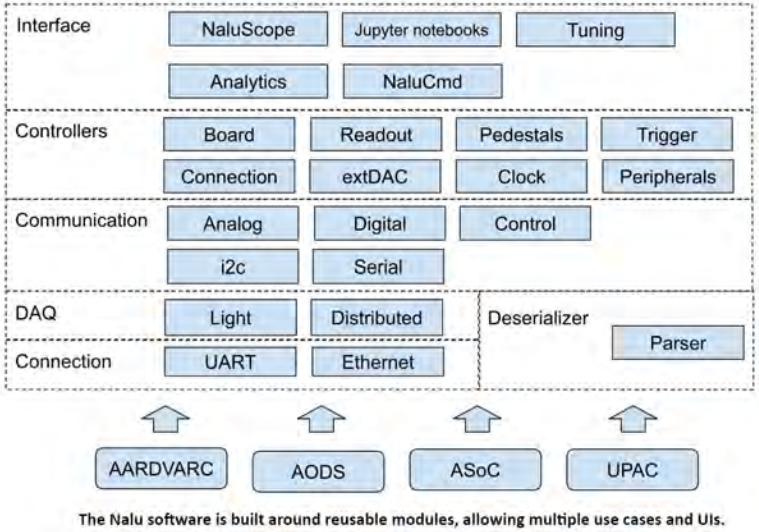
Parameter	Spec
Sample rate	1-1.5 GSa/s
Number of Channels	4
Sampling Depth	16kSa/channel
Signal Range	0-2.5V
Number of ADC bits	12 bits
Supply Voltage	2.5V
RMS noise	~1.5 mV
Digital Clock frequency	25MHz
Timing resolution	50-100ps
Power	120mW/channel
Analog Bandwidth	850MHz
Serial interface	Up to 500 Mb/s***

- Calibration memory access
- PLL on chip
- Isolated analog/digital voltage rings
- Serial interface
- High dynamic range mode
- Self triggering
- Eval cards available
- Custom boards under dev

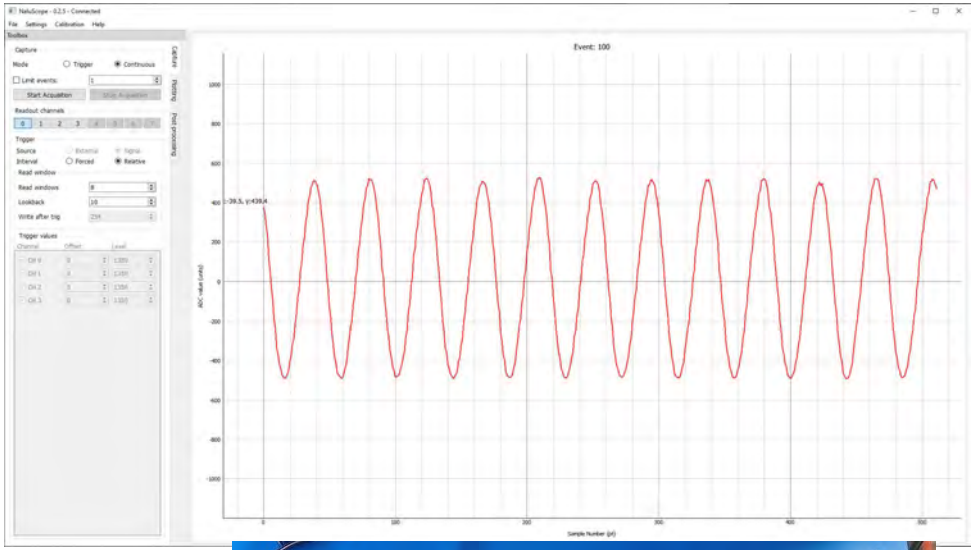
IEEE NSS 2020



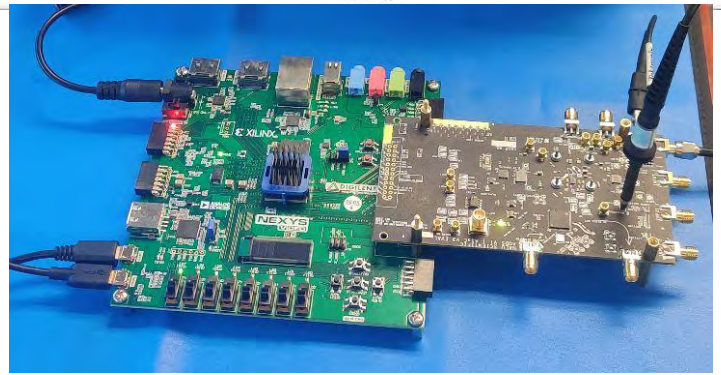
NaluScope Common Software and GUI

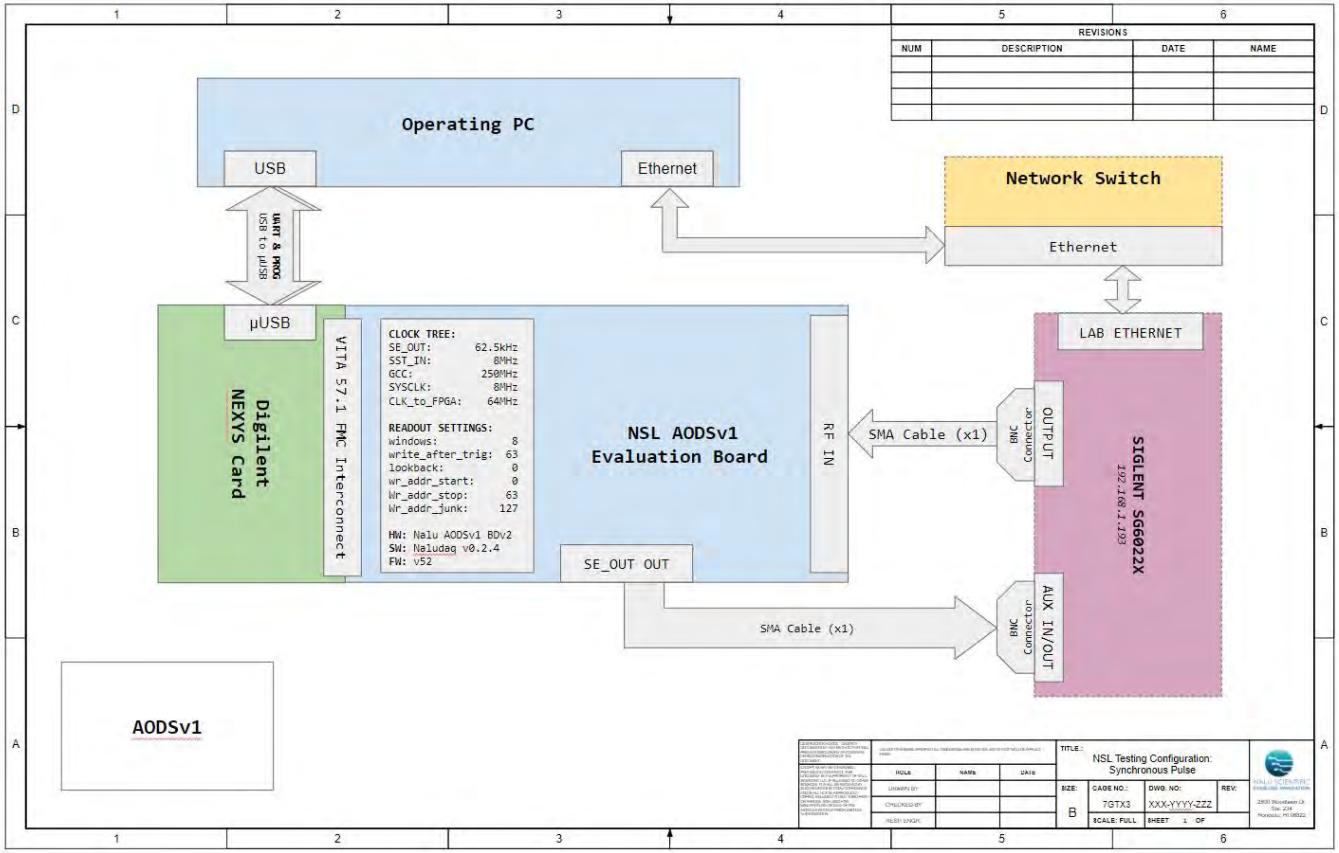


The Nalu software is built around reusable modules, allowing multiple use cases and UIs.



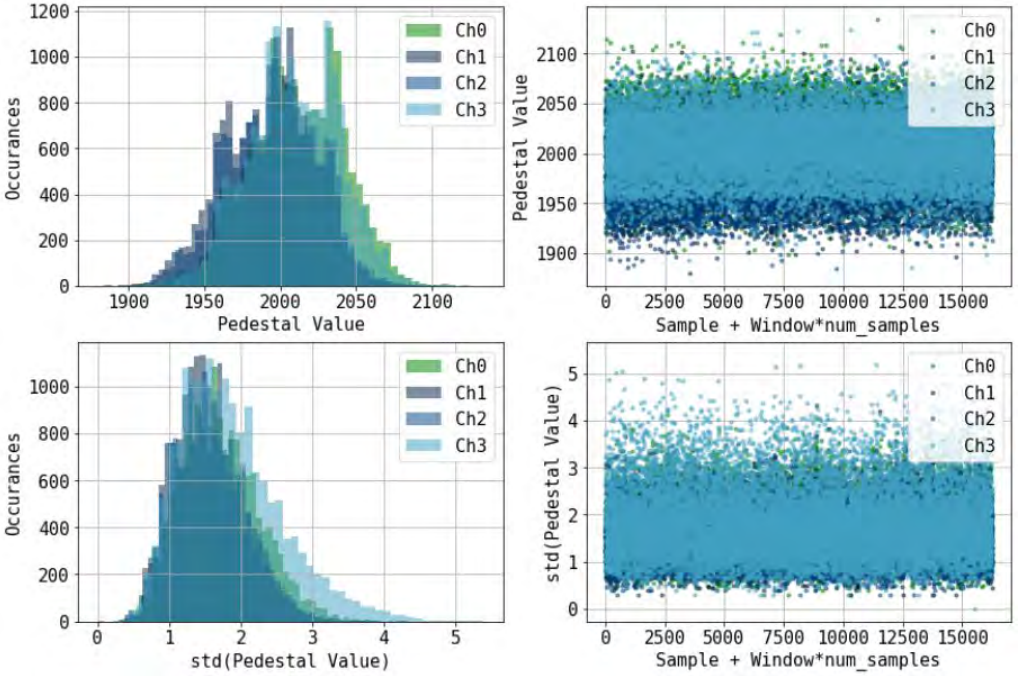
- Windows/Linux PC
- USB interface
- GUI, CLI interfaces
- Common to all Nalu chips
- DAQ configuration
- Data exploration, visualization, curation and storage

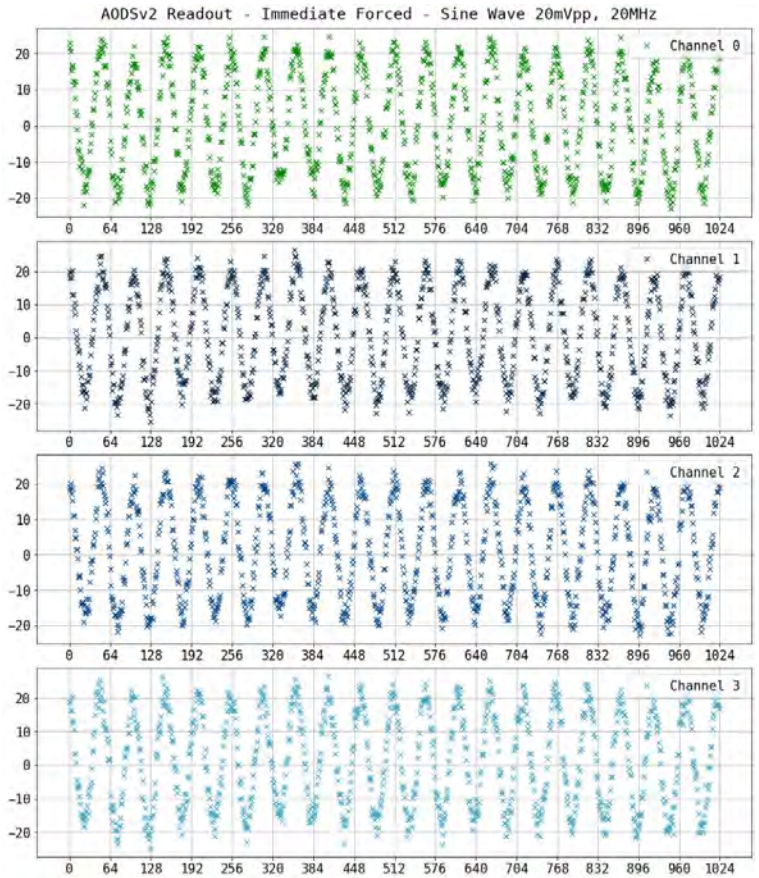




GAIN STAGE CONFIGURATIONS - Initial Testing

DIRECT INPUT MODE

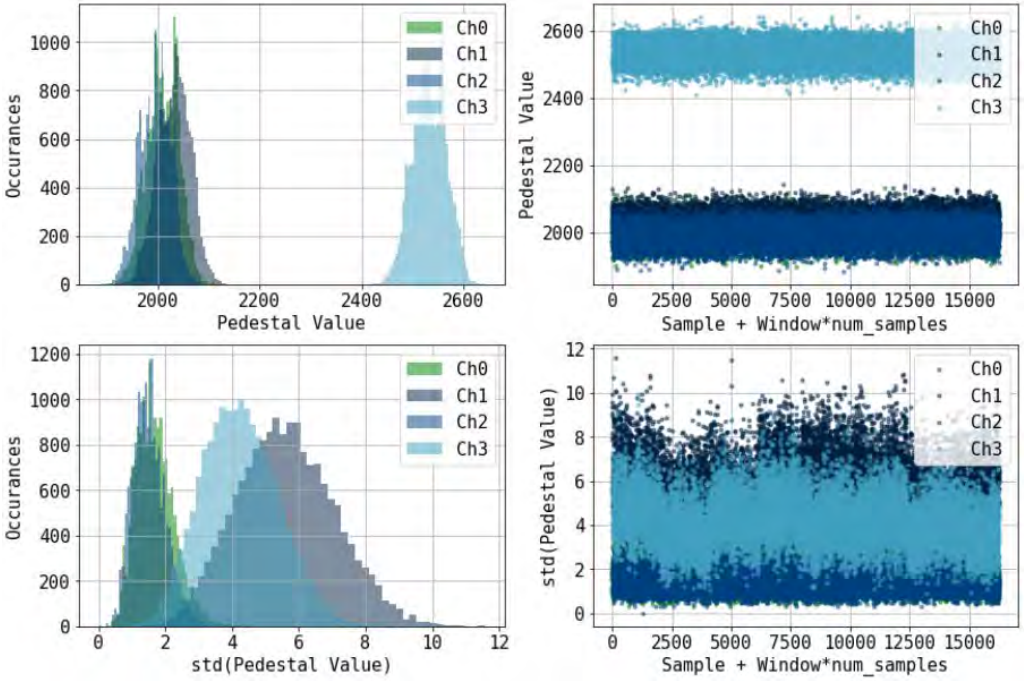


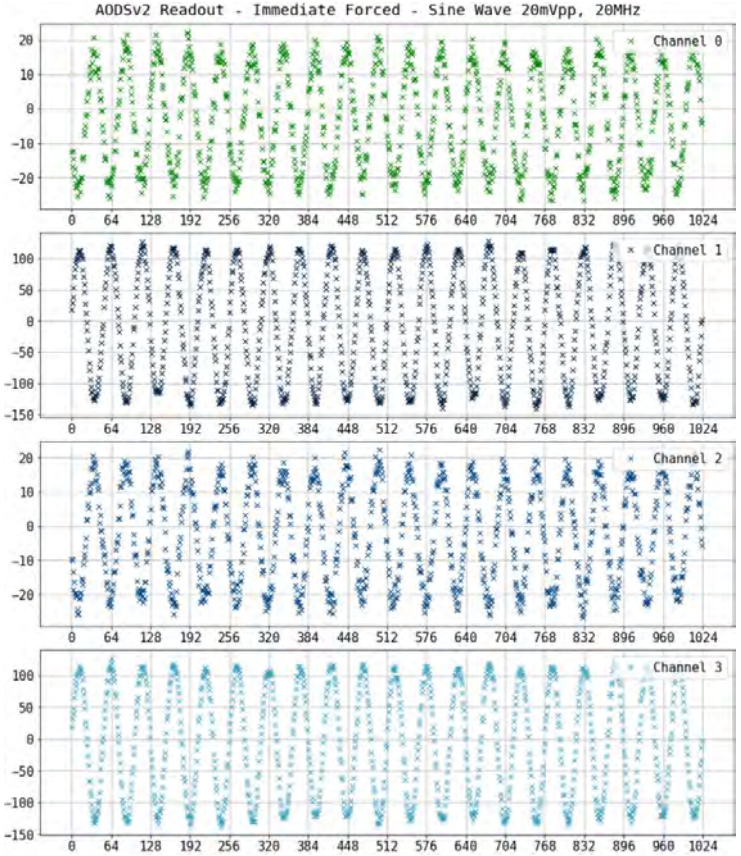


In this mode, all channels are directly fed, with independent inputs and no gain stages

GAIN STAGE CONFIGURATIONS - Initial Testing

TWO SINGLE STAGES MODE

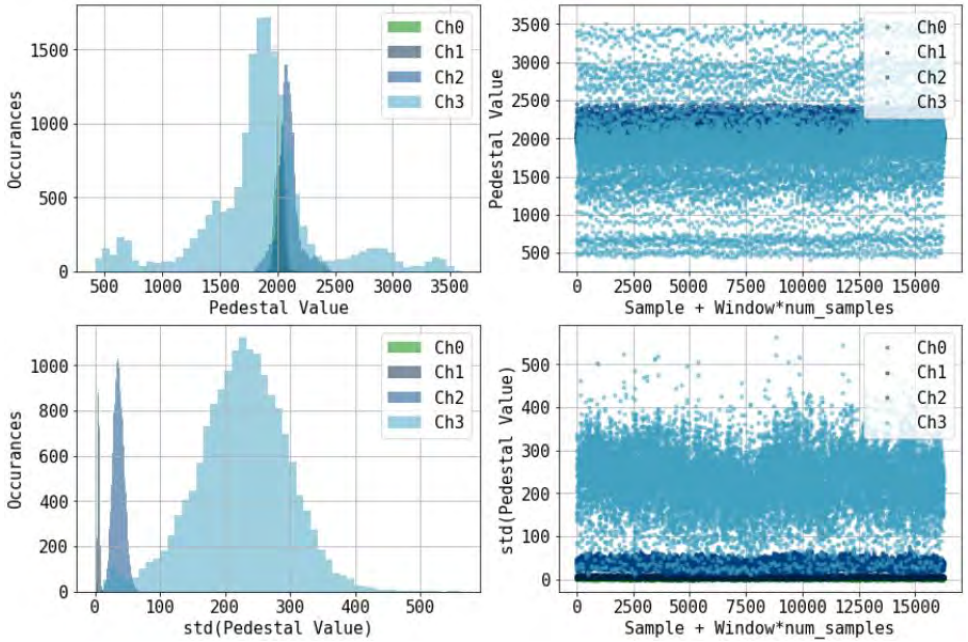




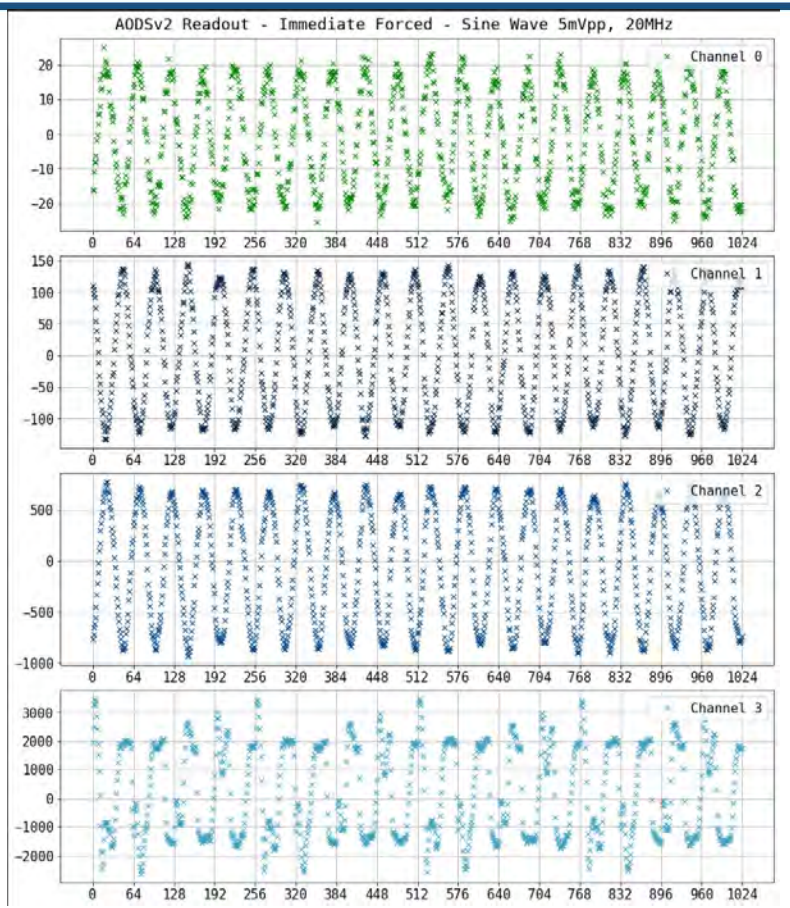
In this mode, channel 1 is a single gain stage version of channel 0's input, and channel 3 is a single gain stage version of channel 2's input

GAIN STAGE CONFIGURATIONS - Initial Testing

ONE TRIPLE STAGE MODE



In this mode, channel 1 is a single gain stage version of channel 0's input, channel 2 is double gain stage version of channel 0's input, and channel 3 is triple gain stage version of channel 0's input

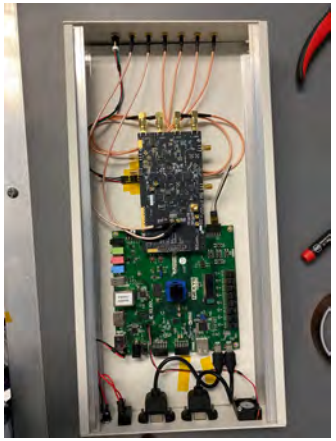


Summary of Activities

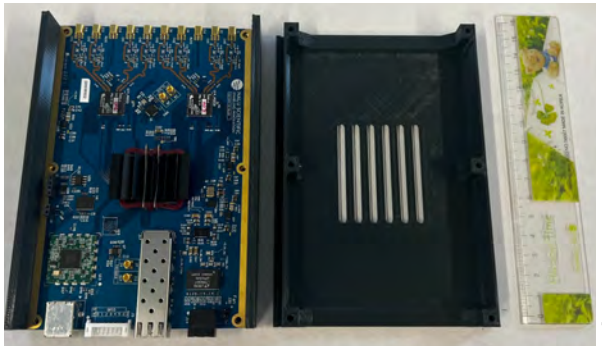
- Initially fell behind schedule:
  - Phase Started in April 2020 - pandemic onset
  - Extra time needed for extensive testing
  - Supply chain problems: FPGA, regulator, clock chip shortage
- Generally caught up on schedule given the NCE
- AODS V2 designed and fabricated in Feb 2022
- AODS V2 testing underway- Items still under test:
  - TID
  - Finalize digital/serial/daisy chain verification
  - Better test board for high dynamic range mode
  - Software and firmware implementation of the high dynamic range mode

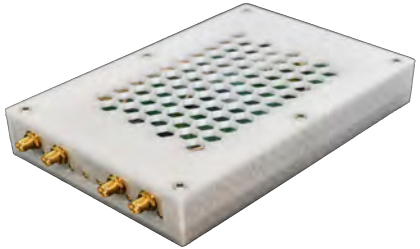
Commercialization

- Sold several ‘NaluBox’ digitizers
  - No ads, only word of mouth!
  - Moving to compact form factor
- Several integration R&D contracts from labs
- FFP product sales contract from lab
- Distributor agreement with CAEN
- <u>Users want a solution (box), than a chip:</u>
  - Vertical integration (chip+HW+FW+SW+app note)
  - Focus on value-add engineering
  - Multi discipline knowledge of the user needs



Shrinking!





ACKNOWLEDGEMENTS

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