Pacific MicroCHIP Corp.

An ASIC with a Low Power Multichannel ADC for Energy and Timing Measurements

DoE award number: DE-SC0018566
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Date of review: 08/23/2022

OUTLINE

- The company, its specialization/expertise
- Multichannel ADC for energy and timing mesurements specifications
- ADC core architecture
- Digital architecture
- ADC data output interface
- Event-driven backend and output DATA frame structure
- ADC performance test
- ADC testing results and pulse processing
- Phase IIB project schedule
- Future plans

COMPANY

Pacific MicroCHIP Corp. is incorporated in 2006. It is headquartered in Culver City, California. Main focus – providing IC/ASIC design services and turnkey solutions. The office includes the working space and a laboratory for ASIC testing.

Core expertise:

- Analog (ADC/DAC, CTF, VGA, BG, LDO)
- Mixed Signal (PLL, CDR, SerDes, MDrv, TIA)
- RF (LNA, Mixer/Modulator, PA)
- Digital (RTL, Synthesis, P&R, Timing Closure, DFT, Verifications)
- Layout (CMOS/SiGe) down to 7nm

MULTICHANNEL ADC ASIC SPECIFICATION

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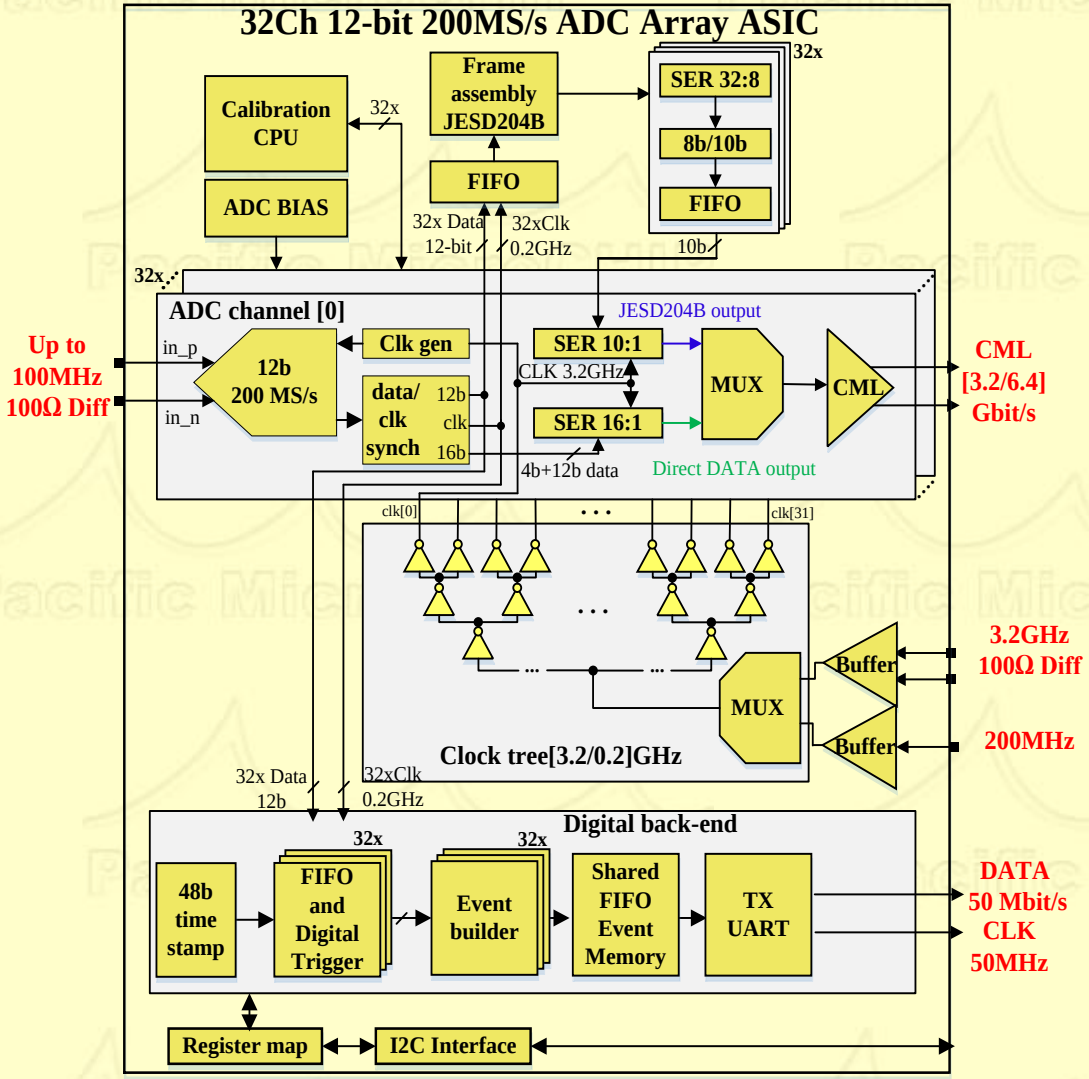
FEATURES:

- 32 independent channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input signal
- ENOB up to 9-bit
- Programmable input signal bandwidth 0.1-0.3 GHz
- Integrated event-driven digital backend
- JESD204B output data interface
- Extended temperature range -40C..+125C
- Low power consumption 5 mW / channel (w/o interface)
- I2C interface for ASIC control

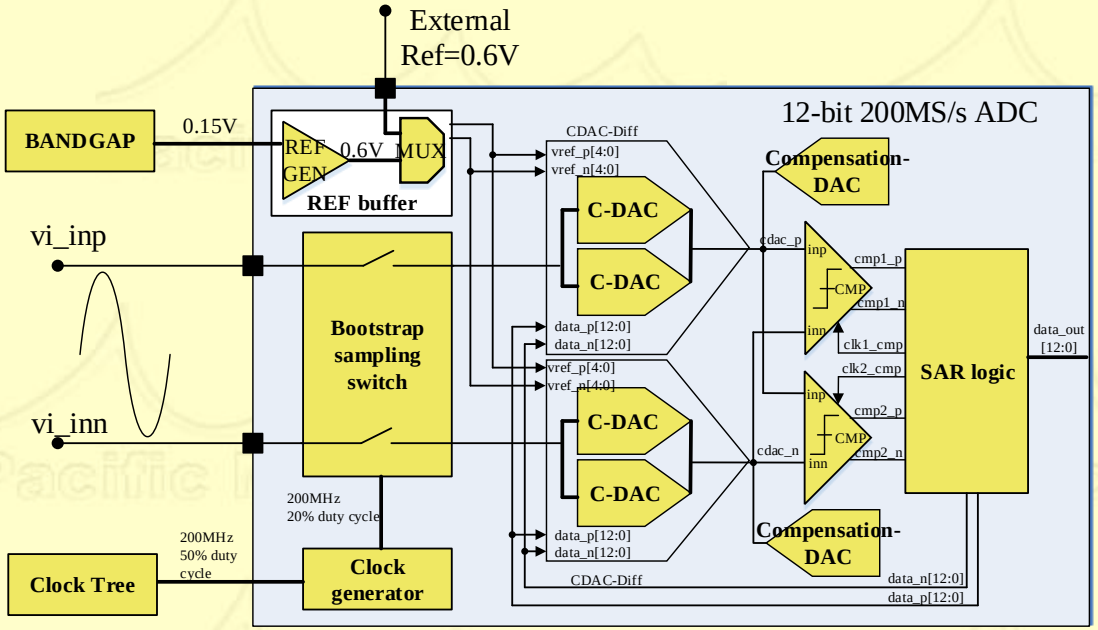


ADC CORE ARCHITECTURE

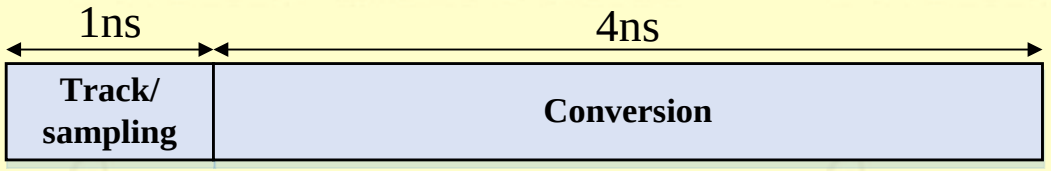
FEATURES:

- 12b SAR ADC architecture
- Segmented 3t-9b CDAC
- Optional external/internal ADC reference voltage source
- Fractional reference voltage
- Dual comparator
- Asynchronous logic
- Built-in FSM for comparator offset compensation
- Built-in FSM for CDAC non-linearity calibration

ADC CORE BLOCK DIAGRAM:



ADC TIMING DIAGRAM:



RAW ADC DATA OUTPUT

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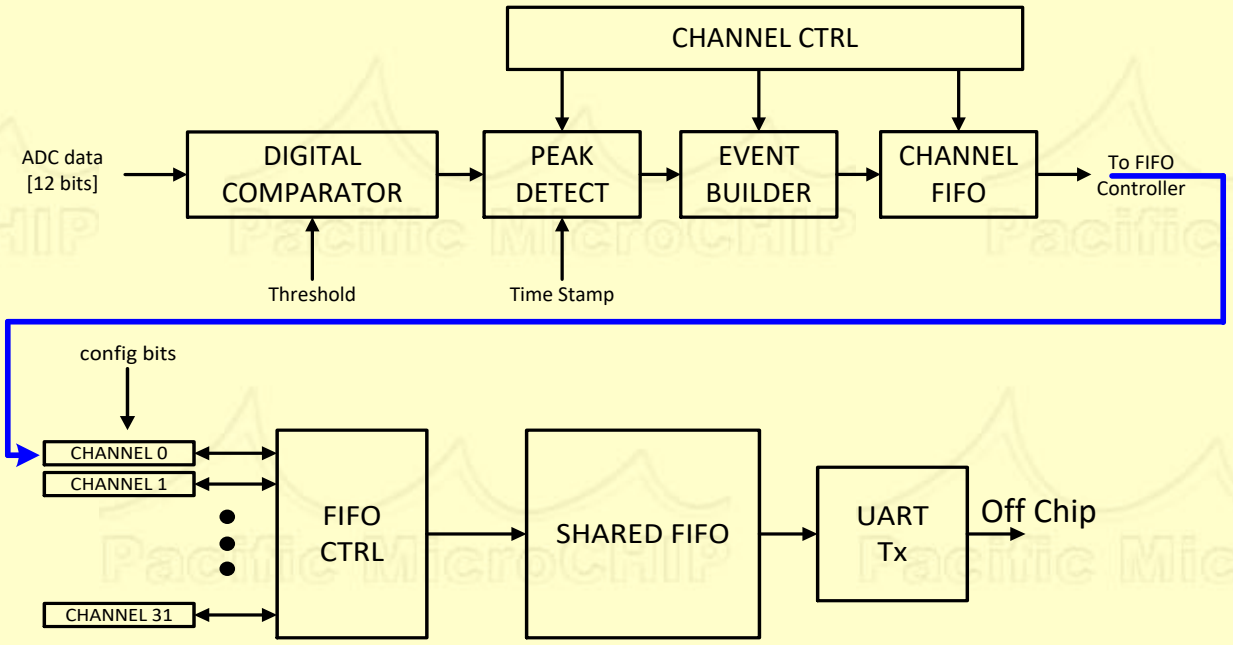
Mode	JESD 204B lanes	ADC per lane	Lane data rate	ADC data rate
Full speed	16	2	6.4Gbps	200MS/s
Half speed	8	4	6.4Gbps	100MS/s
Quarter speed	4	8	6.4Gbps	50MS/s

- Programmable ADC sampling rate of 200/100/50 MS/s
- Constant JESD204B output data rate 6.4Gbit per second
- Shared JESD204B output data interface between 2/4/8 ADCs reduces the number of interface lines, allowing high system integration density

EVENT–DRIVEN BACKEND

- This ADC output is monitored by a digital comparator with a programmable threshold
- When the ADC input exceeds threshold, a time stamp is assigned, and the peak value of the incoming ADC data is recorded.

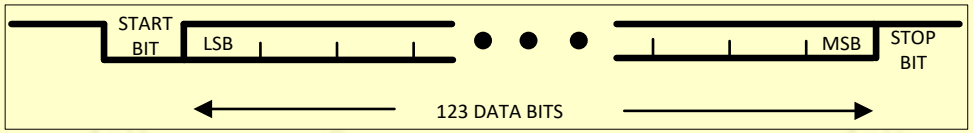


Event-driven digital backend was built in collaboration with LBNL. And we want to thank Dr. Carl Grace for his effort.

- When the event is completed, the relevant information is assembled into a packet by the Event Builder block. When the shared FIFO is ready, events stored in the channel FIFO are read out.

OUTPUT DATA FRAME

Bits	Field Name	Comment
[123]	Parity	Used to monitor integrity of data transmission.
[122]	Event Declaration	0 → test event (see text), 1 → normal
[121:119]	Fixed	Fixed bits - should always read value 3'b011
[118:107]	Window Interval	Determines the number of ADC samples to examine looking for a peak.
[106:102]	Channel ID	5-bit unique identifier.
[101:54]	TOA (Time of Arrival)	The timestamp of where the ADC value passed the threshold. Covers ~16 days at a 200 MHz clock rate.
[53:42]	TOP (Time of peak)	Supports shaper peaking times of up to 20 µs at a 200 MHz clock rate.
[41:30]	TOT (Time over Threshold)	Supports shaper pulse widths of up to 40 µs at a 200 MHz clock rate.
[29:18]	Peak Value	12-bit peak value recorded in the event.
[17:6]	Channel Threshold	12-bit threshold value used during this event.
[5:0]	Shared FIFO usage	For diagnostics and debugging.



50Mbps / 124+2bit / 32ch
≈ 12.4k events per second per channel

ADC POWER CONSUMPTION

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Block	Analog supply current, mA @ 0.9V	Digital supply current, mA @ 0.9V	I/O supply current, mA @ 1.2V	Ground, mA @ 0V
ADC CHANNEL	1.65	7.82	14.88	25.03
ADC CORE 12b@200Msps	1.46	1.62	N/A	3.73
JESD204B PHY	N/A	4.58	14.88	19.48

Typical power consumption of ADC w/o DATA interface: **5mW / ch**

Typical power consumption of ADC with DATA interface: **15.7mW / ch**

(*One JESD204B output data lane used per 2 ADCs operates at 200Msps*)

CHIP, ASSEMBLED PART AND TEST BOARD

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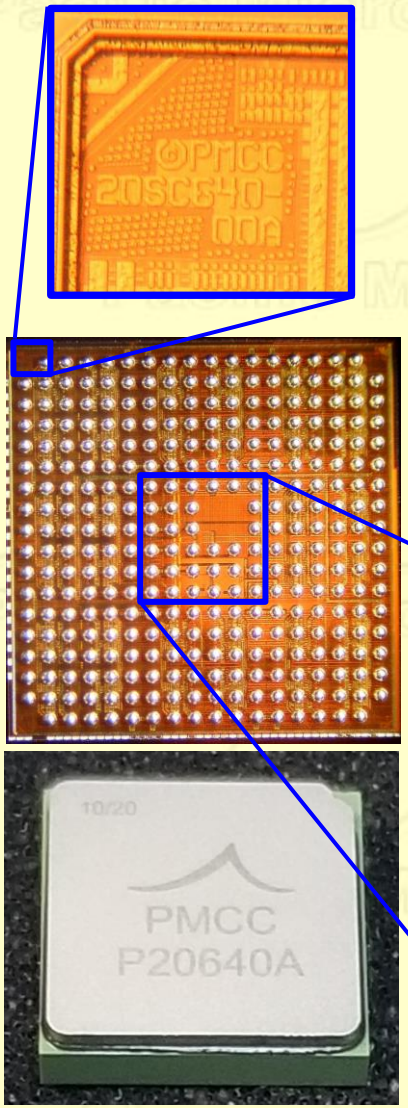
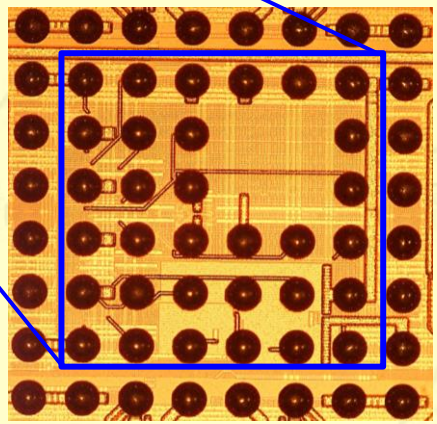
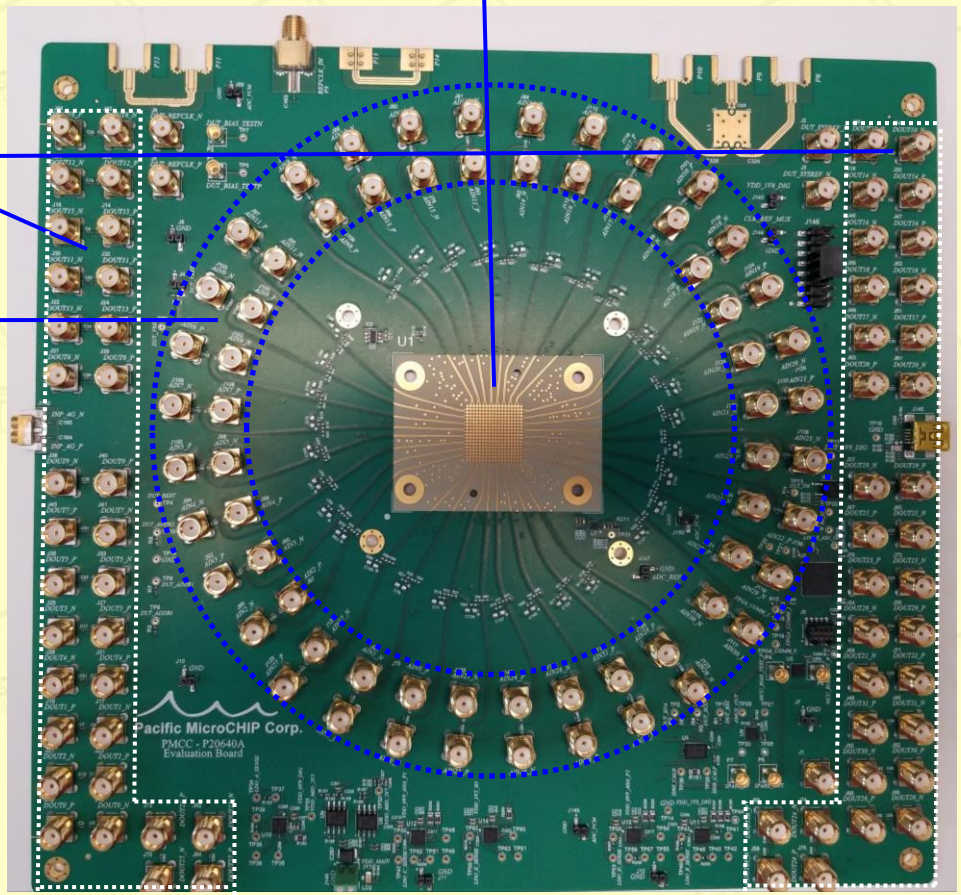




Area for DUT socket

ADC direct output

Analog inputs



TESTING RESULTS ADC (1st Generation): PERFORMANCE

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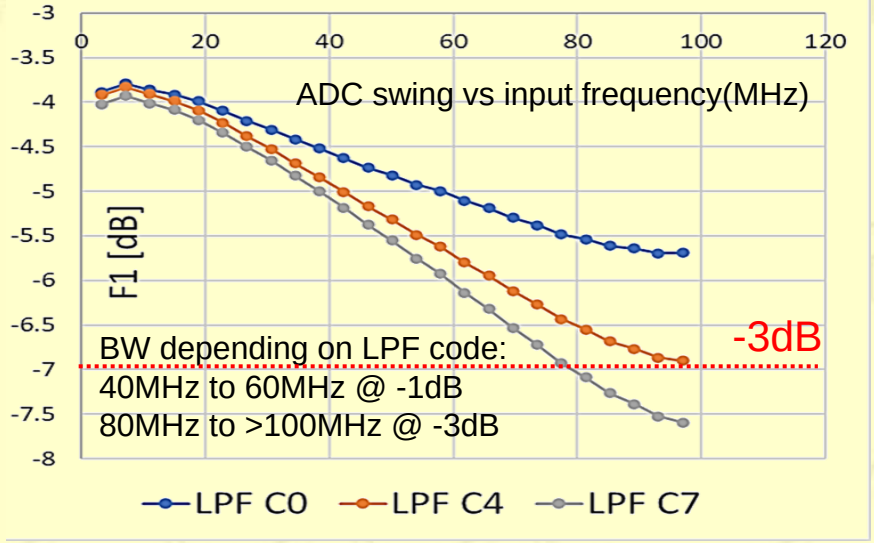
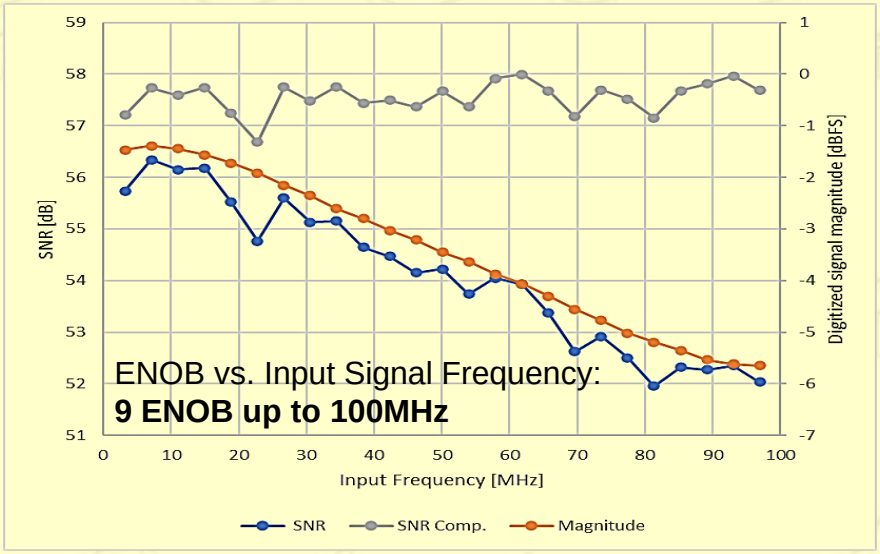
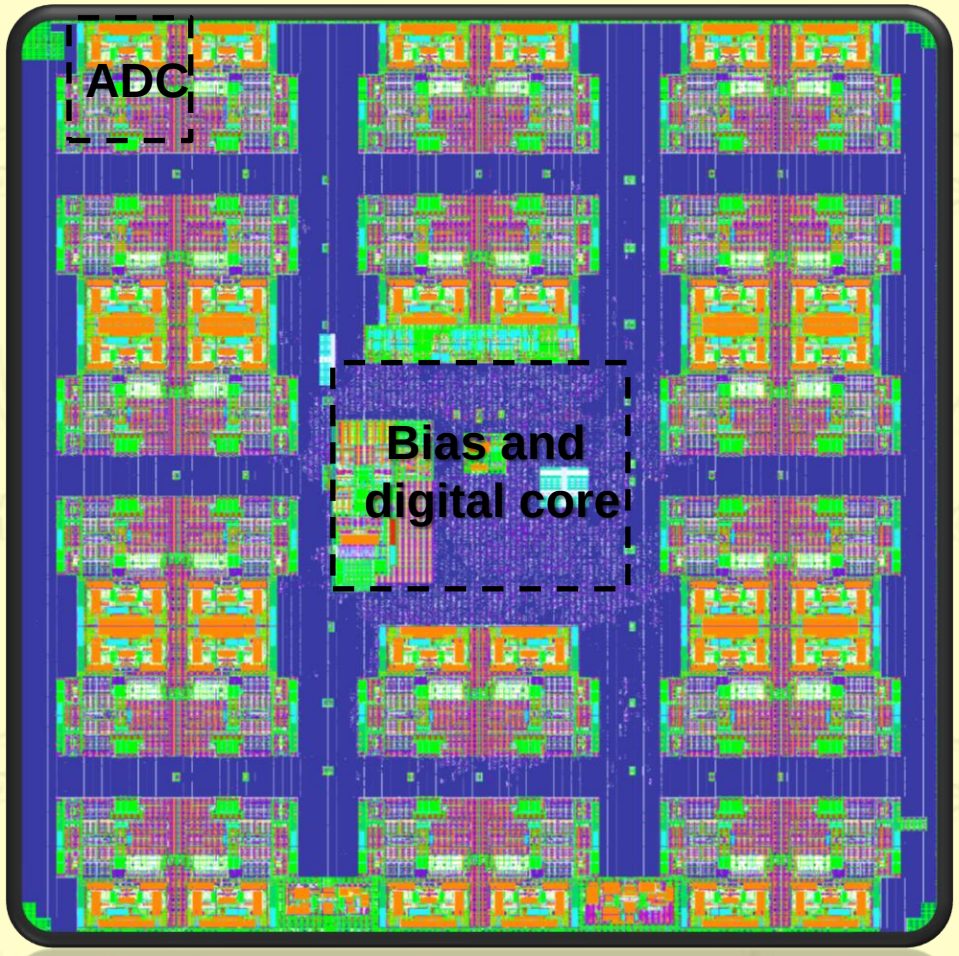




ASIC TOP LEVEL LAYOUT:



TESTING RESULTS: ADC OUTPUT SPECTRUM

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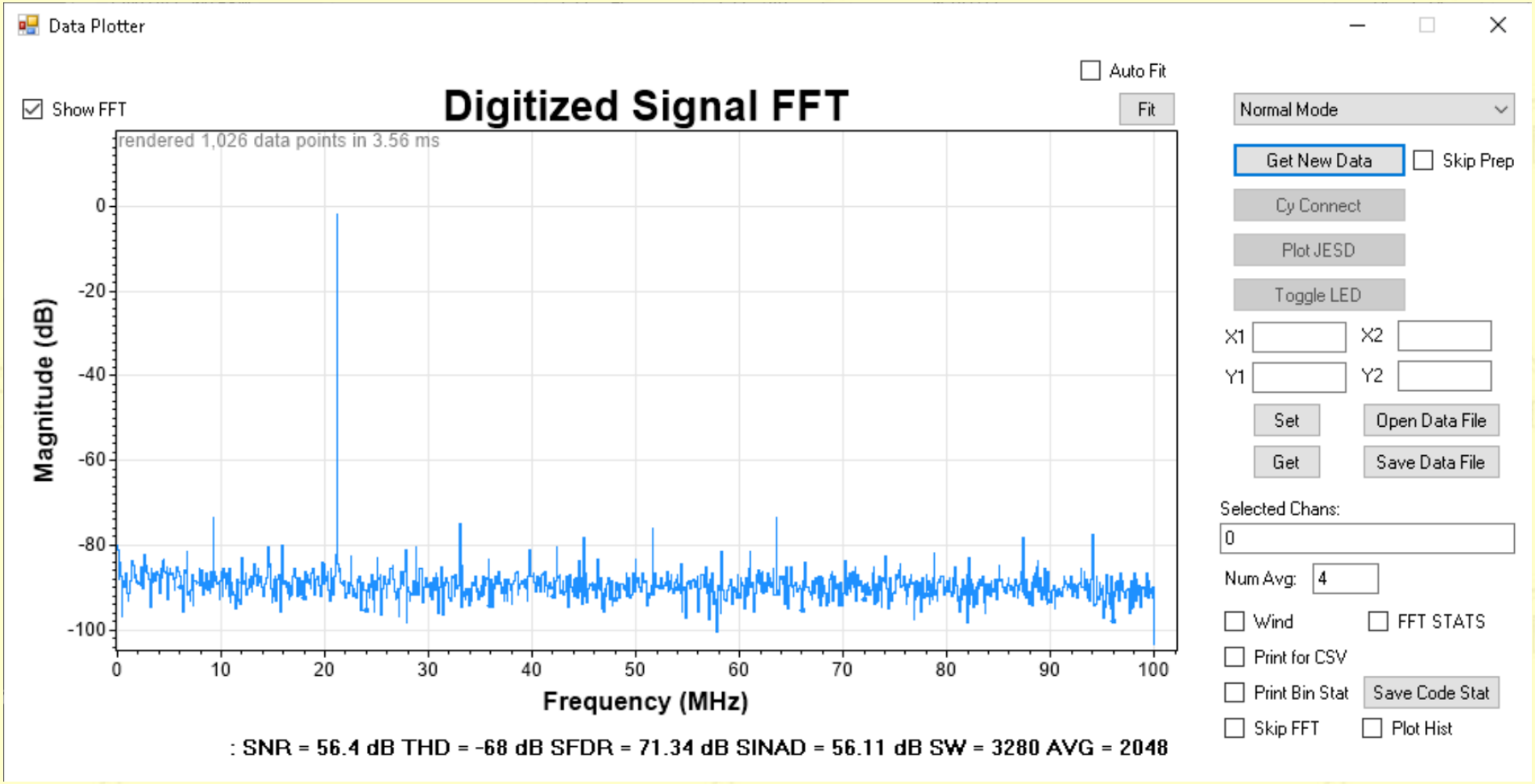
Tested: SFDR 71dB / ENOB ~9



EVENT DRIVEN DIGITAL BACKEND TEST RESULTS

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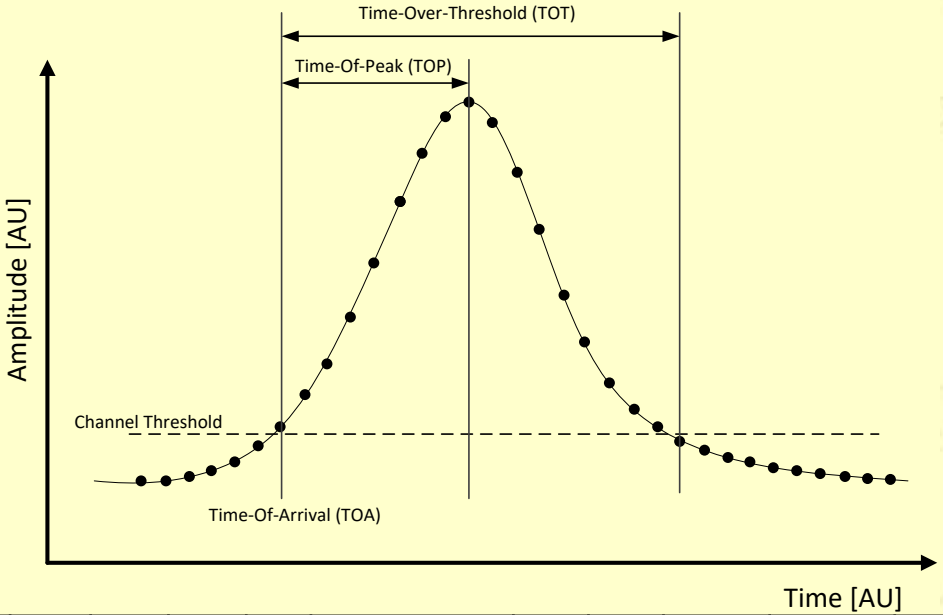
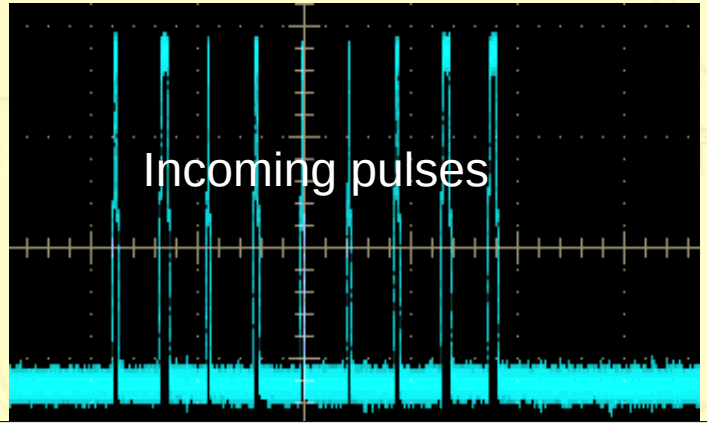
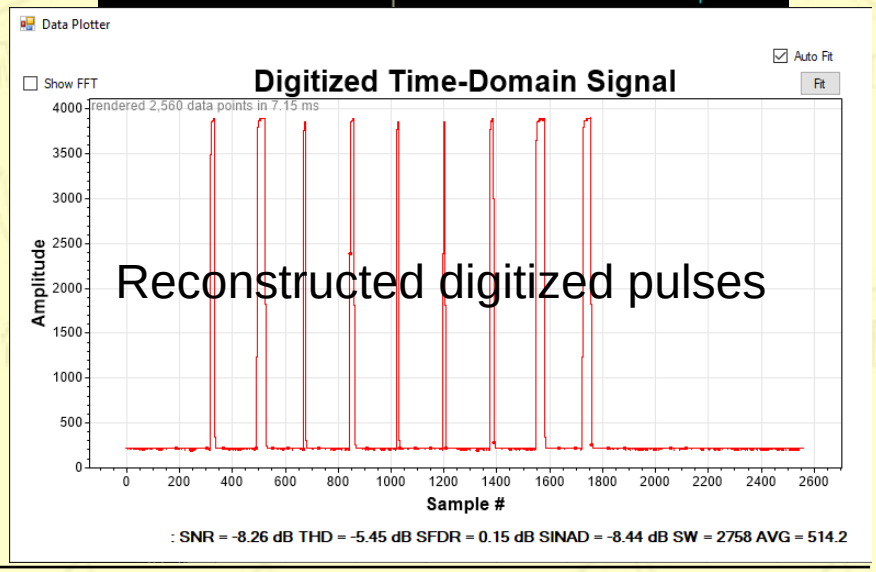
The event-driven backend was designed in collaboration with Dr. Carl Grace of LBNL. It is capable of extracting the TOT, TOP, TOA, and the peak amplitude of incoming pulse signals.







Par0	Event	Fixed	Wind	CH	TOA	TOP	TOT	PEAK	THRESHOLD	SHARED
1	1	3	64	4	578680317105	13	17	3893	1024	0
1	1	3	64	4	578680317281	11	33	3893	1024	0
1	1	3	64	4	578680317457	6	9	3861	1024	1
0	1	3	64	4	578680317633	13	17	3893	1024	1
0	1	3	64	4	578680317809	6	9	3861	1024	2
1	1	3	64	4	578680317985	6	9	3861	1024	3
1	1	3	64	4	578680318161	14	17	3893	1024	3
1	1	3	64	4	578680318337	14	33	3893	1024	4
0	1	3	64	4	578680318513	31	33	3904	1024	5

PHASE IIB PROJECT OBJECTIVE

The performance parameters of the 1st generation ASIC are required to be improved in order for the device to be used commercially. Several design mistakes were identified during the chip testing and must also be addressed within Phase IIB in the 2nd generation ASIC and the evaluation PCB.

Phase IIB objective:

- Fix issues discovered during 1st generation ASIC evaluation.
- Fabricate the redesigned chip (2nd generation).
- Package the chips.
- Update the design and fabricate new PCB.
- Test and characterize the 2nd generation ADC ASIC.
- Prepare updated datasheet and evaluation board for marketing.
- Submit deliverables to the DoE.

MODIFICATIONS for the 2nd GENERATION ASIC

Pacific MicroCHIP Corp.

1. Improve the ADC ENOB value from approximately 9-bit (1st generation ASIC) to at least 10-bit (required).

2. Make an offset calibration FSM to account for the 3 MSBs of the ADC output code.

3. Update the RISC CPU core program memory which has deficiencies.

4. Build in a feature for scaling down the DSP clock frequency proportionally with the divided clock frequency.

5. Separate offset compensation DAC outputs as they currently are shorted together.

6. Improve the PSRR for the clock duty cycle adjustment block.

MODIFICATIONS for the 2nd GENERATION ASIC

Pacific MicroCHIP Corp.

1. Improving the ENOB value from approximately 9-bit (1st generation ASIC) to at least 10-bit (required).

Improvement No	0.8V ref voltage	1.2Vpp input	Improve unit cell CDAC	Improved comparator	2-bits CDAC redundancy	ADC ENOB (bit)	ADC SNR (dB)	ADC SFDR (dB)
1	x	x	x	x	x	9.448	59.45	69.57
2	√	x	x	x	x	9.624	59.55	71.08
3	x	√	x	x	x	9.894	61.06	73.93
4	x	x	√	x	x	9.668	59.71	71.36
5	x	x	x	√	x	9.935	62.04	73.79
6	x	x	x	x	√	9.6	60.05	71.92
7	√	√	√	√	√	**10.56**	**66**	**74.81**

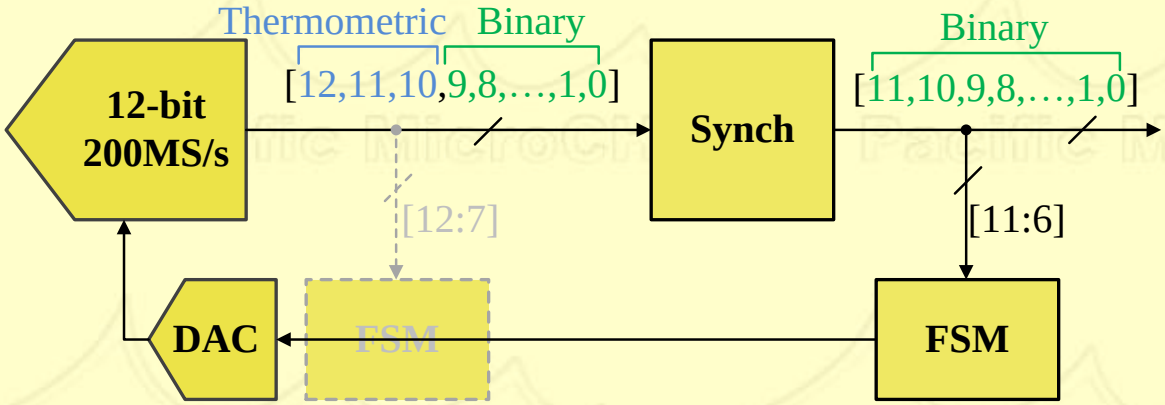
ENOB was improved up to 10.56-bit (in pre-layout simulation) by applying all 4 improvements: 1) Increase reference voltage, 2) Increase CDAC switch size, 3) Improve comparator noise, 4) Add 2-bit redundancy.

The comparison between SNR and SFDR indicates that the noise is still the limiting factor for ENOB.

MODIFICATIONS for the 2nd GENERATION ASIC

Pacific MicroCHIP Corp.

2. Make offset calibration FSM to account for the 3 MSBs of the ADC output code.



The original FSM processes the raw data coming out of the ADC including 3 MSB thermometer coded instead of binary.

The FSM was later decided to be placed after the synchronizer circuit which converts the 3 thermometric MSB bits to 2bit binary. The proposed fix employs [8:3] bits that are not changed at synchronizer block. This solution has been simulated, and the results confirmed correct operation.

3. Update the RISC CPU core program memory which has deficiencies.

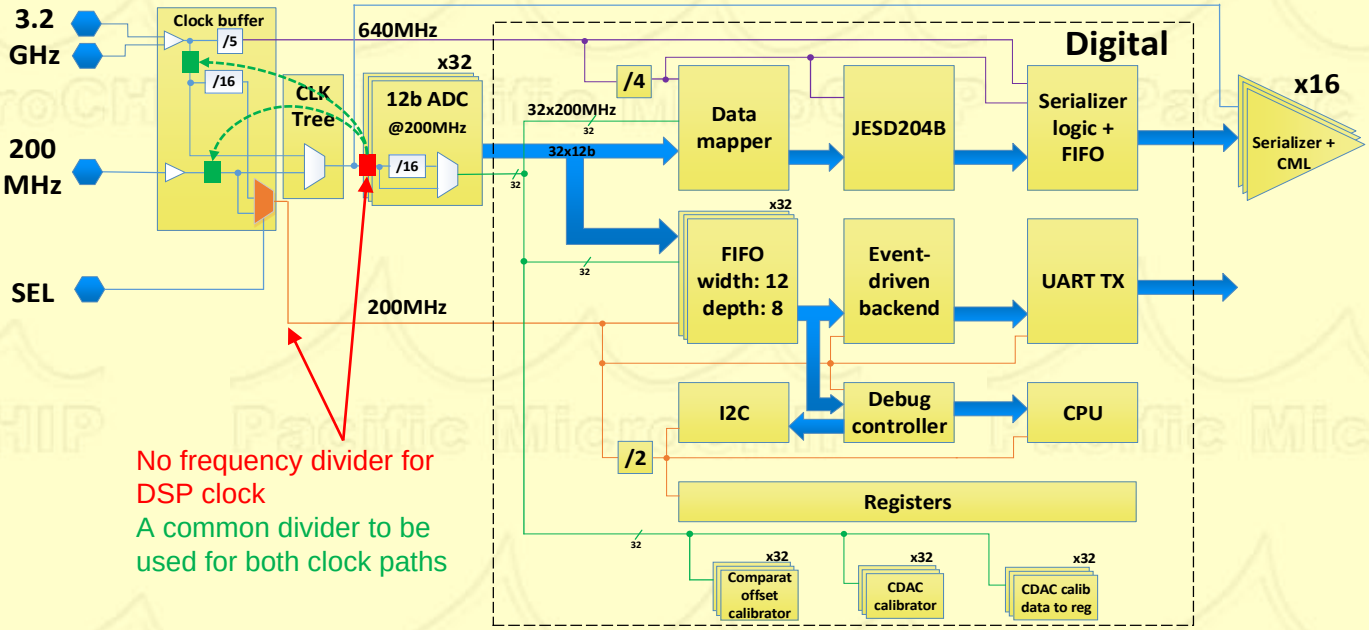
An older CPU with a bug was implemented on the ASIC. The bug prevents the CPU from executing the first instruction properly and to read back the program memory through the I2C interface after writing it. The updated CPU will be implemented.

MODIFICATIONS for the 2nd GENERATION ASIC

Pacific MicroCHIP Corp.

4. Build in a feature for scaling down the DSP clock frequency proportionally with the divided clock frequency.

An ADC sampling clock frequency divider is built into the clock distribution network of the ASIC. However, the frequency of the clock going to the DSP is not scaled down proportionally with the divided clock frequency.



Thus, using any other than default clock frequency division option makes the pulse detection to malfunction. An equivalent frequency divider has to be implemented for the digital clock.

MODIFICATIONS for the 2nd GENERATION ASIC

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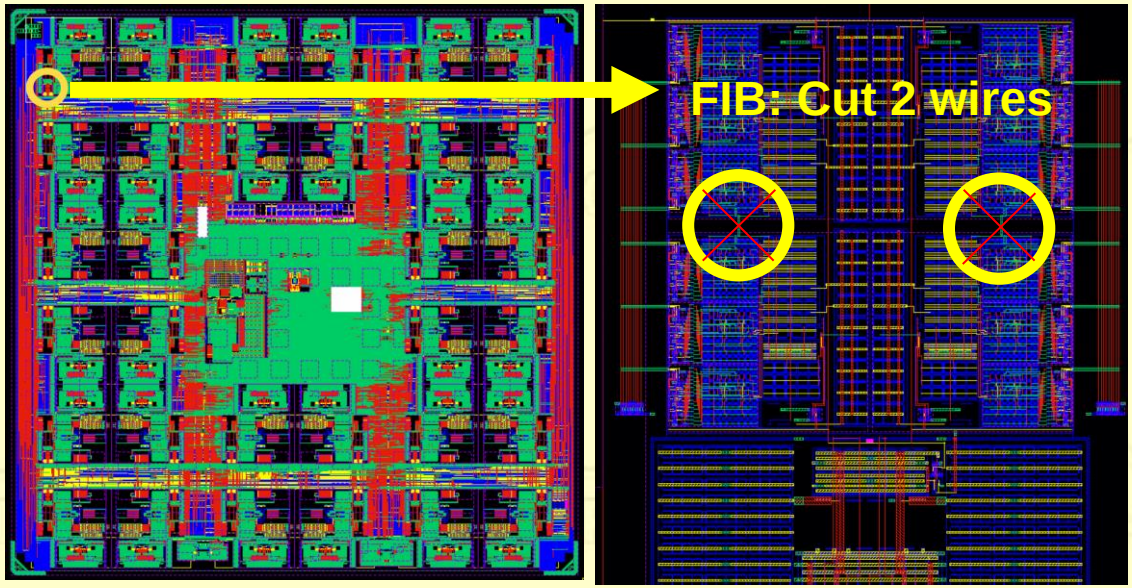
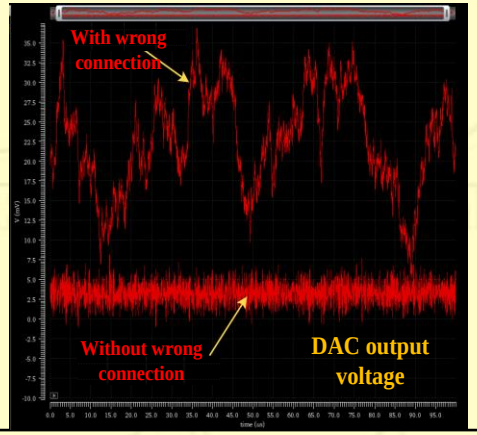
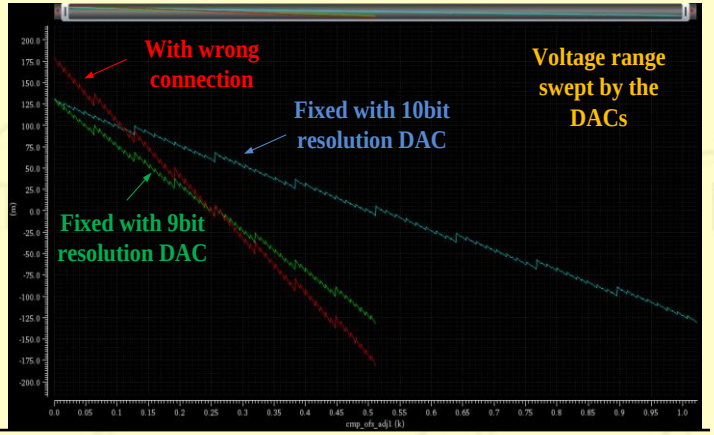
5. Separate offset compensation DAC outputs (shorted together in 1st generation ASIC).



To fix the issue, we introduced two modifications. The first was to remove the wrong connection between the two DACs. It was verified by performing the FIB.

The second modification was to increase the resolution of the DAC from 9bit to 10bit, improve offset cancellation precision by reducing the offset compensation step.





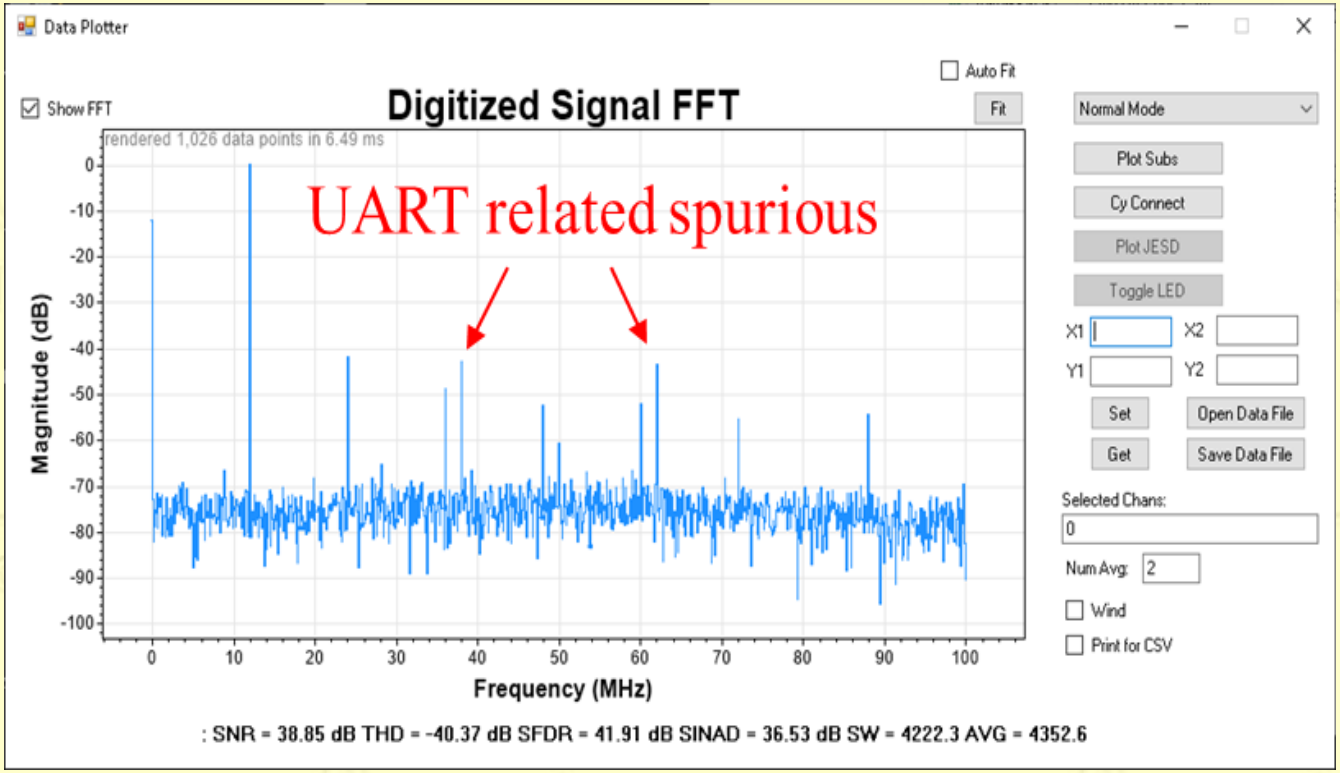
MODIFICATIONS for the 2nd GENERATION ASIC

Pacific MicroCHIP Corp.

6. Improve the PSRR for the clock duty cycle adjustment block.

It was discovered that two spurs are introduced on the ADC output signal spectrum. These spurs are detected at the input signal frequency ±50MHz (the clock frequency of the UART). Figure shows measured ADC output spectrum for 12MHz input signal while the UART is enabled.

Further analysis showed that the supply voltage used for ADC local clock generator, is shared with the UART block. As a result, the 50MHz clock modulates the sampling clock. This issue was fixed by separating the supply voltage of the two blocks.



PHASE IIB PROJECT SCHEDULE

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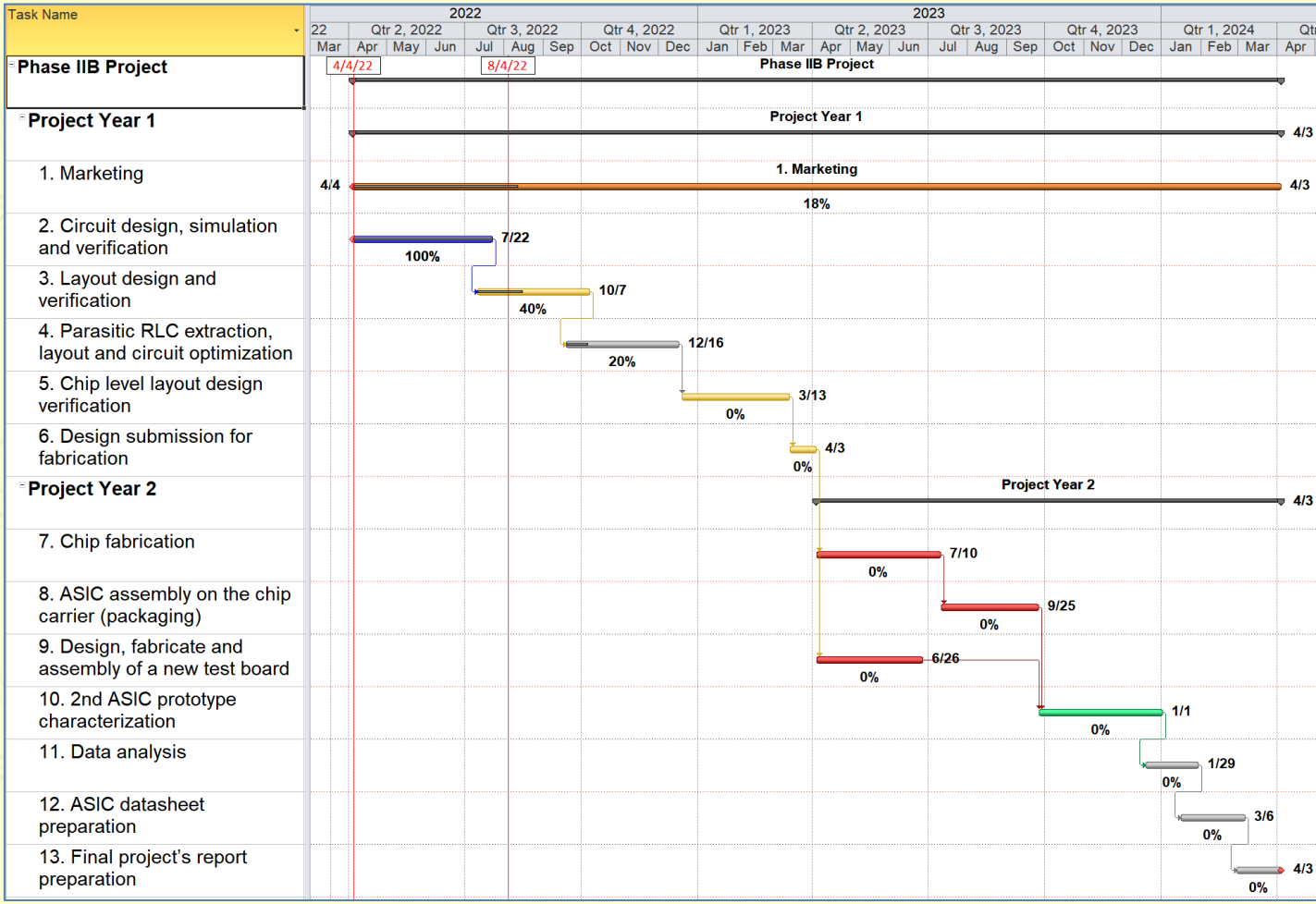
Project status:

- Circuit design, simulation and verification done.
- We are slightly ahead the schedule.
- The project is expected to be completed as planned - by 04/03/2024.



FUTURE PLANS

Pacific MicroCHIP Corp.

- Finalize layout changes.
- Run ASIC top level verification/simulation.
- Fabricate redesigned ASIC.
- Package fabricated die.
- Produce new test PCB.
- Test/characterize the produced 2nd generation ASIC.
- Start shipping the ASIC parts to select customers.

THANK YOU!

Application Ideas for the ADC ASIC are appreciated!