TELLURIC LABS
Tempus Est

Continuous Flow Time and Trigger DAQ

DWDM Tb Photonics Integrated Circuit for Continuous Readout

Award DE-SC0019581

Presented to
DOE SBIR STTR Exchange Meeting 2021
August 19, 2021

Radu Radulescu
Telluric Labs

TELLURIC LABS
Tempus Est

CF TTDAQ Target Goals

- Photonic Integrated Circuit (PIC) 64 DWDM channels at 25Gbps (1.6 Tbps) bidirectional per fiber (two orders of magnitude increase in readout bandwidth for continuous readout0
- Radiation tolerant. Remotely illuminate by lasers outside radiation area
- Both linear and digital signal transport compatible – direct electo-optic conversion.
- Use of high density 5G modulation techniques.
- In-band asynchronous timing synchronization over plaint COTS links (GTS protocol)
- FPGA based pS timestamping for signals and network traffic (ETDC)

Functional blocks:

- DWDM Photonic Integrated Circuit Modulator/Demodulator;
- IPAG FPGA board (, ETDC, 25G GTY serdes, switch, zero suppression, user signal processing blocks) ;
- GTS synchronization protocol.

Features

- PIC novel architecture works with the 100Ghz and the 50GHz ITU lambda grid without cross talk.
- 3.2 THz Free Spectral Range (FSR)
- Continuous readout eliminating data storage at FE for later readout.
- No HW trigger. No HW for timing distribution. Any computer with an FPGA NIC can be synchronized.
- Timestamps are numerically re-timed and synchronized, without timing control hardware, through the nonintrusive GTS protocol.
- Power consumption of less than 10W.

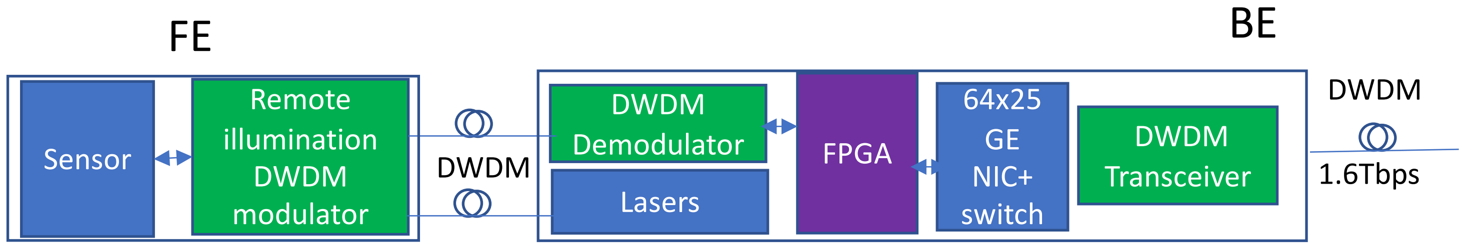
Benefits

- SW classification allows parallel independent triggers for parallel experiments.
- Substantial reduction of digital electronics in high radiation area. Complexity migrates to lower cost, higher performance COTS BE, avoiding lengthy radhard ASIC development.
- Faster and lower cost construction of detectors.
- Shorter experimental time – all trigger and experiment setup is in SW, higher timing accuracy.
- Seamless integration of any user subsystem through SW retiming of collected data.

TELLURIC LABS
Tempus Est

DWDM Tb Photonics Integrated Circuit for Continuous Readout
Structure and Network Topology

DWDM Photonic Integrated Circuit (PIC) is using MicroRing Resonators for both Modulators and Detectors.
The PIC will work in unidirectional, fractional duplex, or full duplex with an aggregated bandwidth of about 1.6 Tbps per fiber.
Two PICs can be connected in daisy chain to double the number of channels per fiber.
The PIC as 248 pads at a double, interleaved, 75um pitch rows for wire bonding.



Current commercial solution for transceivers having locally integrated lasers

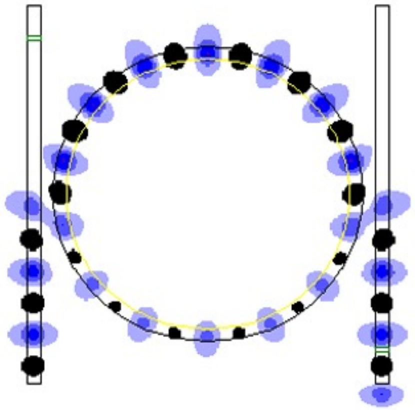
DML (directly modulated laser , VCSEL 850nm ~100m)
PAM/QUAM – High frequency linear electronics
EML (externally modulated laser) – local CWL
MZM (Mach Zehnder Modulator)– high voltage, lengthy (>1mm)
GPON - local laser, external mux

Some specific advantages of the microring resonators:

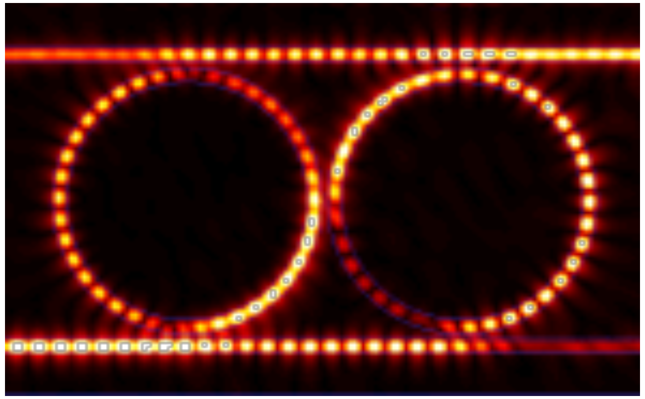
Lowest power
Native wavelength filtering (including add drop)
High sensitivity
Tunable across wavelength spectrum (both in temperature, and voltage)

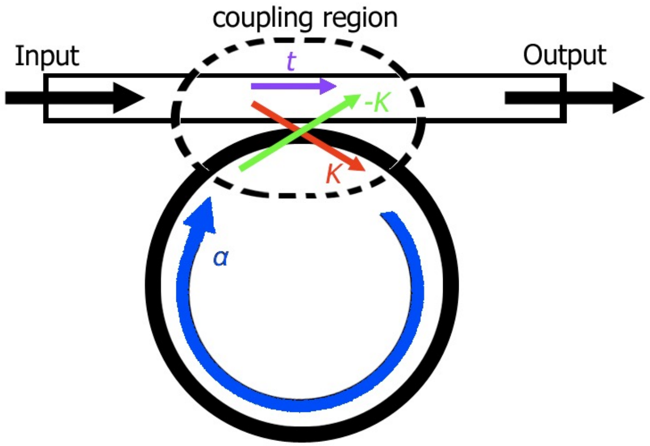
MICRORING RESONATORS

Band reject filter **Band pass filter**



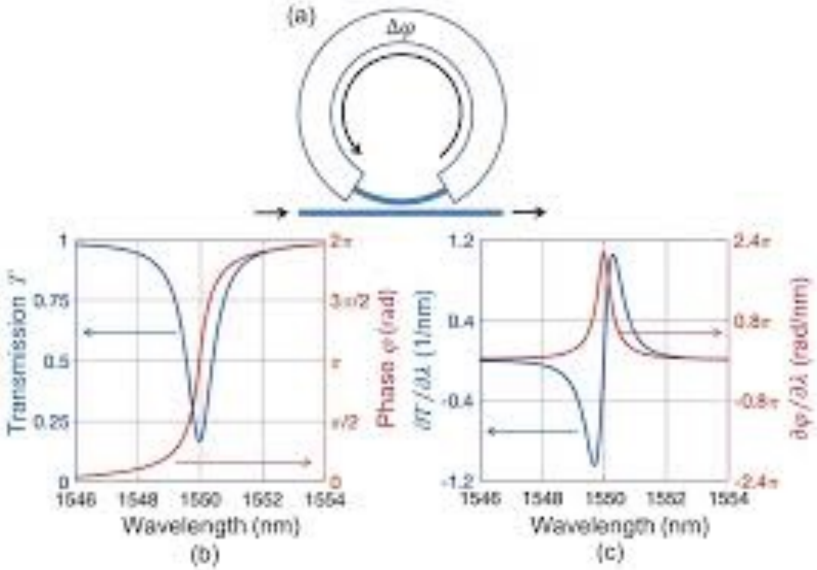
Add drop topology





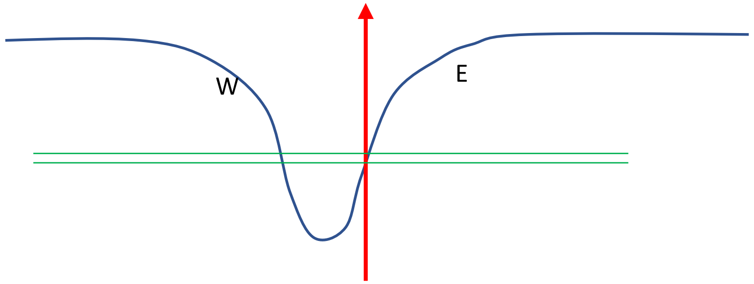
Band reject filter

Through topology

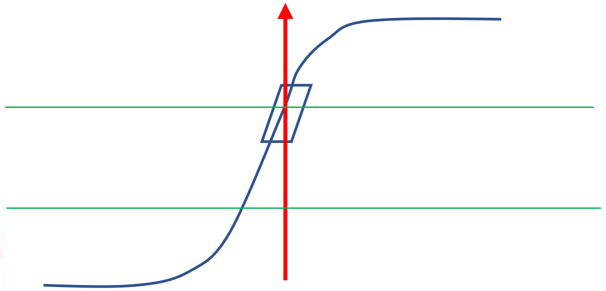


Animated RAMZI MRR modulation principle (~10GHz/V)

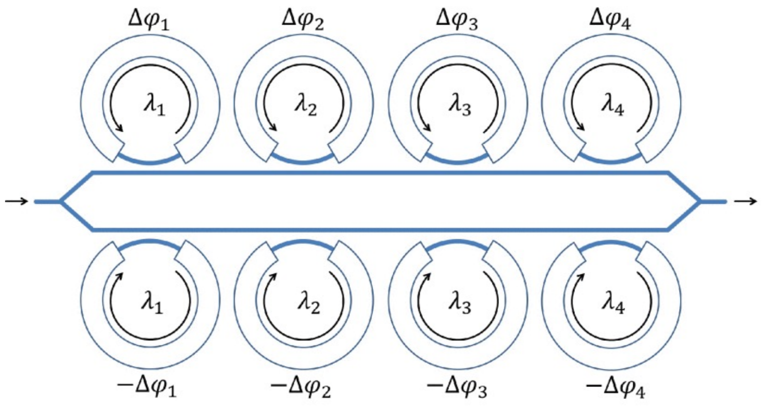
Amplitude Modulation



Phase Modulation



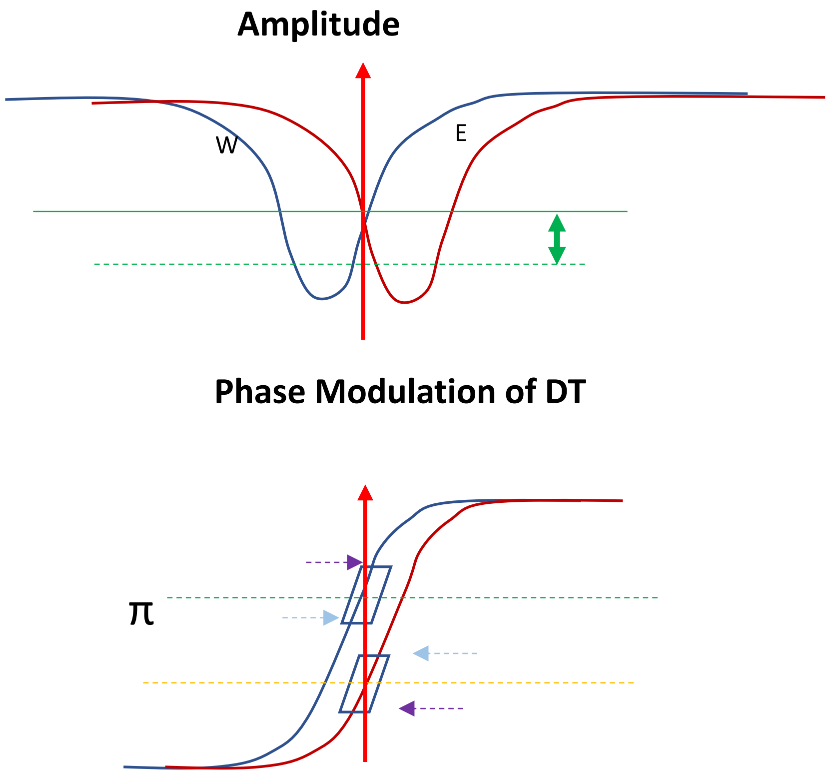
RAMZI modulation



Differential RAMZI – analog modulation

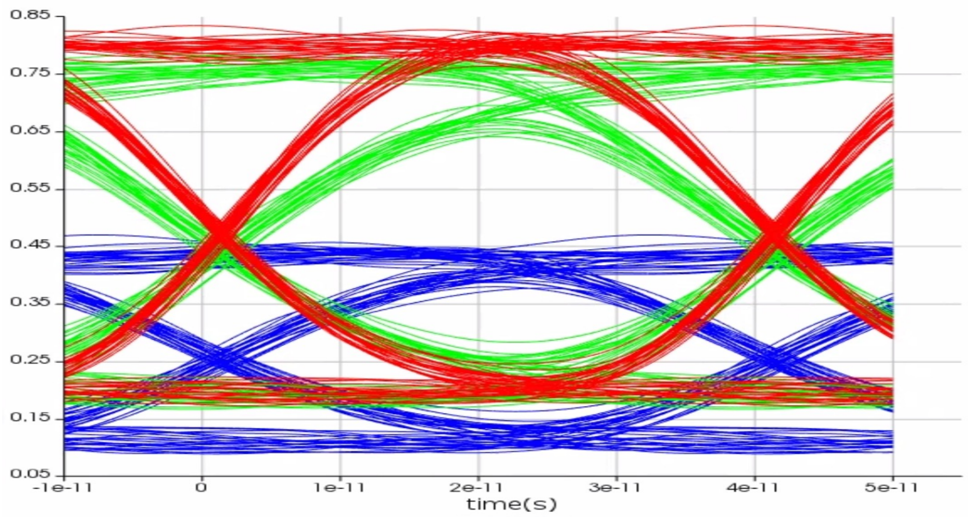
https://ieeexplore.ieee.org/document/8540485

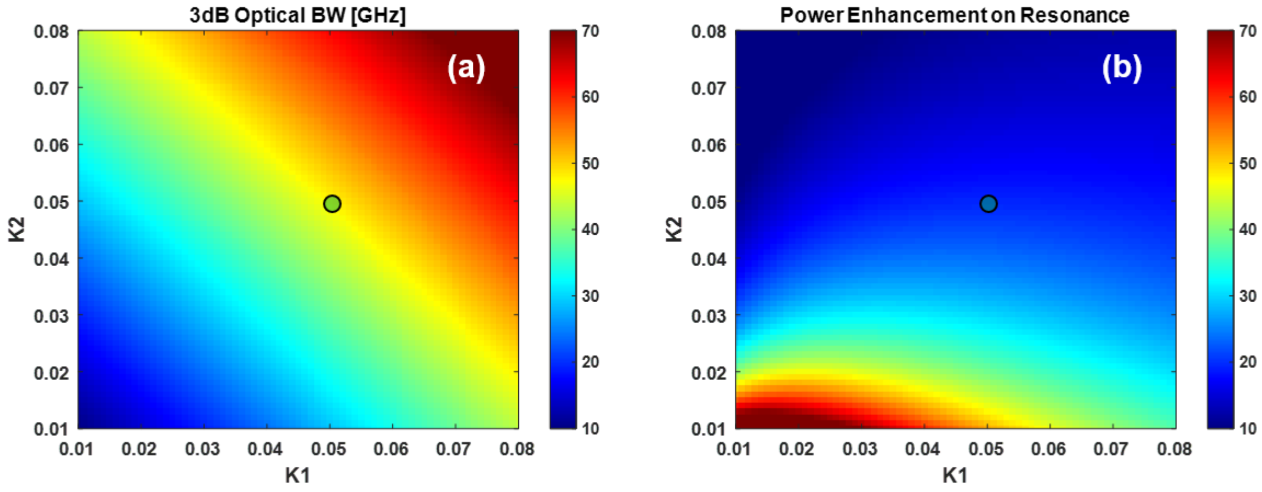
Animated RAMZI MRR modulation principle (~10GHz/V)



TELLURIC LABS
Tempus Est

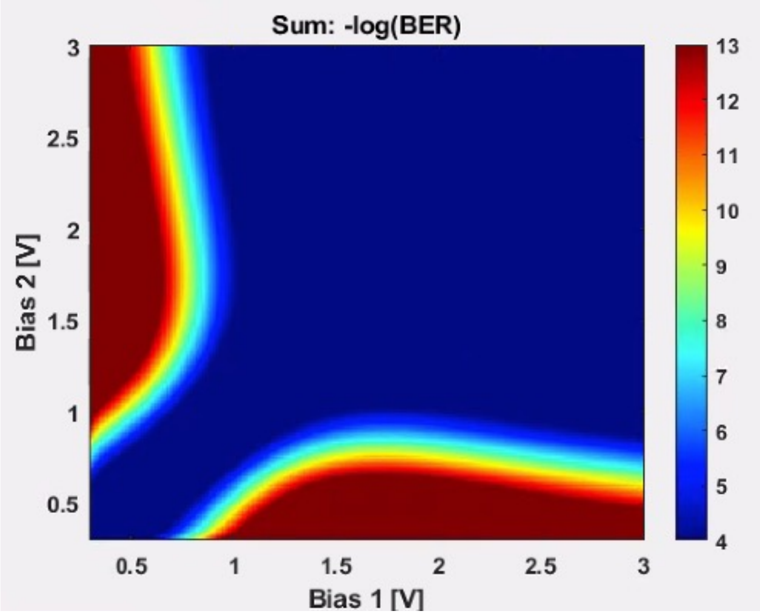
RAMZI differential modulation efficiency simulation



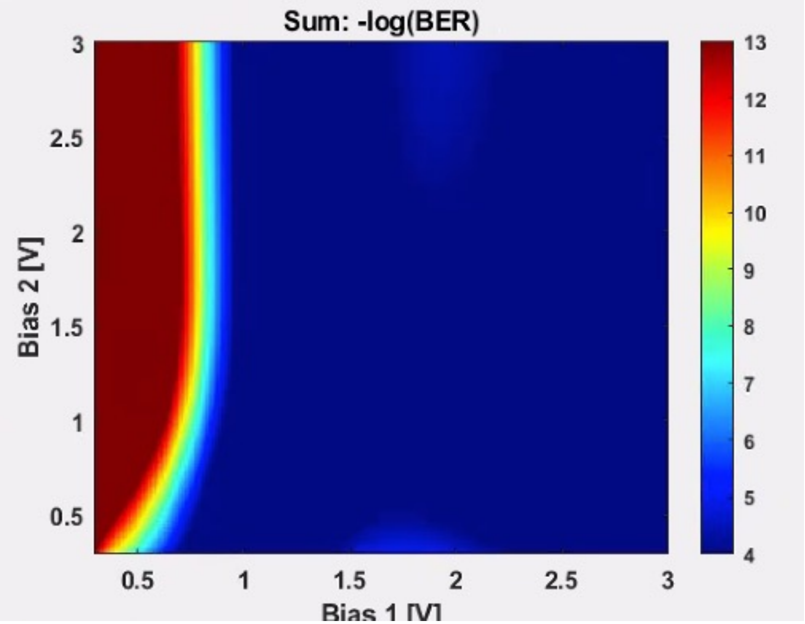


We simulated several circuit topologies for the differential modulators (comprising a North(N) and a South(S) ring resonator modulators (RRM)) and analyze the eye diagrams. Here is an example

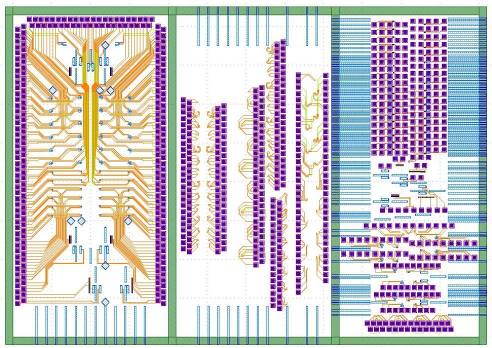
(a) Optical FWHM bandwidth as a function of the power coupling coefficients for a passive add-drop ring. (b) Power enhancement factor as a function of the power coupling coefficient



Optimal operating range for bias voltage



Tb PIC STATUS



PICs are currently being tested.

The device was developed in partnership wit MIT LL and manufactured at a US foundry

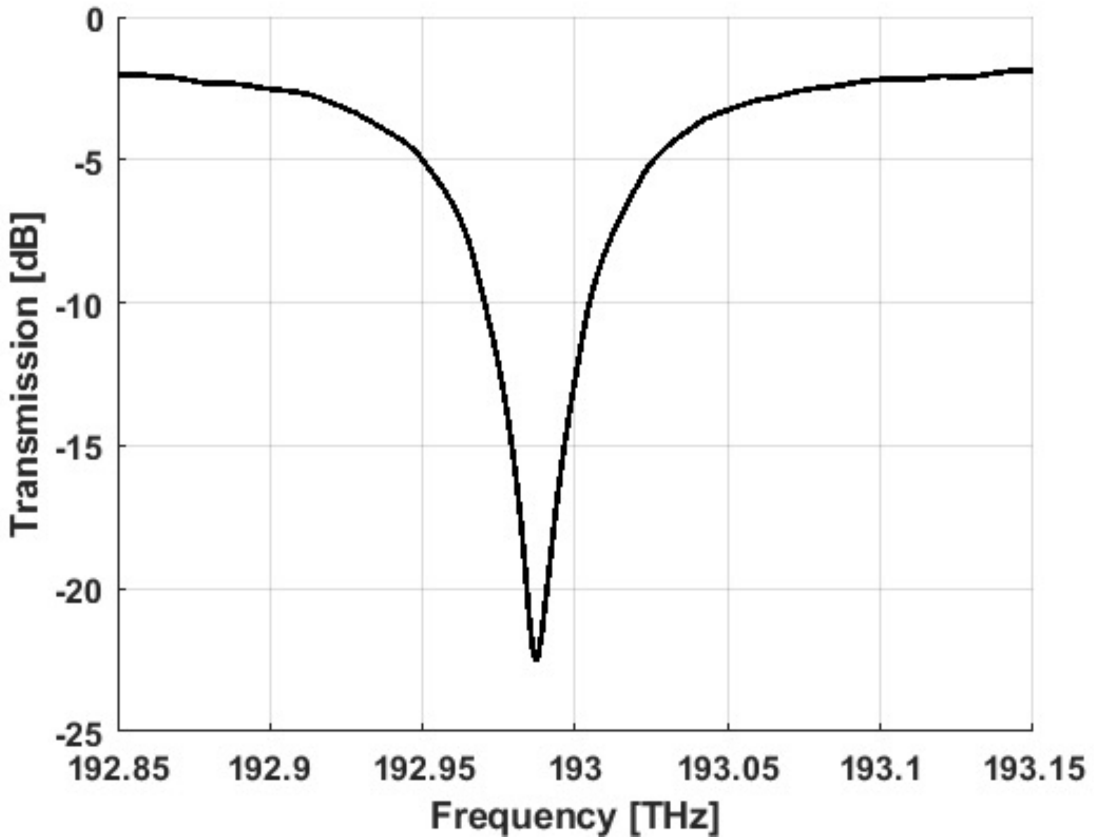
We split the 6x4 mm die surface into three 4x2mm chiplets comprising

1) the first spin of Prometheus transceiver (12 differential Transmit and Receive DWDM channels),
2) a simplified intermediate complexity transceiver testing several new four channels architectures and components, and
3) a basic components chiplet comprising all individual components of Prometheus from the foundry PDK, and alternative new implementations of microring modulators designed by Lincoln Laboratory.

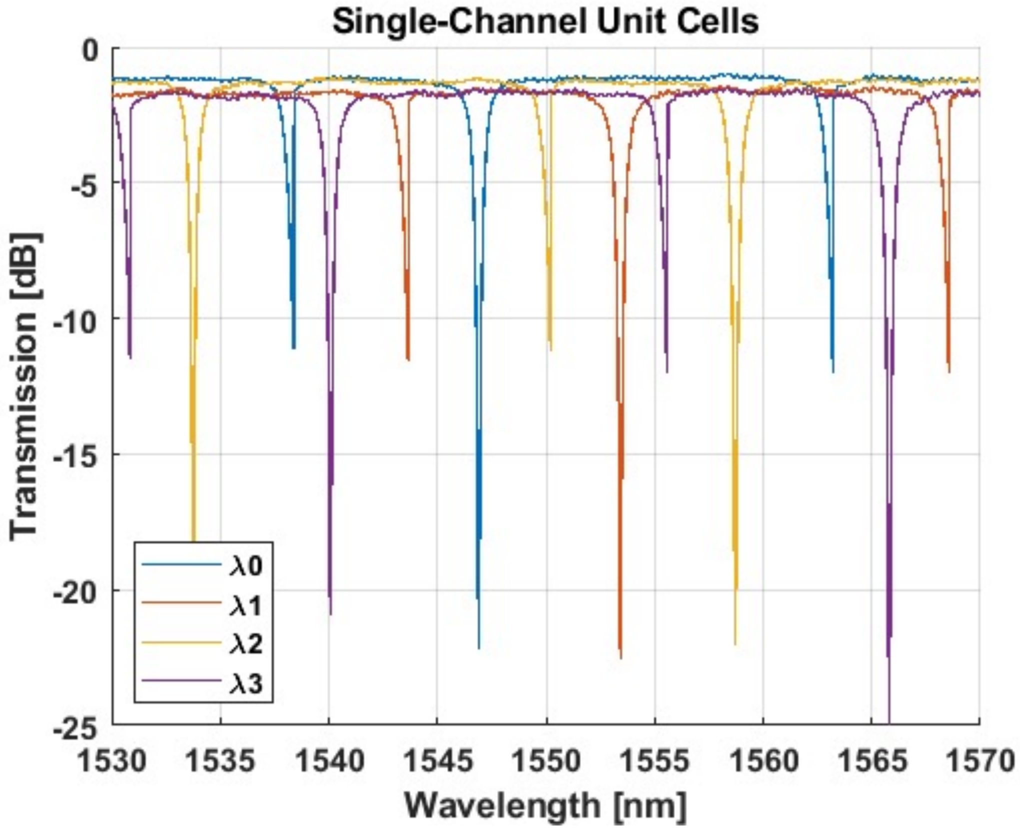
There are hundreds of photonic components that have to be tested either individually or in a functional block.

Current optical tests confirmed the expected characteristics of the waveguides, splitters, modulators, and photodetectors.

TEST RESULTS
DWDM Tb PIC



Detail MicroRing optical characteristic

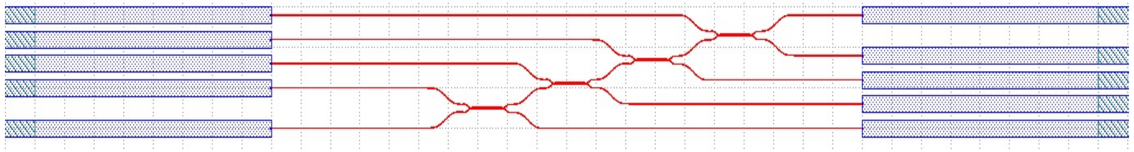


Free Spectral Range (FSR) = 3.2 THz
Thermal shift tuning

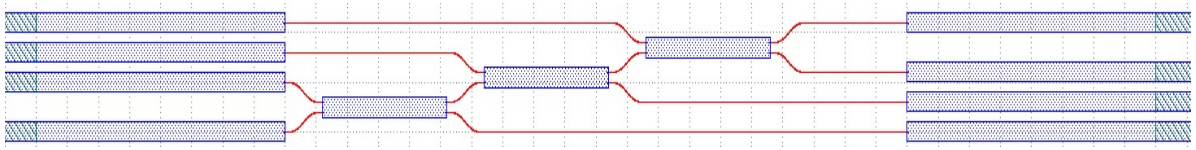
TELLURIC LABS
Tempus Est

Several tested photonics components circuit

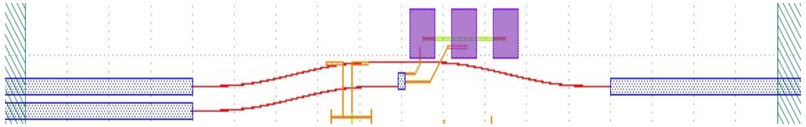
80/20 Splitter Test



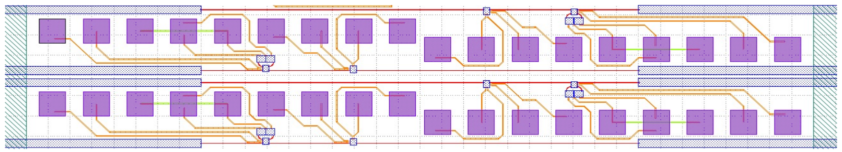
3dB Splitter Test



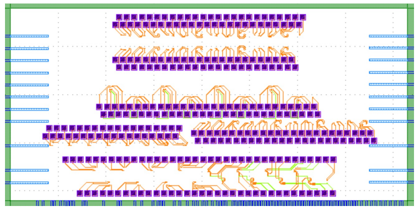
Photodiode



Single-Channel Modulator + Demodulator Test



Other proprietary components



The second chiplet contains a variety of transceiver architectures with four wavelength channels, in multiple configurations. These circuits provide risk mitigation for the “hero circuit”, consisting of fewer components and less complex architectures, as well as a more conservative channel frequency spacing so as to reduce the effects of crosstalk

TELLURIC LABS
Tempus Est

Thank you !

For more information contact us

157 Broad Street

STE 201

Red Bank New Jersey 07701

Tel: 732-740-9017

Fax: 732-858-5827

E-Mail: info@telluriclabs.com

BACKUP SLIDES

APPLICATIONS

Tb PIC Possible Application Example

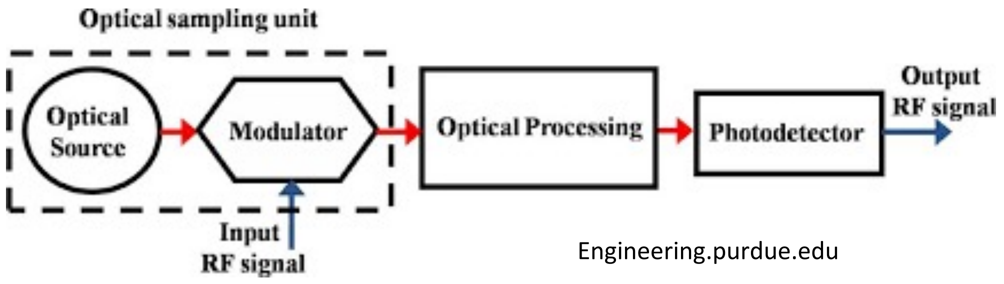
Data Center

HPC

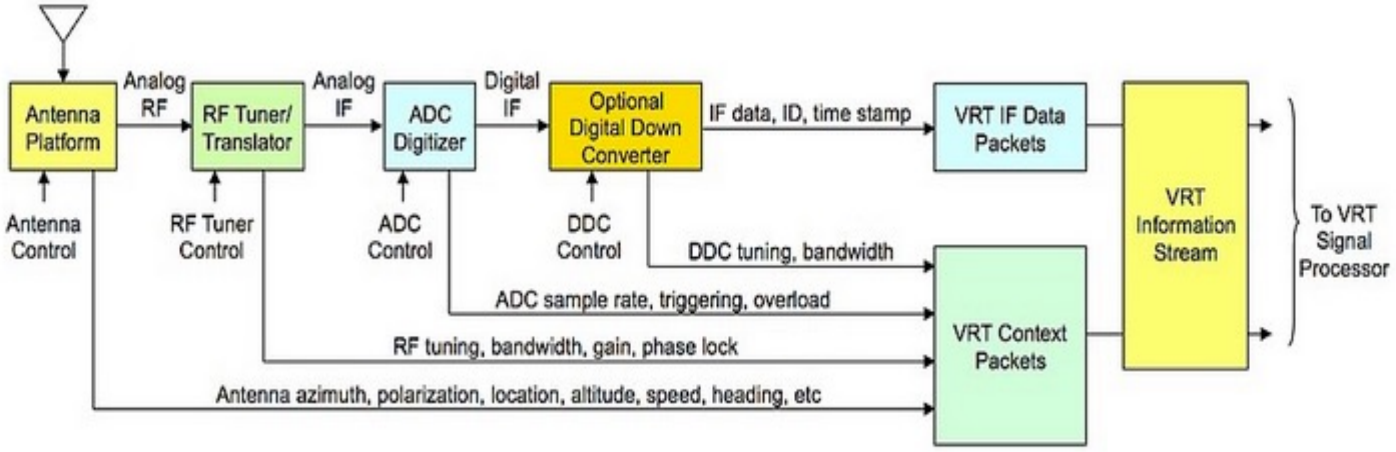
TELLURIC LABS
Tempus Est

Tb PIC Possible Application Example

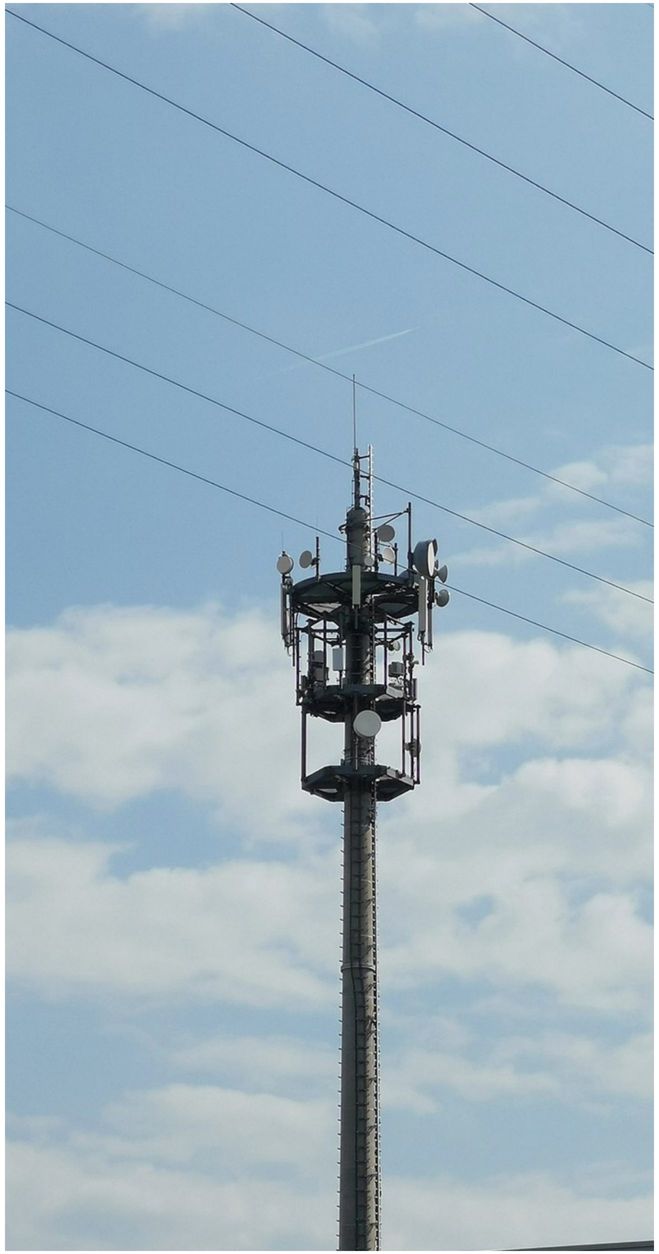
OPTICAL PROCESSING OF RF SINGNAL



Engineering.purdue.edu



Block Diagram of VITA Radio Trans-port (VRT)



5G

TELLURIC LABS
Tempus Est

Tb PIC Possible Application Example
Triggerless, Continuous Readout for BNL EIC