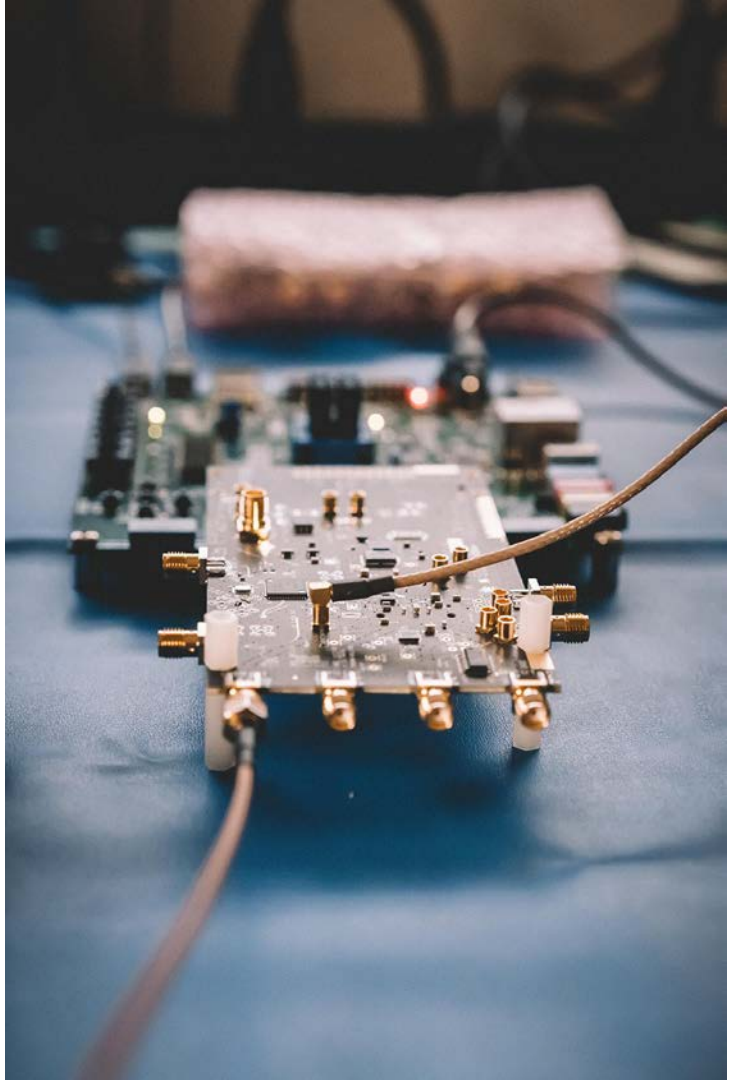


NALU SCIENTIFIC
ENABLING INNOVATION

# Design and development of the All-in-One Digitizer System-on-chip "AODS"

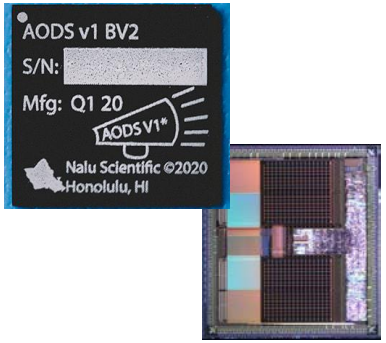
A low-cost, low power, low-noise and low channel-count Application Specific Integrated Circuit (ASIC) with a high dynamic range option.

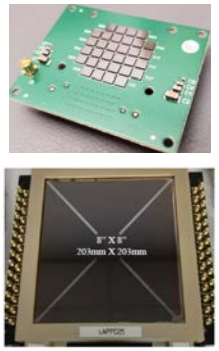
**Aug 18, 2021**
**Isar Mostafanezhad, Ph.D.**
**Founder and CEO at Nalu Scientific LLC**

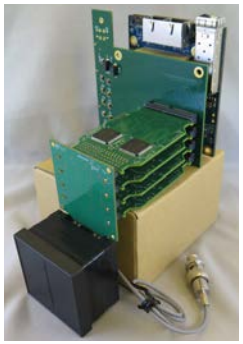
Work funded by US DOE SBIR - DE-SC0019527

NALU SCIENTIFIC
ENABLING INNOVATION

# WAVEFORM DIGITIZER SoCs
## For Precision Fast Timing Applications



### 1. Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

### 2. Integration:

- SiPM
- PMT
- LAPPD
- Detector arrays

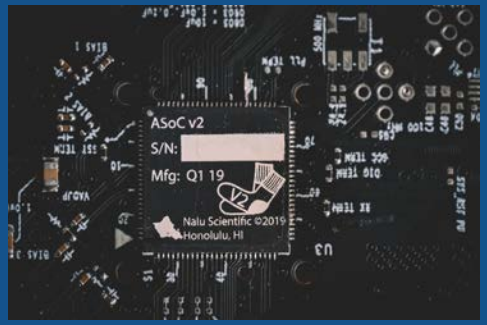
### 3a. Main application:

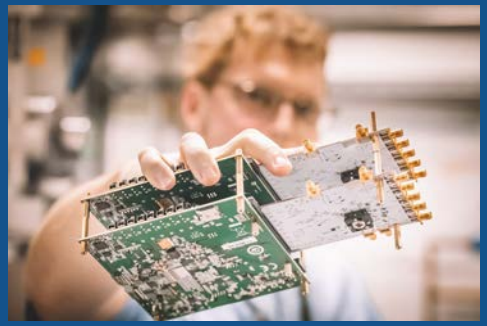
- NP/HEP experiments
- Astro particle physics

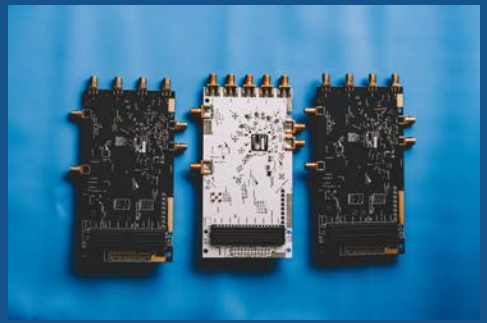
### 3b. Other applications:

- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging


2021 DOE NP SBIR PIs meeting. LAPPD photo courtesy of Incom.





# ABOUT NALU SCIENTIFIC

**Fast Growing Startup in Honolulu, Hawai'i**

- Located at the Manoa Innovation Center near U. of Hawaii
- 18 staff members
- Access to advanced design tools
- Rapid prototyping and testing lab

**Technical Expertise**

- IC design: Analog + digital System-on-Chip (SoC)
- Hardware design: Complex multi-layer PCBs
- Firmware design: FPGAs, CPUs
- Software design: GUI, analysis, documentation

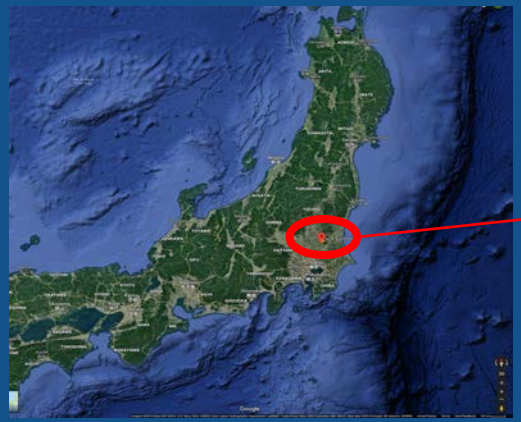
**Scientific Expertise - subject matter**

- HEP/NP particle detection and tracking
- Radiation detection
- Readout electronics for physics detectors

**Nalu = 'wave' in native Hawaiian language**

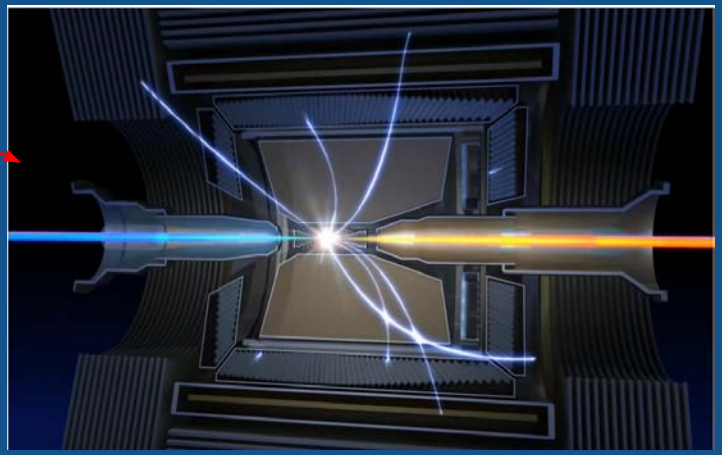
# WHERE WE STARTED

A Search for New Physics – The Belle II Experiment



**Tsukuba City**
Located 60 mi north of Tokyo

**High Energy Accelerator Research Facility (KEK)**
in Tsukuba



Interaction point inside the electron/positron collider
Source: KEK Youtube channel

NALU SCIENTIFIC
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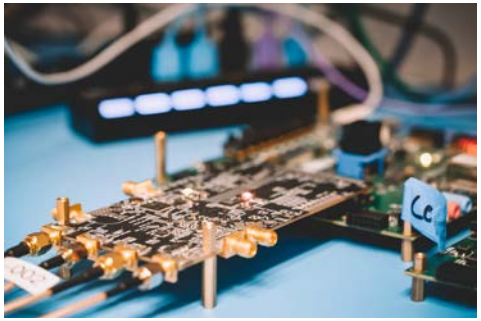
# Current SoC-ASIC Projects

| Project | Sampling Frequency (GHz) | Input BW (GHz) | Buffer Length (Samples) | Number of Channels | Timing Resolution (ps) | Available Date |
|---|---|---|---|---|---|---|
| **ASoC** | 3-5 | 0.8 | 16k | 4 | 35 | Rev 3 avail |
| **HDSoC*** | 1-3 | 0.6 | 2k | 64 | 80-120 | Sep'21 |
| **AARDVARC** | 8-14 | 2.5 | 32k | 4 | 4 | Rev 3 avail |
| **AODS** | 1-2 | 1 | 8k | 1-4 | 100-200 | Rev 1 avail |
| **STRAWZ** | 5 | 2 | 2k | 64 | 10 | Dec'22 |
| **HPSoC** | 8-10 | 2 | 2k | 64 | 4 | Dec'23 |

- **ASoC**: Analog to digital converter System-on-Chip
- **HDSoC**: SiPM specialized readout chip with bias and control
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option
- **STRAWZ:** Streaming Autonomous Waveform-digitizer with Zero-suppressio
- **HPSoC:** High Pitch digitizer SoC: AC-LGADs specific readout

* 32 channel prototype available and under test.

Work funded by DOE SBIRs. University of Hawaii as subcontractor. Commercial grade tools.

# AODS Project Highlights

**Low channel count, low cost, digitizer with daisy chain and high dynamic range options.**

**Overall technical objective:**

Functional AODS chip fabricated, tested, characterized and documented:

a. On-chip generated clocks and their associations
b. On-chip signal processing capabilities for Phase I (a simplified DSP)
c. On-chip calibration circuitry
d. Digital transceivers and failsafe mechanisms for daisy-chain operation

| Parameter | Specification |
|---|---|
| Sample rate | 1-2 GSa/s |
| Analog Bandwidth | 500MHz |
| No. bits | 12 |
| Supply Voltage | 2.5V |
| Dynamic Range | 60 dB |
| Virtual dynamic Range | 90 dB |
| Timing accuracy | <100ps |
| Gain Response | As low as 32 ns |
| Input noise | 1mV |
| Gain stages | 0dB,15dB, 30dB, (45dB) |
| Analog buffer | 16384 |
| Integration | SoC |
| Serial Rate | 500Mbps |

**Phase II technical objectives:**

1. AODS Design: it will be based on the experience gained from Phase I and will benefit from a top-down approach that will provide basis for further verification. Analog front end will guarantee programmable gain, termination and high dynamic range. Digital back end will provide dynamic range integration, digital signal processing and communication (daisy chaining) features.
2. AODS Verification: based on previously defined specifications will be separately performed on analog and digital portions and the overall chip
3. AODS Prototype Fabrication: will use well tested 250 nm technology to reduce the risk
4. AODS Evaluation PCB Design: will emphasize extensive testing of all the novel AODS features
5. Firmware/Software and testing : design and development of firmware and software to allow extensive testing of all AODS features, as well as basis for standalone use of evaluation boards by potential users.

# AODS V1 DESIGN DETAILS

## Compact, high performance waveform digitizer

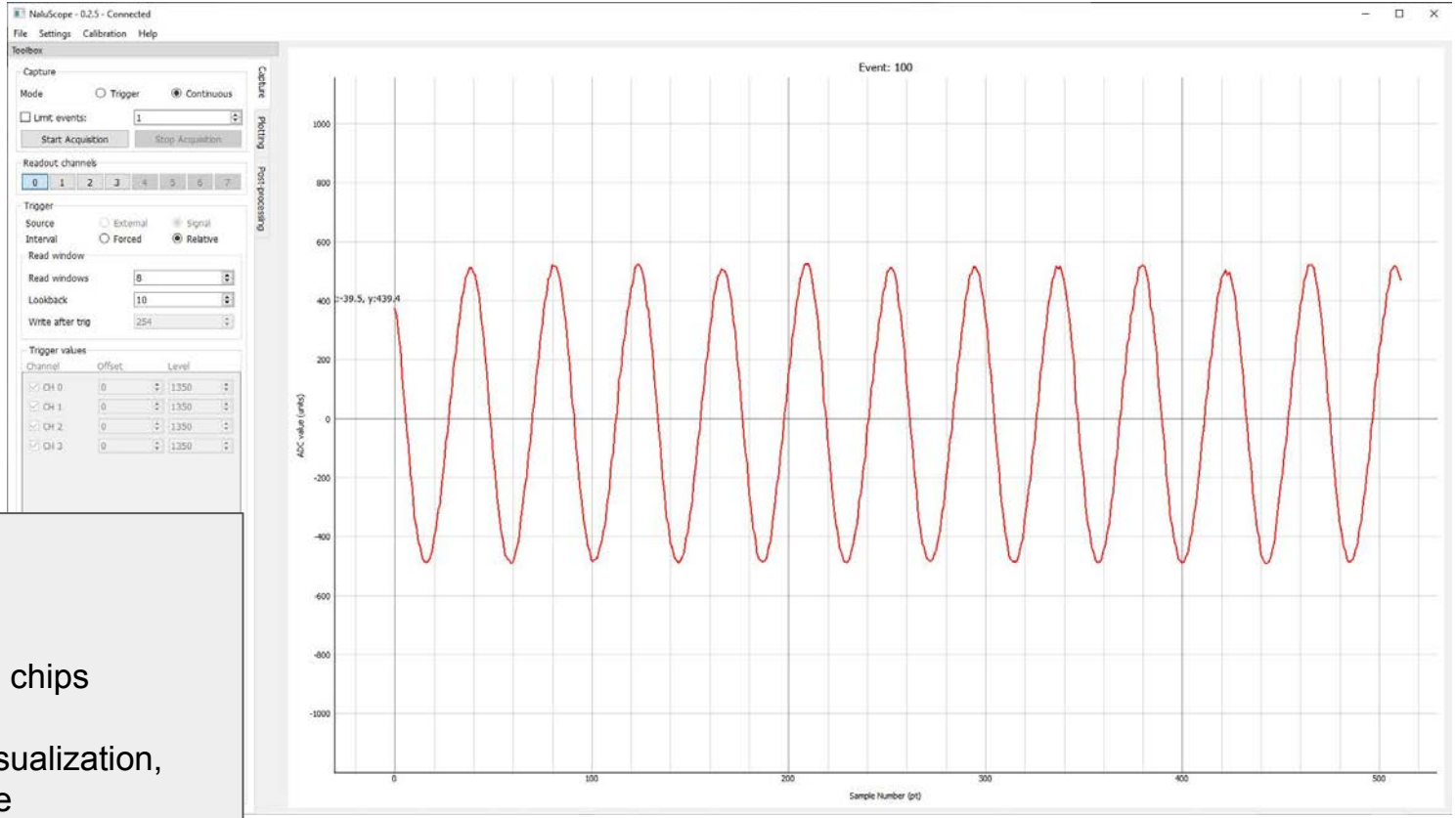
- Mid performance digitizer: 1-2 Gsa/s
- Highly integrated
- Commercially available, low cost, patented design
- 5mm x 5mm die size

| Parameter | Spec |
|---|---|
| Sample rate | 1-1.5 GSa/s |
| Number of Channels | 4 |
| Sampling Depth | 16kSa/channel |
| Signal Range | 0-2.5V |
| Number of ADC bits | 12 bits |
| Supply Voltage | 2.5V |
| RMS noise | ~1.5 mV |
| Digital Clock frequency | 25MHz |
| Timing resolution | 50-100ps |
| Power | 120mW/channel |
| Analog Bandwidth | 850MHz |
| Serial interface | Up to 500 Mb/s*** |

- Calibration memory access
- PLL on chip
- Isolated analog/digital voltage rings
- Serial interface
- High dynamic range mode
- Self triggering
- Eval cards available
- Custom boards under dev

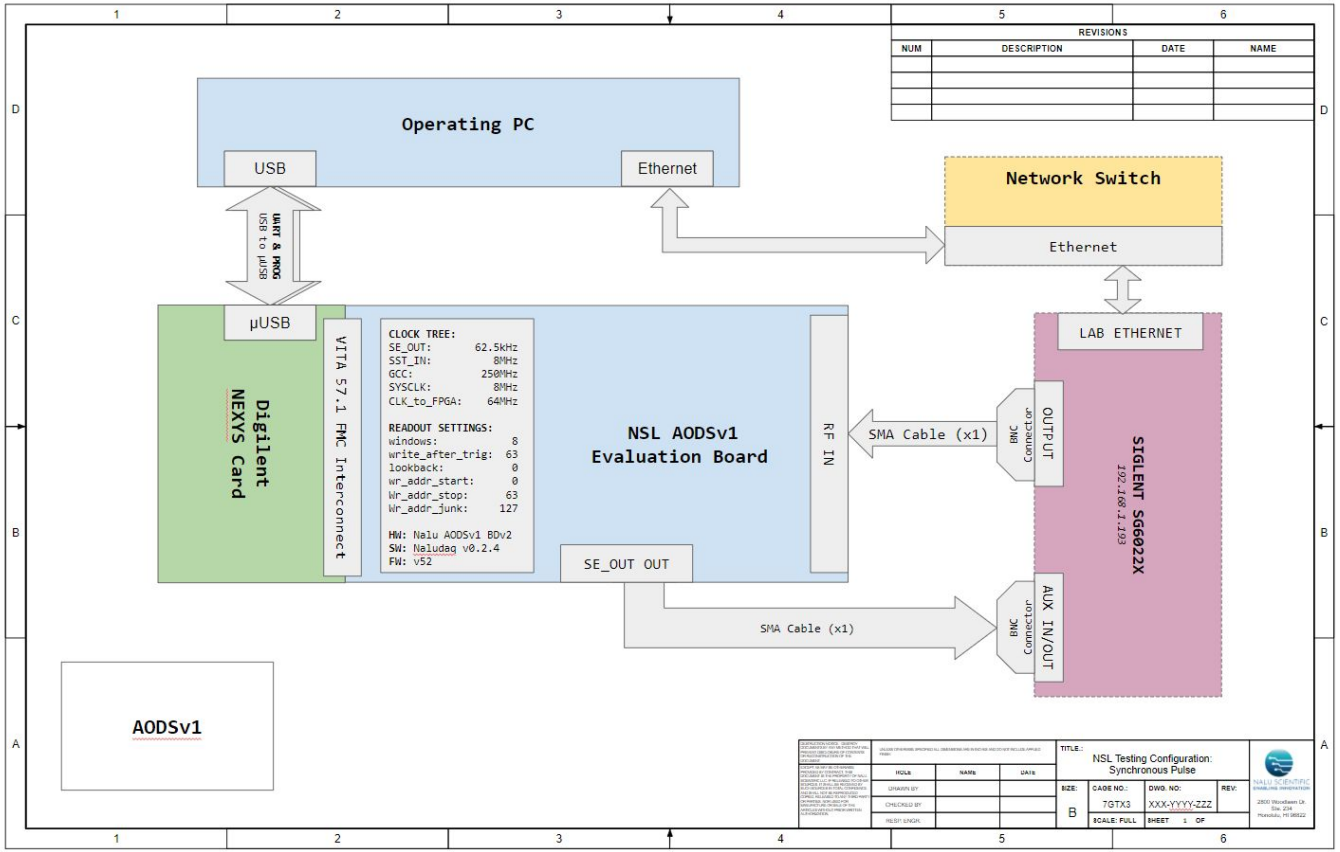
IEEE NSS 2020

# NaluScope Common Software and GUI

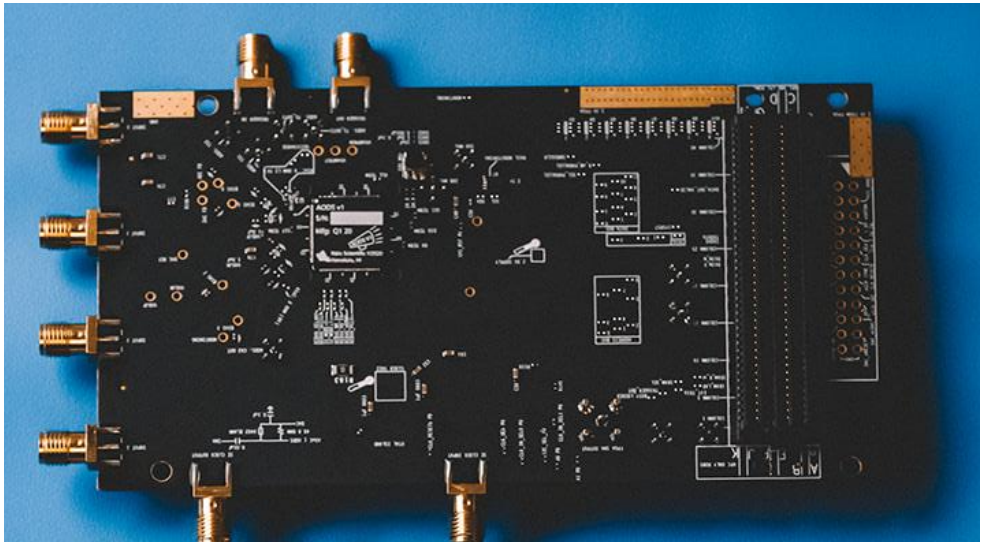


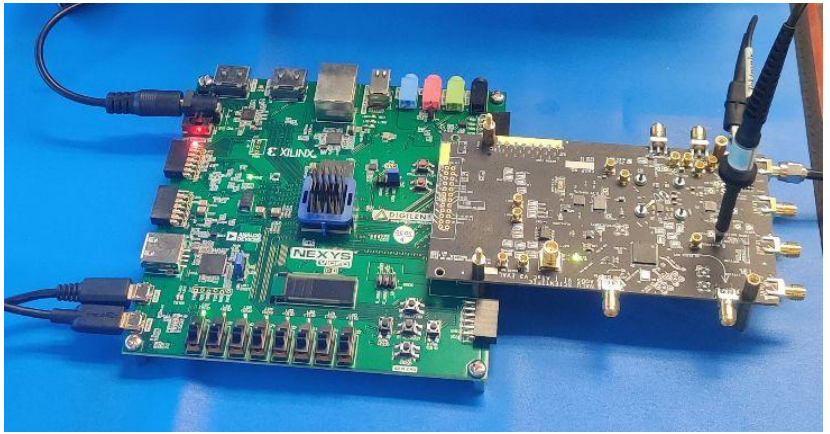

- Windows/Linux PC
- USB interface
- GUI, CLI interfaces
- Common to all Nalu chips
- DAQ configuration
- Data exploration, visualization, curation and storage

# Testing work flow

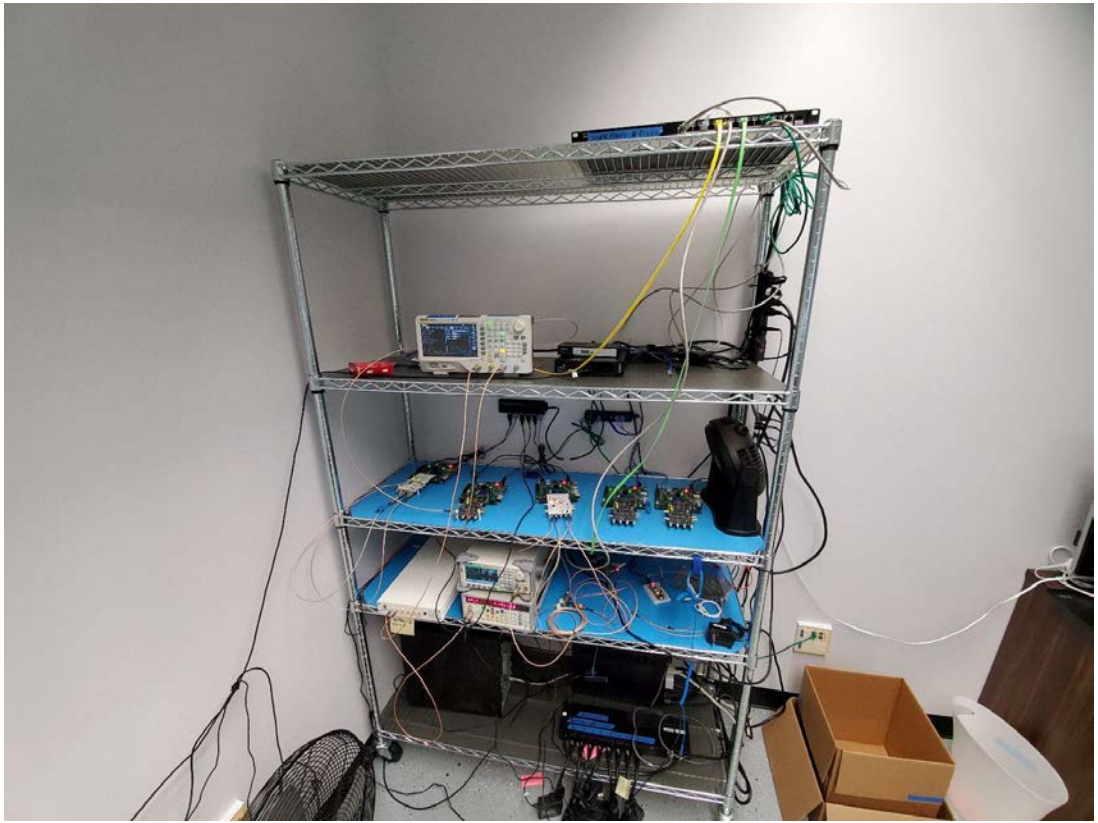


# Evaluation card

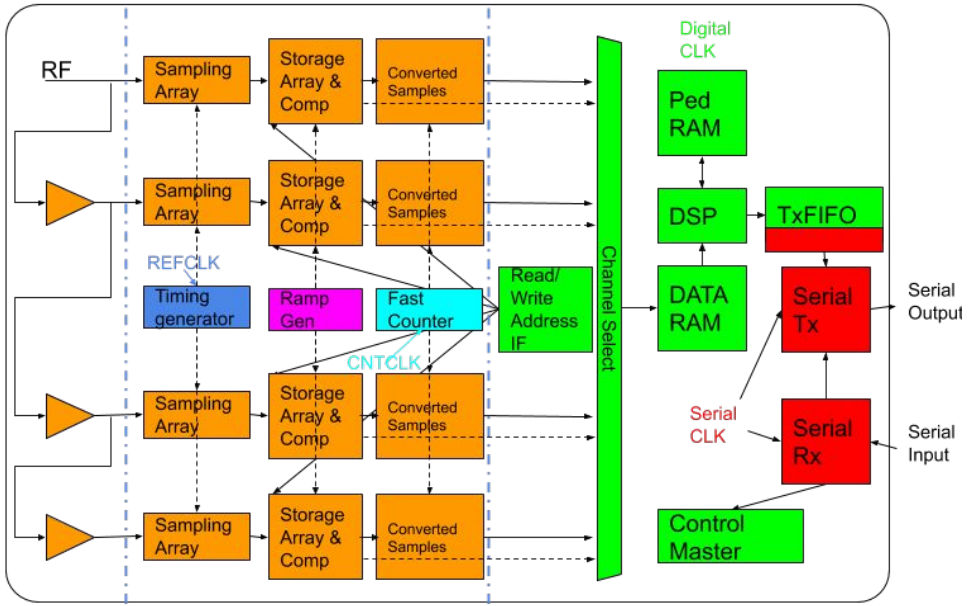


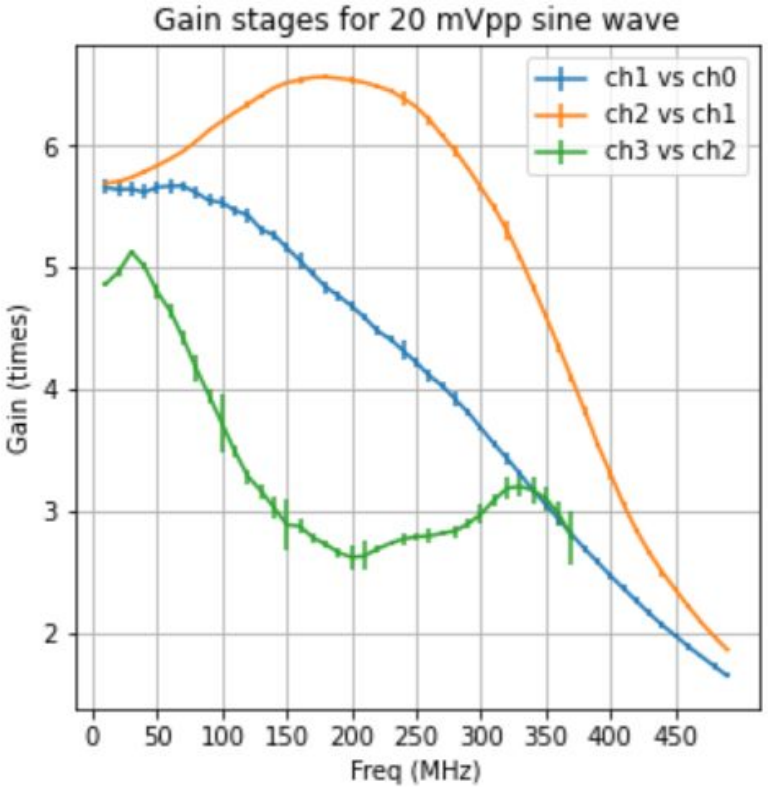


# Test setup - remote access



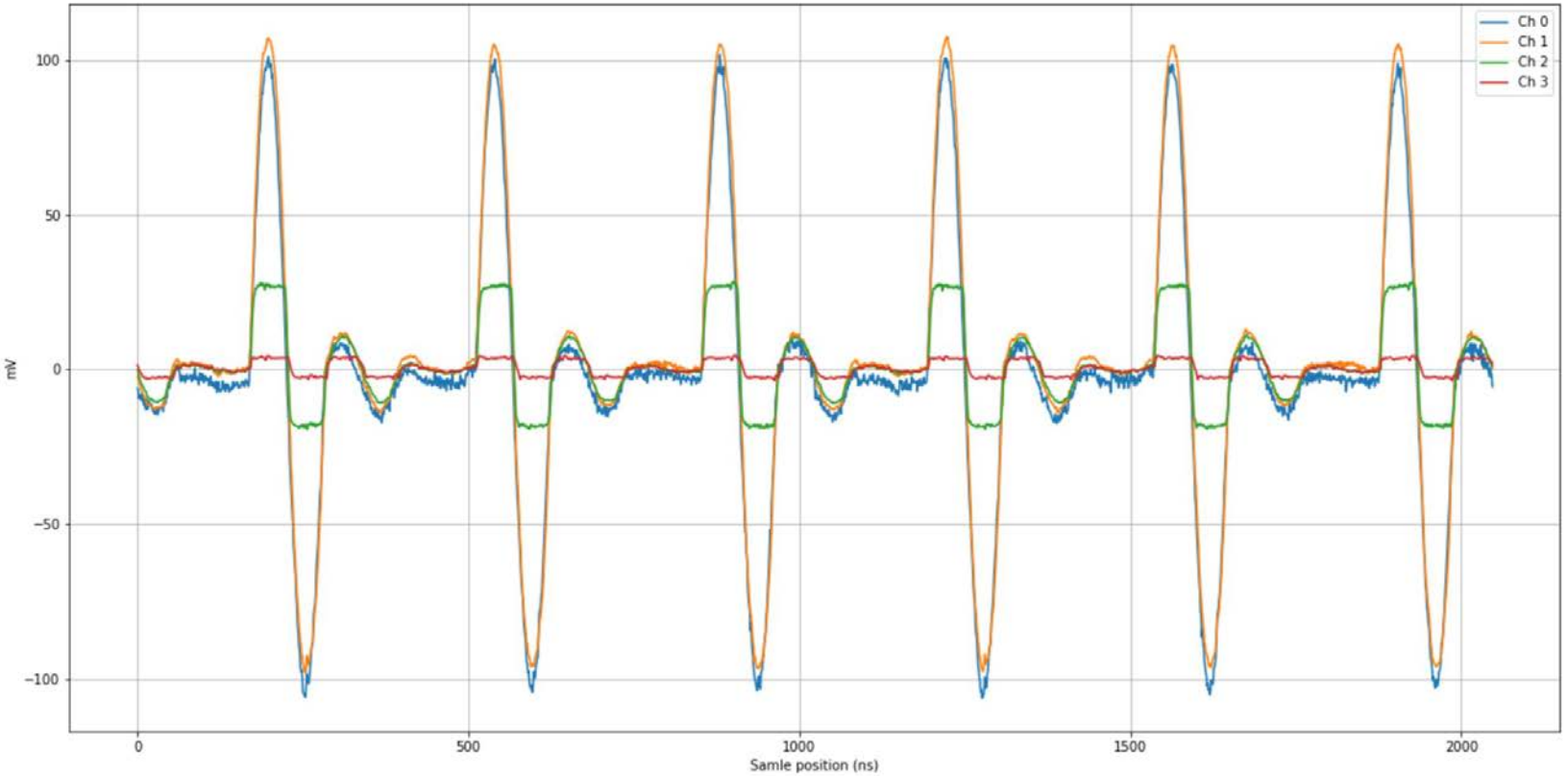
# Test setup



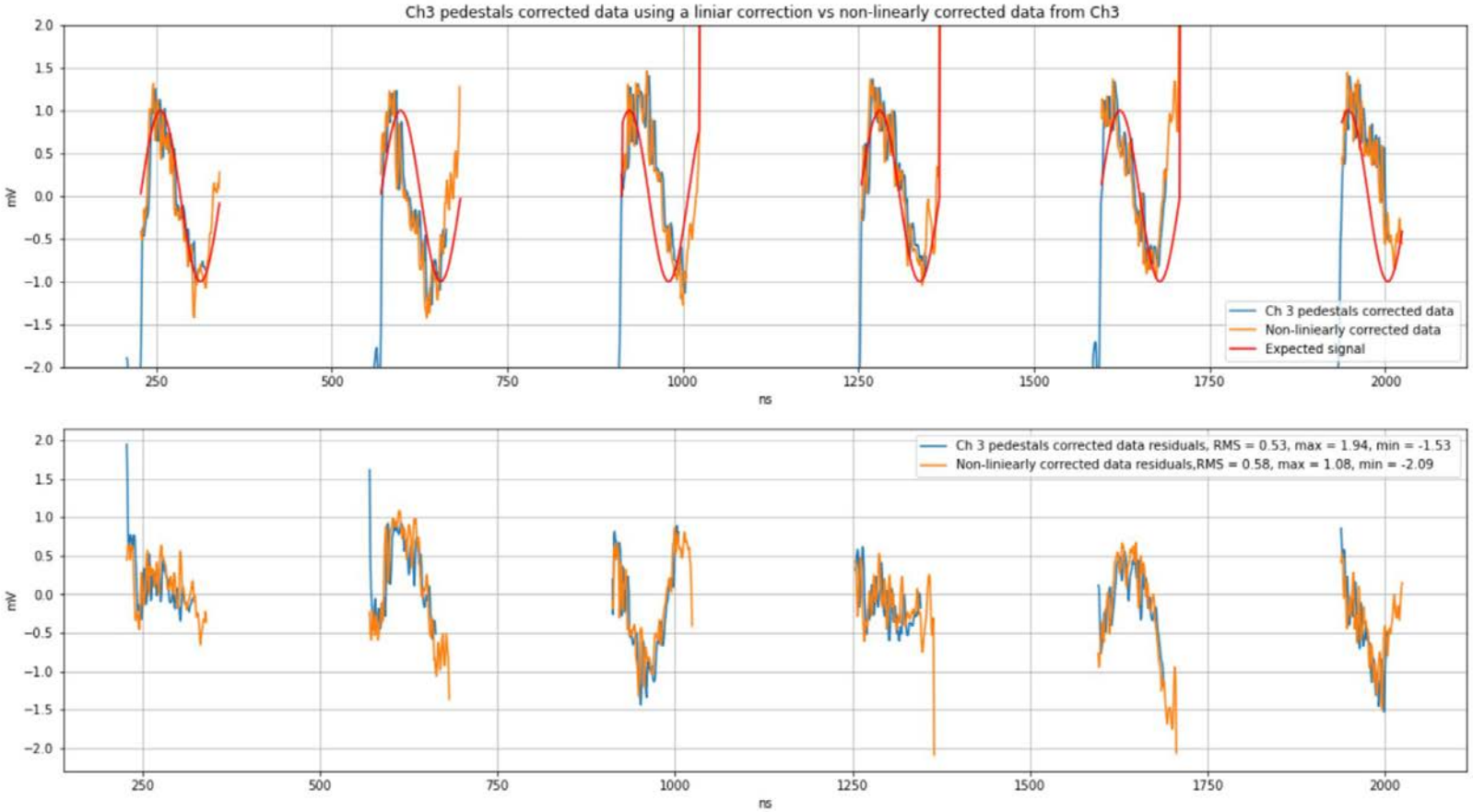



# Reconstruction

100mV, 10mV and 1mV cycles close to each other



# Reconstruction - zoomed in - work in progress

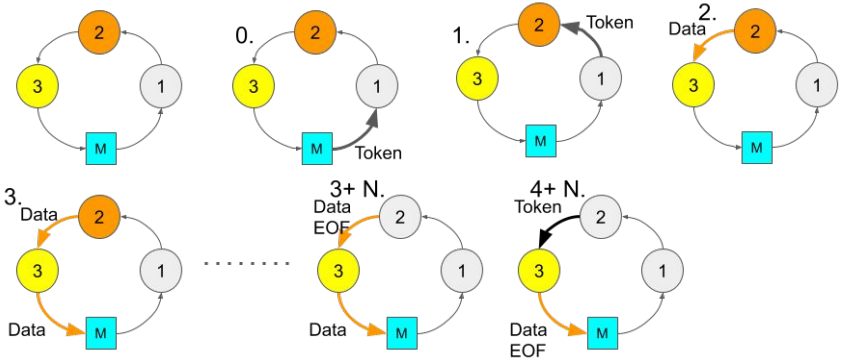


# SERIAL PROTOCOL

Readout node M: source of tokens or commands

Individual AODS

- Interpret the command, respond with ACK/NACK
- Hold the token, send data, release the token
- Pass the token/commend as they receive them



# SERIAL PROTOCOL

A simple serial protocol to allow daisy chaining of multiple devices

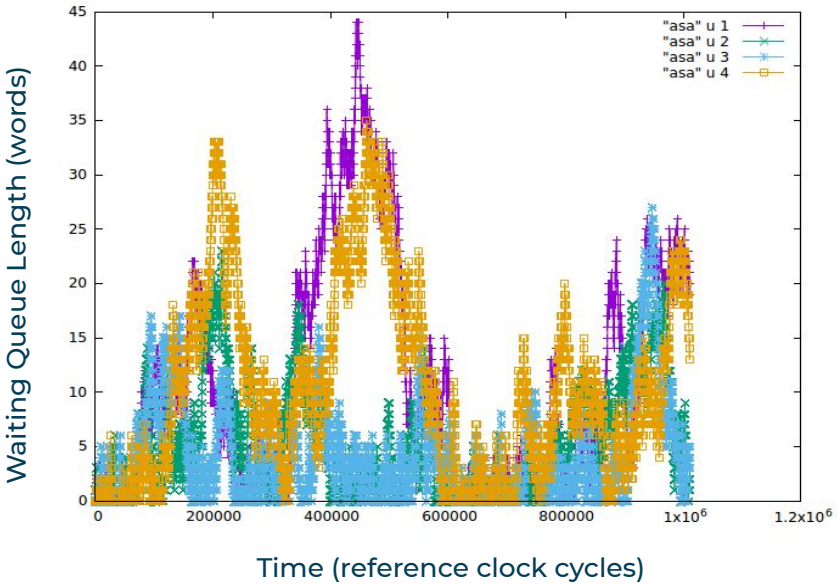
Four Packet types:

- Command (to individual slave or broadcast)
- Command ACK/NACK to master: acknowledge command or transmission error.
- Token (broadcast): any node with data captures it and start transmission, then release it to next node
- Data (to master): generated by the individual slaves only in response to a captured token - it empties the first packet sitting in their FIFO (if present)

# SERIAL PROTOCOL
## PERFORMANCE

Monte Carlo simulation with Poisson events in a chain of 4 AODS p(hit/cycle)=0.0025, packet - 100 cycles, occupancy = 1 (max possible throughput)

Queueing of up to analog buffer length - no loss of information



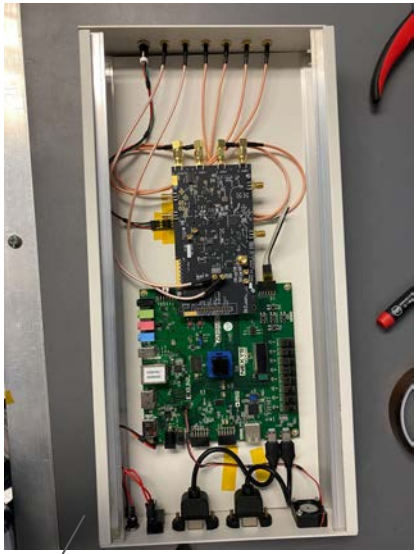
# Schedule

| Month into Phase II | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | % time |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Objective** | 5 | 5 | 1,4,5 | 1,4,5 | 1,4,5 | 1,2,4,5 | 3 | 3 | 3 | 1,5 | 1,5 | 1,2,5 | |
| WBS 1. kick-off | X | | | | | | | | | | | | 5% |
| WBS2,7.Characterize the AODS (rev.1,2) | $X_1$ | $X_1$ | $X_1$ | $X_1$ | $X_1$ | | | | | $X_2$ | $X_2$ | $X_2$ | 10% |
| WBS3,4,5,8 Design (rev 2,3)/Fabricate (rev 3) | | | $D_2$ | $D_2$ | $D_2$ | $D_2$ | $F_2$ | $F_2$ | $F_2$ | $D_3$ | $D_3$ | $D_3$ | 15% |
| WBS6,10 Test/dev suite | | | $X_2$ | $X_2$ | $X_2$ | $X_2$ | | | | | | $X_3$ | 15% |

- Slightly behind schedule:
  - Extra time needed for extensive testing.
  - Chip/FPGA shortage problems.
- Items still under test:
  - TID
  - Finalize digital/serial/daisy chain verification
  - Better test board
- AODS Rev 2 submission planned for Nov'22:
  - New low noise amps
  - Moving reconstruction into ASIC
  - Updated digital backend/calibration

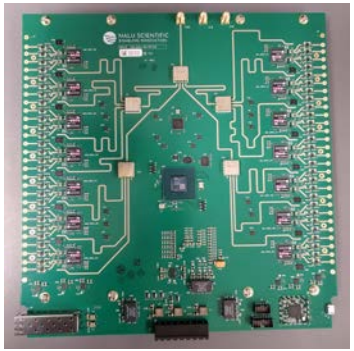
# Commercialization

- Sold over 10 ‘NaluBox’ digitizer evaluation kits
  - No ads, only word of mouth!
  - Moving to compact form factor
- Several integration R&D contracts from labs
- First FFP product contract from lab
- Distributor agreement in the works
- <u>Experimentalists want a solution (box), than a chip:</u>
  - Vertical integration (chip+HW+FW+SW+app note)
  - Focus on value-add engineering
  - Multi discipline knowledge of the user needs

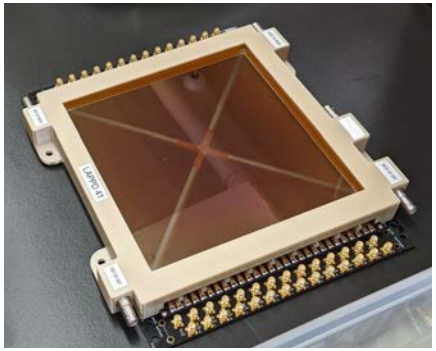



Shrinking!

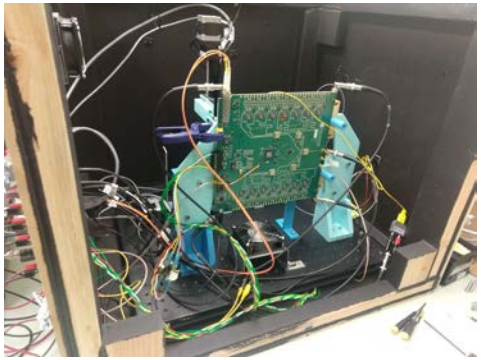
# Integration efforts - HIPeR



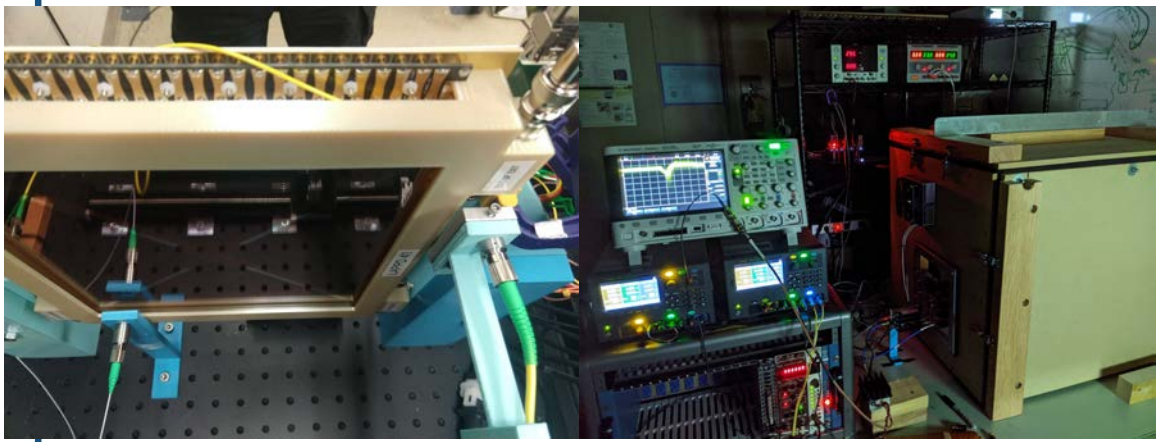
AARDVARC based readout

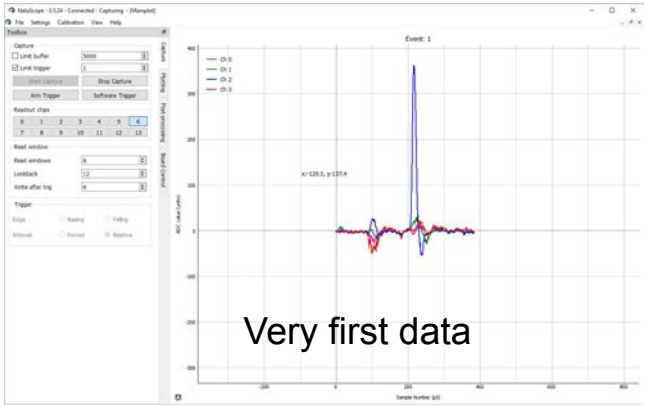


Incom's Gen 1 LAPPD



Integration and testing (UH)

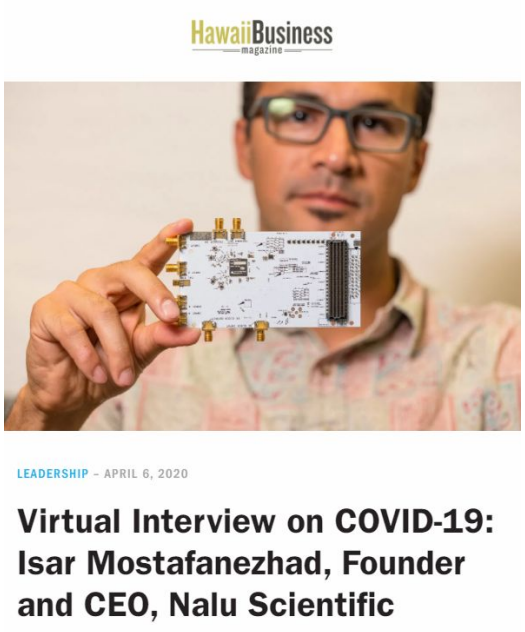





**Nalu Scientific Phase I SBIR in collaboration with Incom and University of Hawaii.**

# Getting the Word Out

- Awards (40U40, most innovative, …)
- Attending conferences, trade shows, pitch competitions
- Media attention on restarting/diversifying economy in Hawaii esp post COVID
- **Check us out: website, Social Media handles: FB, LinkedIn, Twitter**





Booth and AARDVARC Live demo at US-Japan Particle Physics Symposium in Honolulu (April 2019)

Pacific Biz News 40 under 40


Next Top Startup Pitch Competition
Runner up - IMS2019 - Boston


Hawaii Biz Magazine
Most Innovative Small Biz of the year


IEEE Young Professionals Panel
IMS2019 - Boston


IPAC 2019 booth- Melbourne


Hawaii Congressman Ed Case visit

# ACKNOWLEDGEMENTS

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