Pacific MicroCHIP Corp.

12-bit 32 Channel 500MSps Low Latency ADC

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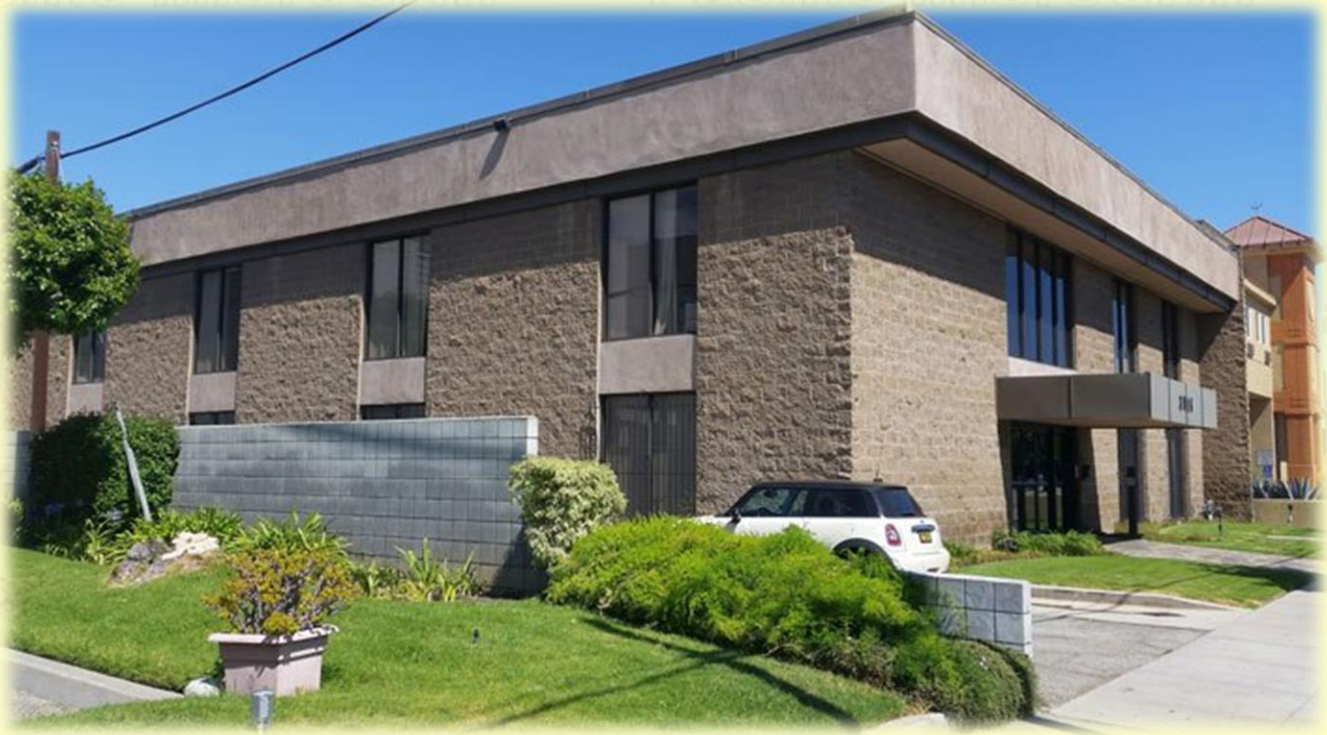
OUTLINE

Pacific MicroCHIP Corp.

- The Company, its Specialization/Expertise
- Our offerings
- Where the ASIC fit
- Project goals for Phase II
- ASIC specifications and block diagram
- ADC core architecture
- Comparison with ADCs available on the market
- ASIC layout
- Fabricated chips and packaging information
- Testing setup and results
- Future plans

COMPANY

- Pacific MicroCHIP Corp. is incorporated in 2006.
- It is headquartered in Culver City, California
- Main focus – providing IC/ASIC design services and turnkey solutions.



OUR OFFERINGS

Pacific MicroCHIP Corp.

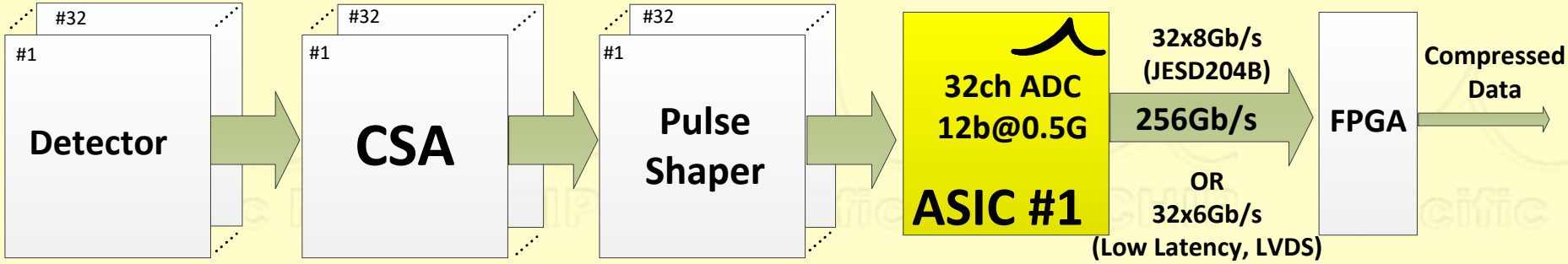
IC/ASIC Design Services:

- Circuit Design (analog, RF/mixed, digital)
- Simulation
- Physical Design
- Chip Assembly

Turnkey Solutions:

- IC Design
- Chip Fabrication Logistics
- Package Development (involving a 3rd party)
- Chip Packaging (involving a 3rd party)
- PCB Development for Testing/Eval. (involving a 3rd party)
- Testing/Characterization (an in-house lab)
- Delivery of Chips, Parts and Board Level Solutions

WHERE THE ASIC FIT



NP detectors require thousands of signal processing channels:

- Shrink in size - our ASIC combines 32 independent ADCs per chip.
- Reduce power consumption - we offer 25mW per ADC (w/o JESD buffers).

Upgrades in these systems demand for:

- Digitizing accuracy - our ADC features 12-bit resolution.
- Adequate sampling speed - our ADC features up to 0.5GS/s.
- Low conversion latency - we offer 8ns.

Targeted applications:

- Low latency particle beam control systems.
- Imaging and spectroscopy systems for gamma-ray detectors.
- Multichannel detectors based on tube and silicon photo multipliers.

PROJECT GOALS FOR PHASE II

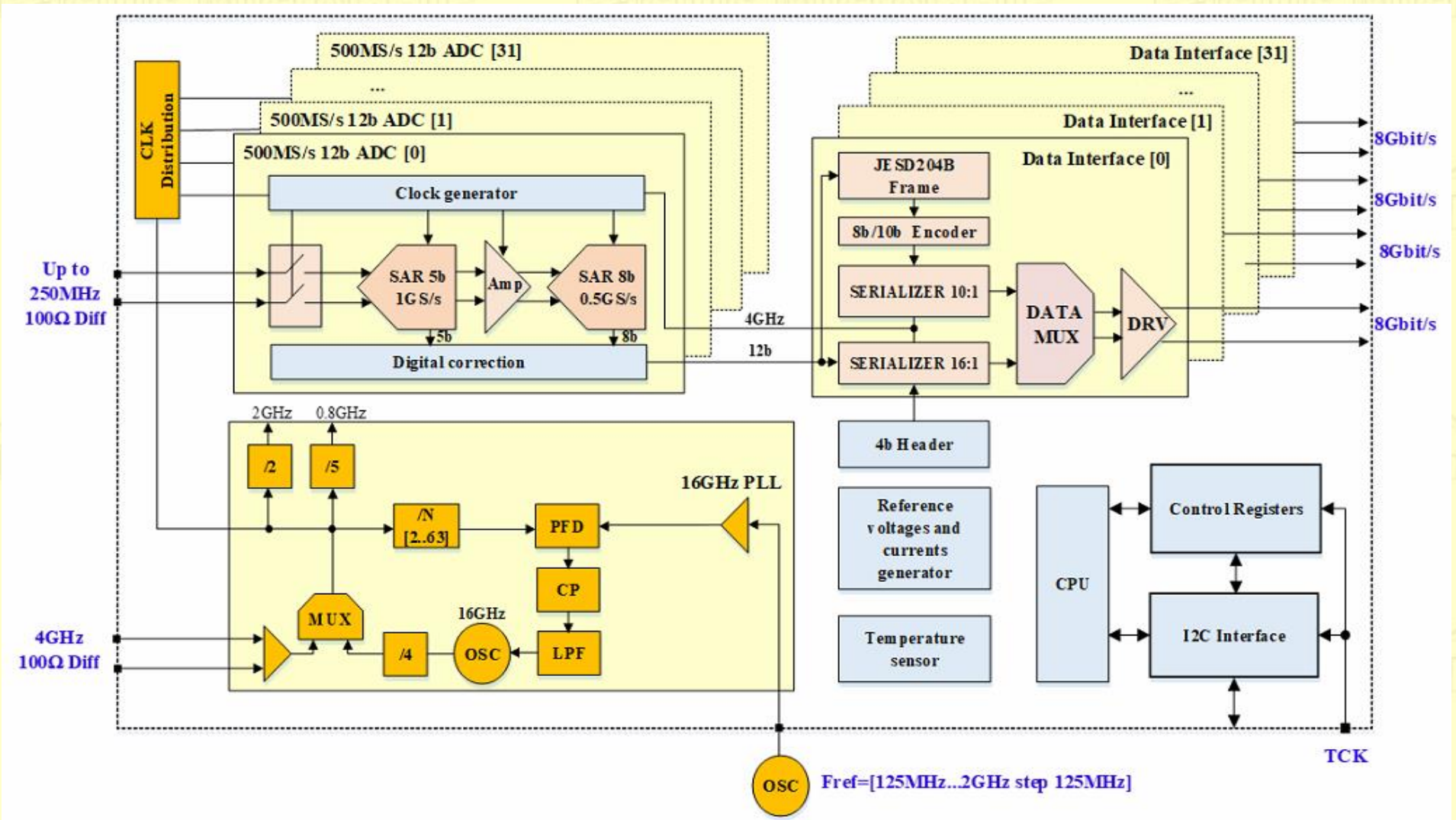
Pacific MicroCHIP Corp.

- Design circuits and layout for the ADC ASIC.
- Fabricate the chip.
- Develop a special chip carrier.
- Package the chips.
- Develop a test PCB and a DUT socket.
- Develop a GUI and a test bench.
- Test and characterize the ADC ASIC.
- Prepare a datasheet for marketing.
- Submit deliverables to the DoE.

ASIC SPECIFICATION

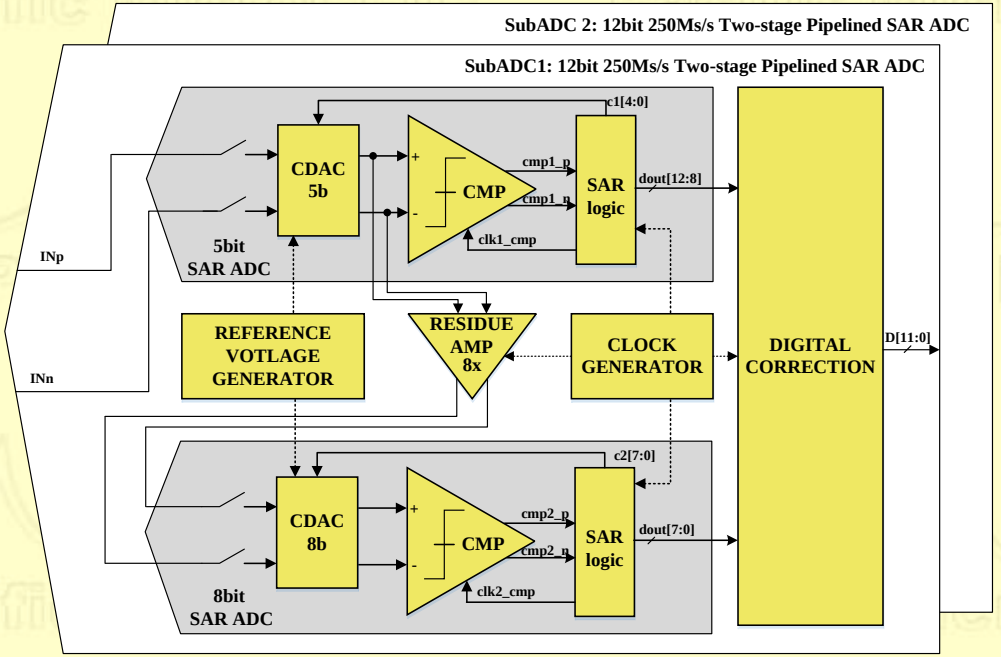
- 32 independently operated ADC channels
- 500 MS/s sampling rate
- 0.6Vpp differential input swing
- Up to 9.5-bit ENOB
- 250MHz Input signal bandwidth
- -40C..+125C temperature range
- 25mW/channel power consumption (with interface)
- JESD204B output data interface
- 8ns latency (direct ADC data output mode)
- 32x8Gb/s output data rate
- I2C interface for ASIC control
- 8.7mm^2 estimated ASIC layout footprint
- Solder bumped die in a BGA package
- 28nm CMOS technology

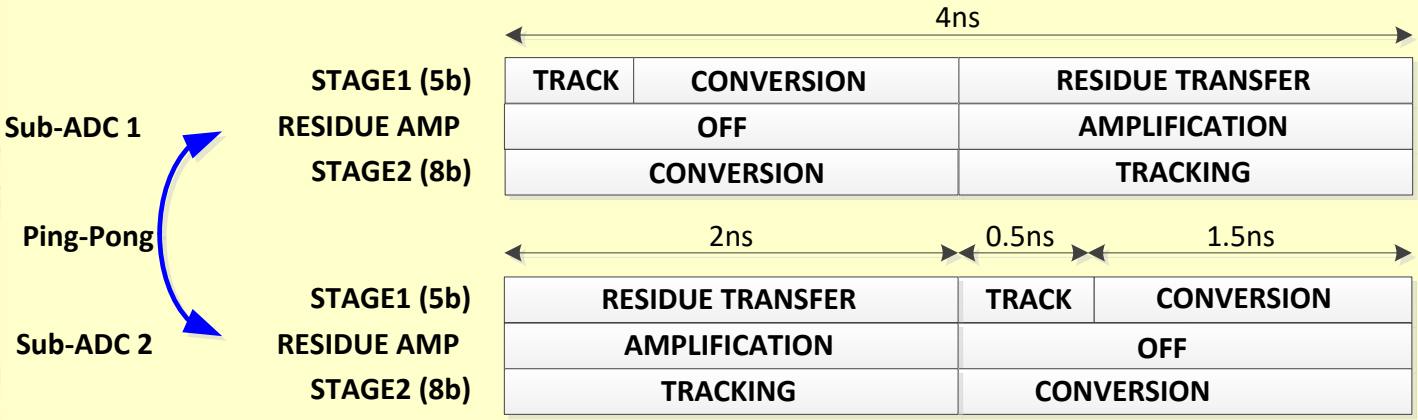
ASIC BLOCK DIAGRAM



ADC CORE ARCHITECTURE

- Two-times time-interleaved ADC core
- Sampling clock skew adjustment
- Two-stage pipelined SAR architecture
- Programmable residue Amp gain
- Programmable ADC FS range
- Bootstrapped input switches
- 1-bit redundancy between ADC stages





COMPARISON TO 12-bit ADCs AVAILABLE ON THE MARKET

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#	Vendor	# of Channels	Sample Rate, MS/s	Power Cons. per Channel	Architecture/ Latency
1.	TI 12-bit ADS52J90	32	40	41mW	Pipeline/ 2.5us
2.	TI 12-bit ADS5403IZAYR	1	500	1W	Pipeline/ 240ns
3.	TI 12-bit ADS54T04IZAYR	2	500	1.15W	Pipeline/ 240ns
4.	ADI 12-bit AD9234BCPZRL7	2	500	1.5W	Pipeline/ 240ns
5.	Pacific Microchip Corp. 12-bit*	32	500	36mW	SAR/Pipeline/ 8ns

* Expected performance

MULTICHANNEL ADC ASIC LAYOUT

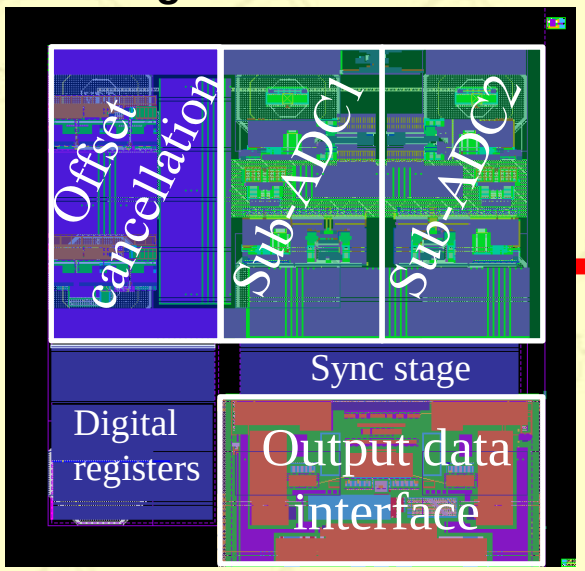
Chip's periphery:

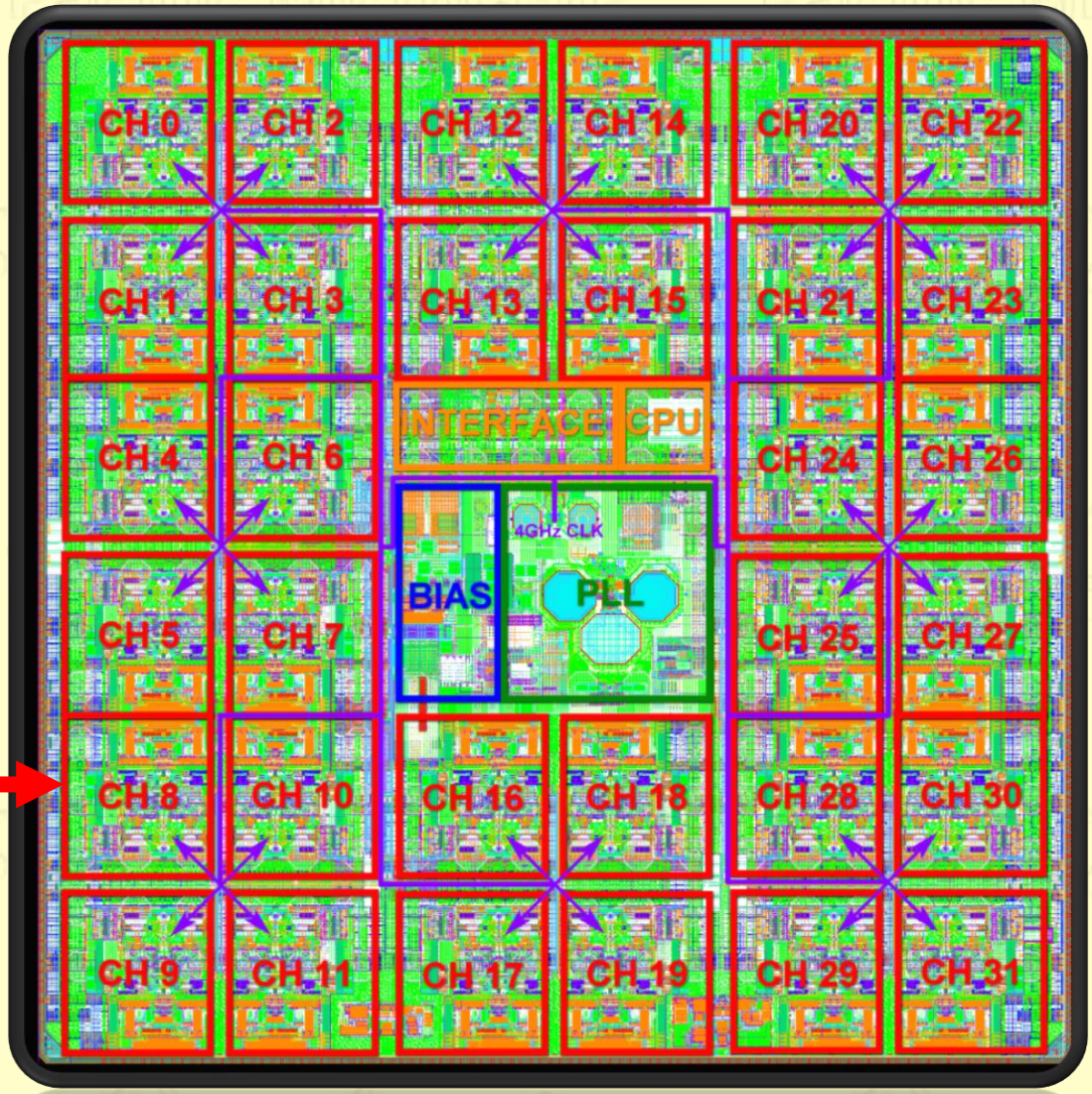
32 independent ADC channels located in 2 circles

Central part:

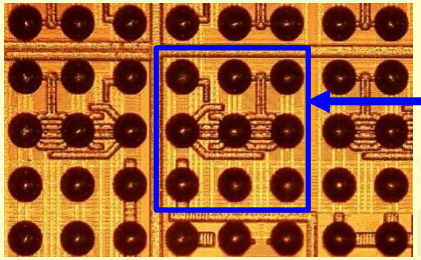
- PLL with a clock tree
- CPU for calibration
- I2C control interface

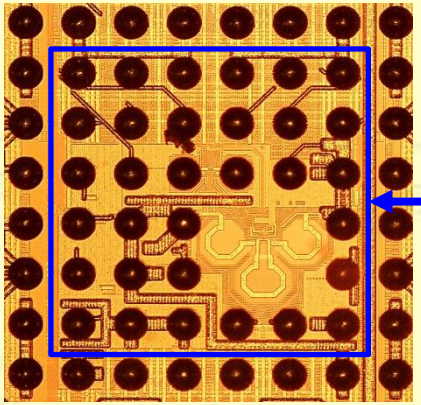
Single ADC channel:

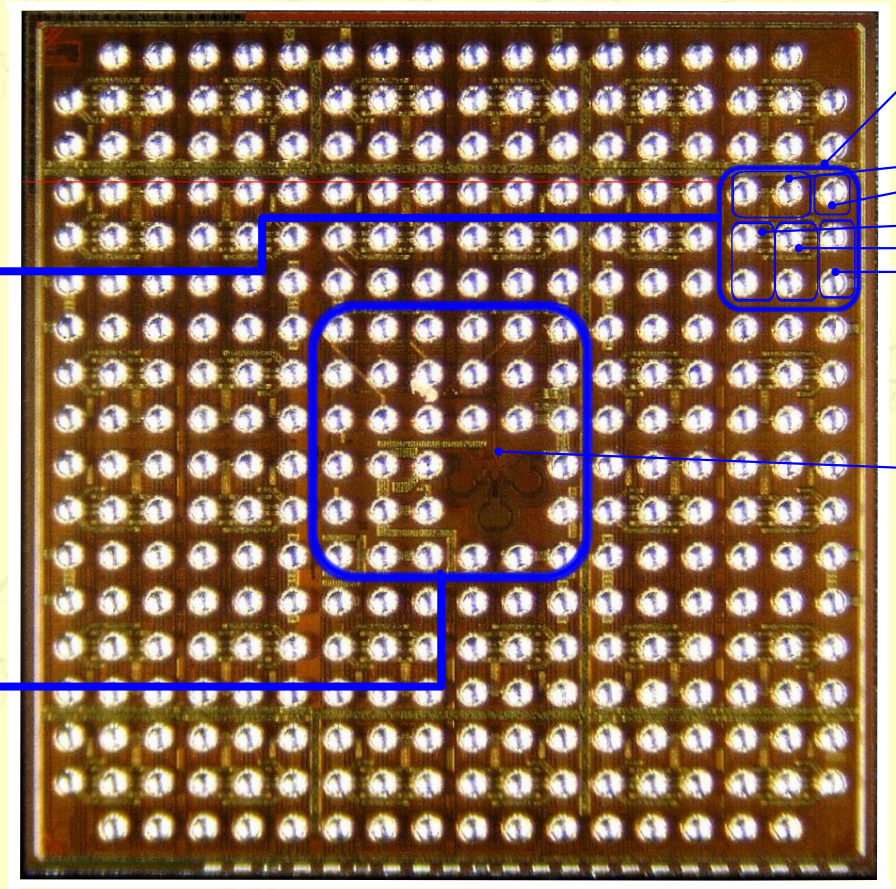




FABRICATED CHIPS



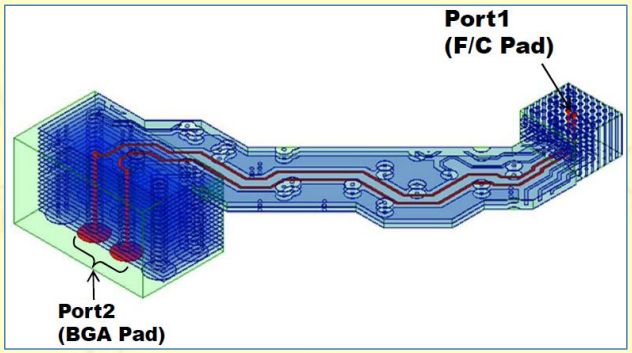


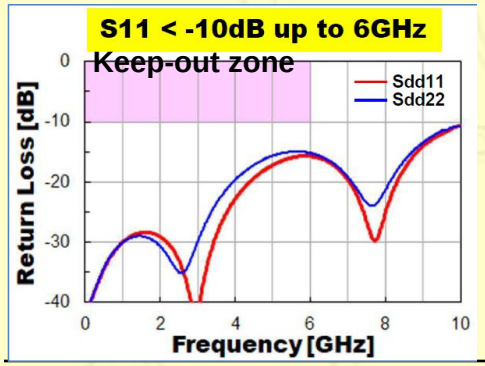


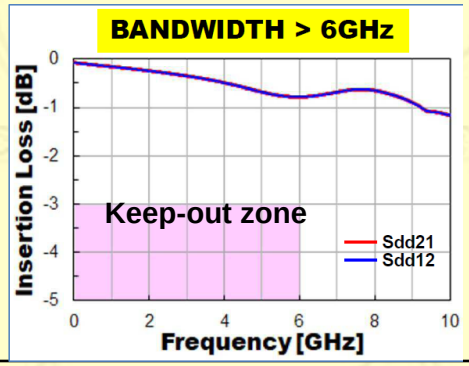
CHIP PACKAGING

Package: BGA 15.2 x 15.2 mm, 18 x 18 balls, 0.8mm ball pitch

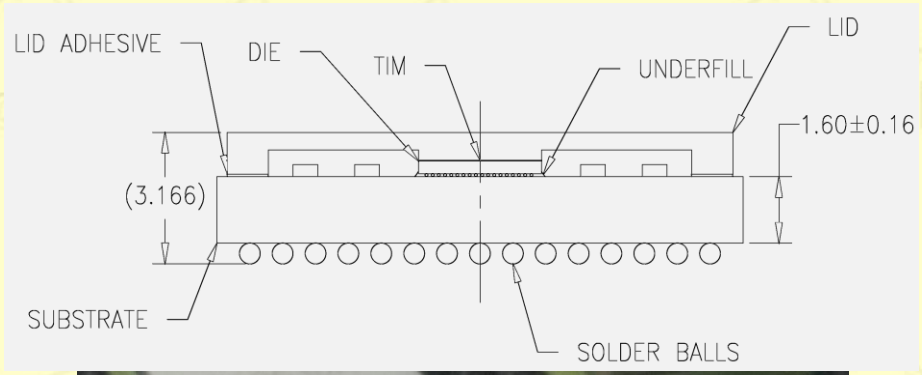
S-parameter simulation results for longest signal input wires:
S11 < -10dB up to 10GHz
S21 > -1dB up to 9GHz

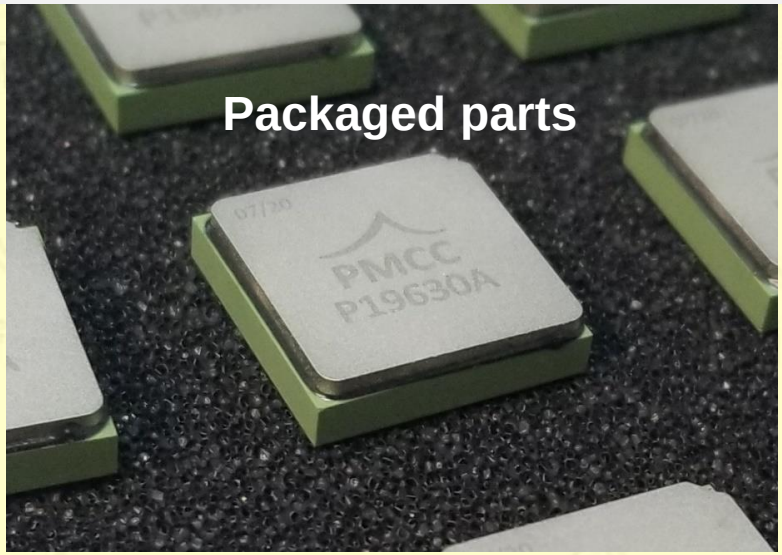






Package cross-section





TESTING SETUP

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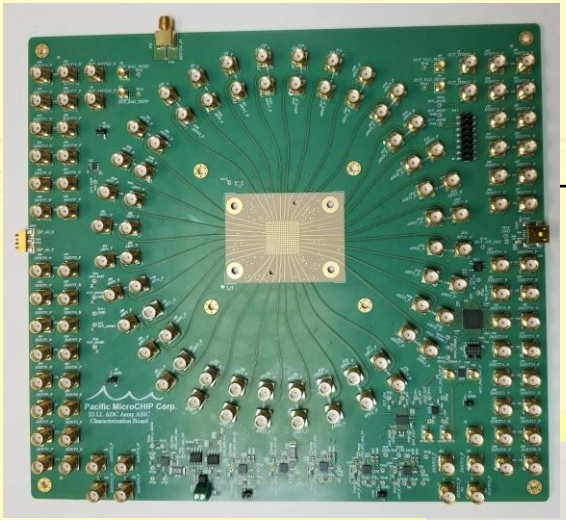
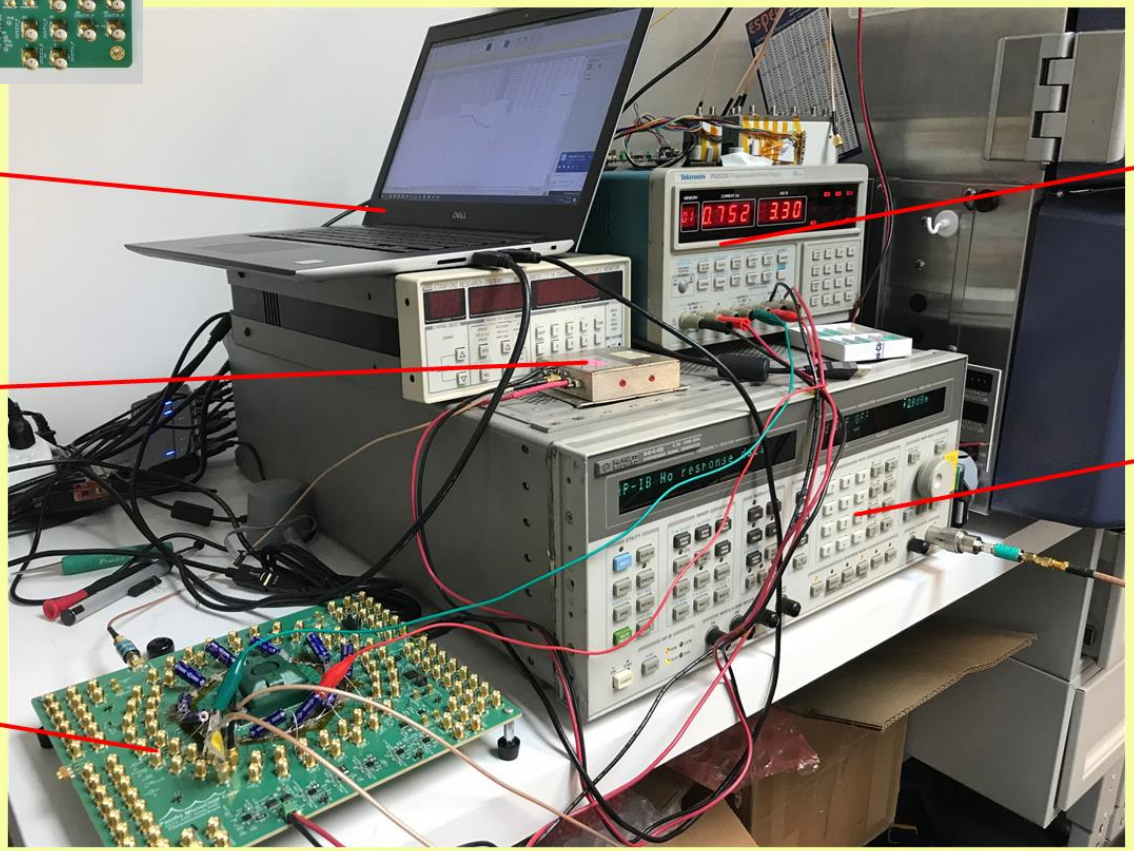


← Test Board

Windows PC for controlling all equipment and characterization PCB

Ultra-low jitter 2GHz clock source

Characterization PCB



Power supply for powering board, clock generator and external VCM

HP8644B Ultra-low noise signal generator

TESTING RESULTS

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Power Consumption

Supply	V [Volts]	I [mA]	P [mW]
VDDD	0.9	445	400.5
VDD18	1.8	9	16.2
VDDA	0.9	88	79.2
VDD12	1.2	564	676.8
PLL	0.9	60	54.0
Total:			1226.7
Per Channel:			**38.3**

Notes:

- Power of the JESD204B interface is included.
- An input signal is applied only to a single ADC out of 32.
- The VDDD consumption is expected to increase when a signal is applied.

TESTING RESULTS : PLL

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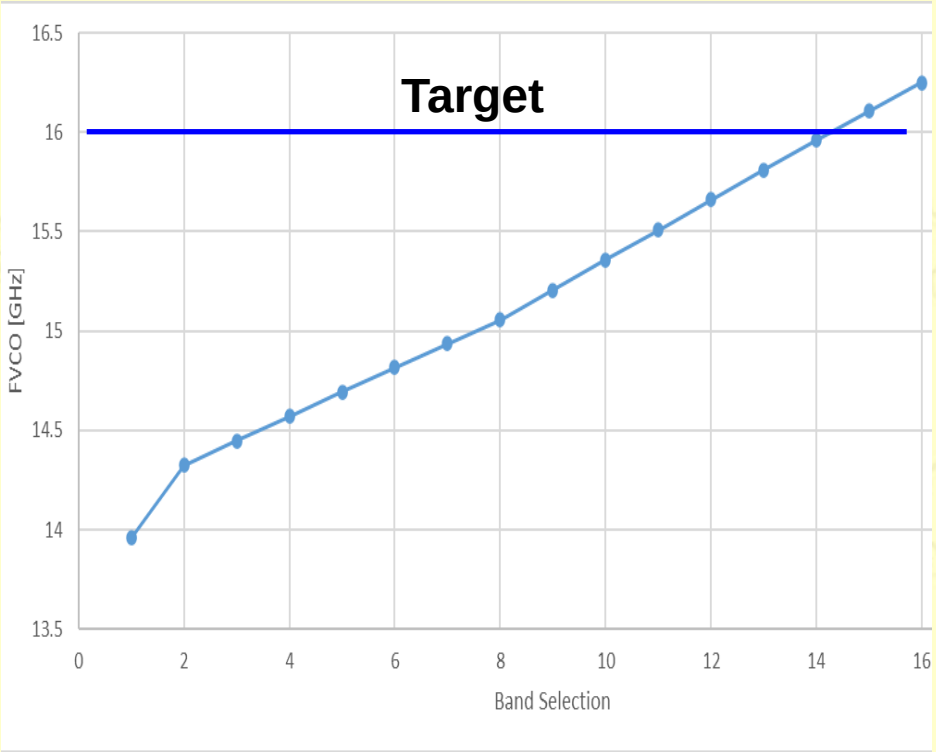
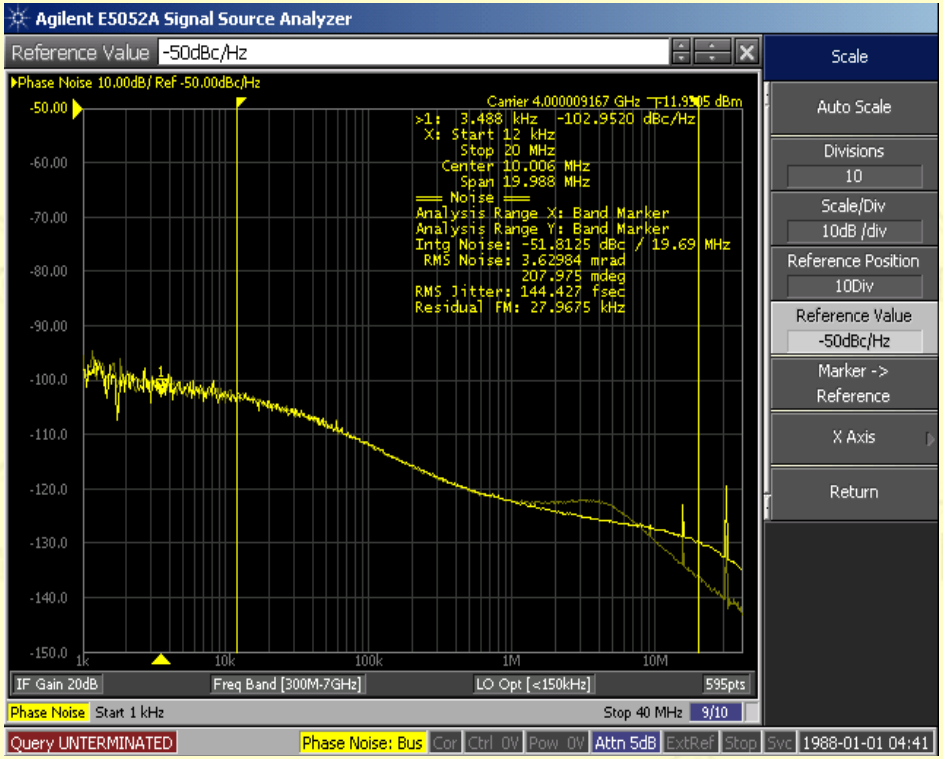
Targeted frequency achieved on the 14th band. It will be tuned up in the 2nd prototype.

Phase noise tested at 16GHz/4. 144fs RMS jitter (12K-20MHz range). Jitter does not depend significantly on PLL BW.





TESTING RESULTS : PERFORMANCE

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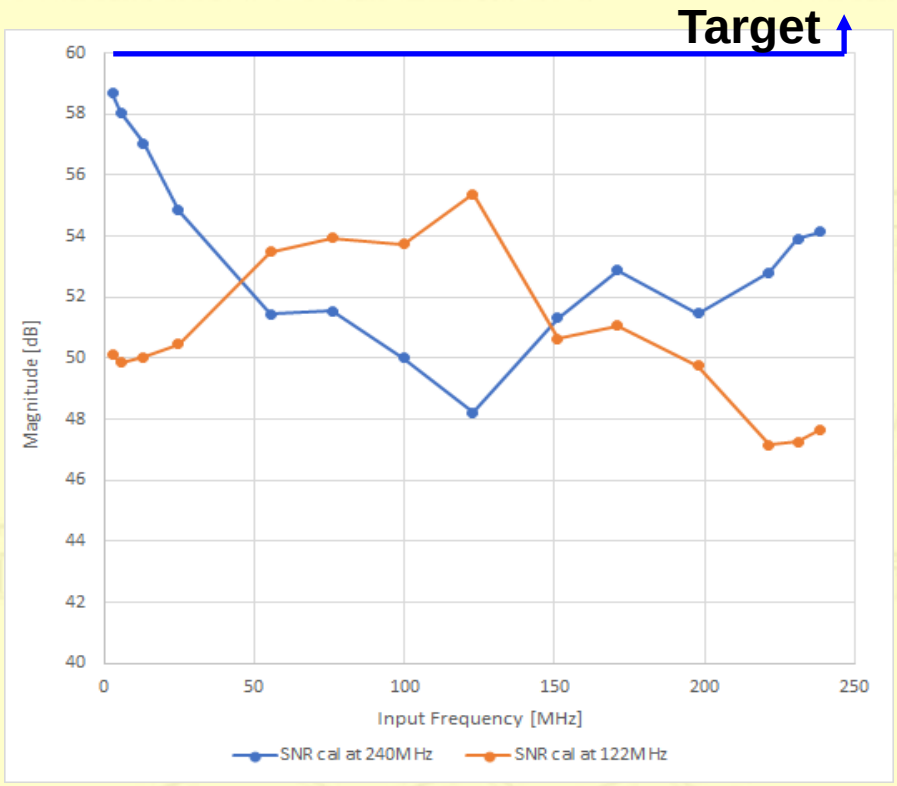

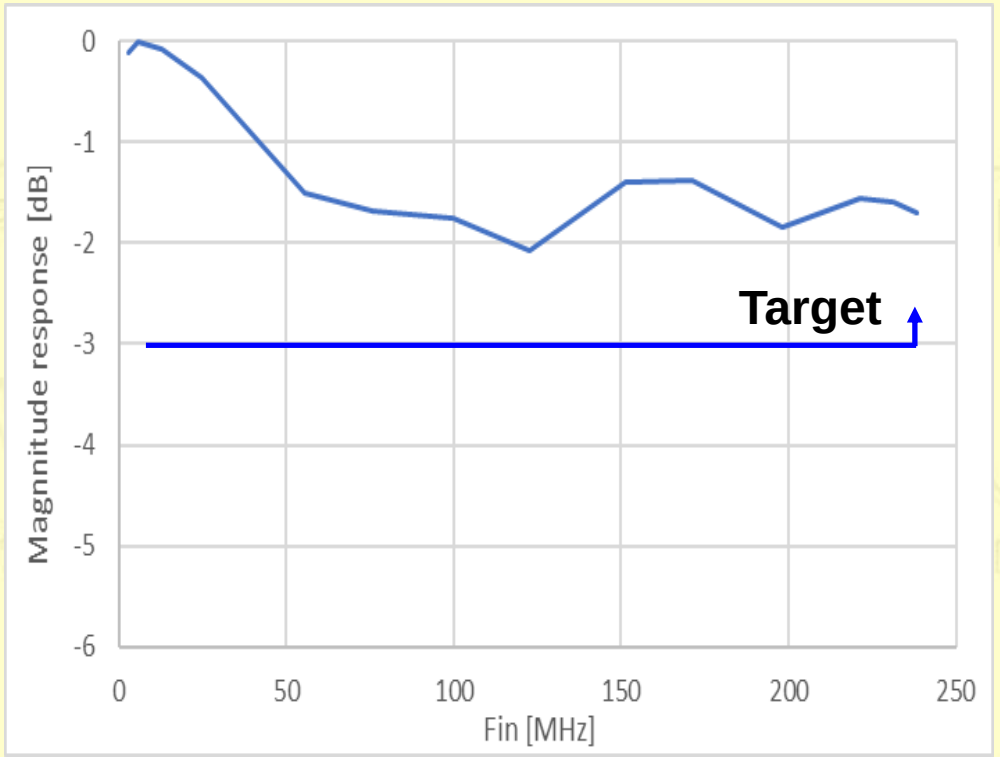

ENOB vs. Input Signal Frequency,
When ADC is calibrated at 240MHz:
9.5 ENOB @ 5MHz
7.2 ENOB @ 250MHz (Nyquist)

ENOB vs. Input Signal Frequency,
When ADC is calibrated at 122MHz:
8.5 ENOB @ 122MHz

FUTURE PLANS

Pacific MicroCHIP Corp.

- To find funding for Post Phase II project
- To redesign the chip, increase its performance, fix issues identified during testing.
- To fabricate the final chip.
- To test/evaluate it.
- To prepare the chip description and datasheets.
- To provide the chip to the NP/HEP community and commercial customers.

THANK YOU

We would appreciate any application ideas and customer leads for the presented 32ch ADC ASIC !