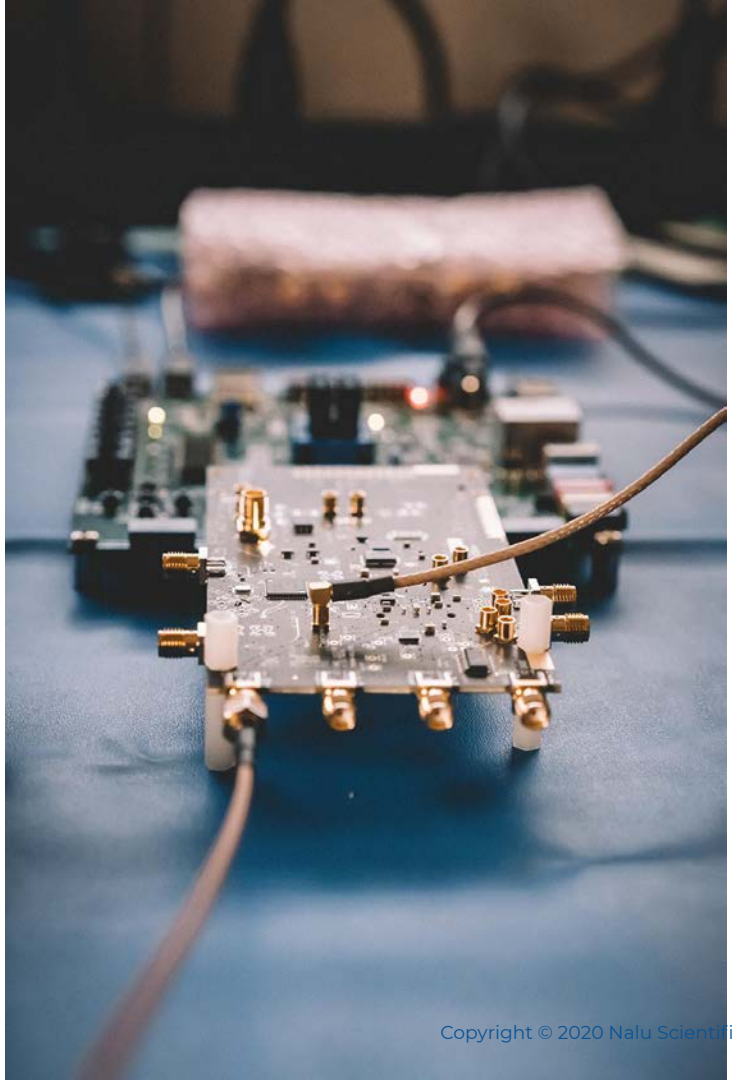


NALU SCIENTIFIC
ENABLING INNOVATION

Design and Fabrication of the ASoC

August 13th, 2020
Isar Mostafanezhad, Ph.D.
CEO and Founder of Nalu Scientific LLC

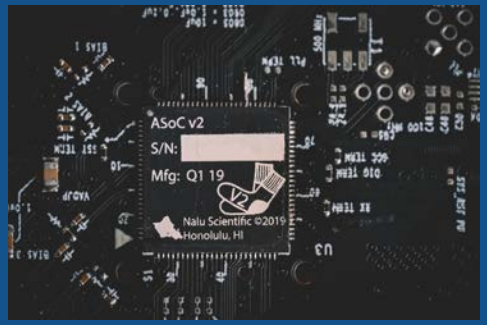
Grant: DE-SC0015231- SBIR Phase II

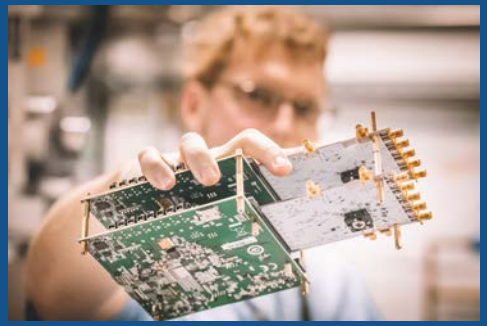
4/10/2017- 4/09/2019, NCE 1/30/2020

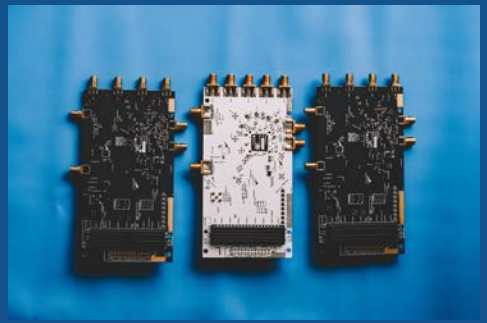
PRESENTATION SUMMARY

TOPICS COVERED:

- About Nalu Scientific
- Background on NP/HEP experiment needs
- ASoC Project
- Synergies
- Commercialization Efforts
- Next Steps







ABOUT NALU SCIENTIFIC

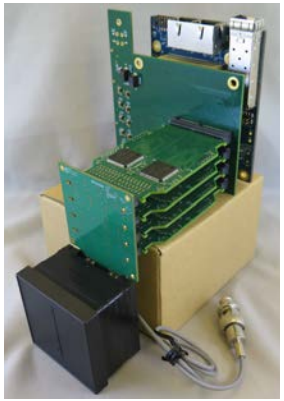
Fast Growing Startup in Honolulu, HI
- Located at the Manoa Innovation Center

Integrated Circuits Design
- Analog + digital System-on-Chip (SoC)
- Digital implementation

Hardware Design
- Field Programmable Gate Arrays (FPGA)
- Complex multi-layer Printed Circuit Board (PCBs)

Expertise in:
- Fast timing
- Radiation detection
- Readout electronics for Particle Physics

WAVEFORM DIGITIZER SoCs
FOR SINGLE PHOTON TIME OF FLIGHT DETECTION



1. Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly

2. Integration:

- SiPM
- PMT
- LAPPD
- Detector arrays

3a. Main application:

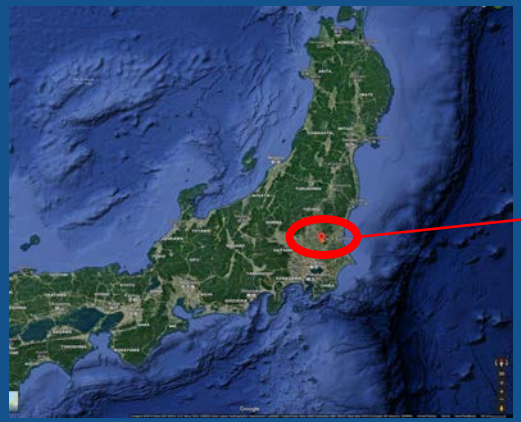
- NP/HEP experiments
- Astro particle physics

3b. Other applications:

- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging

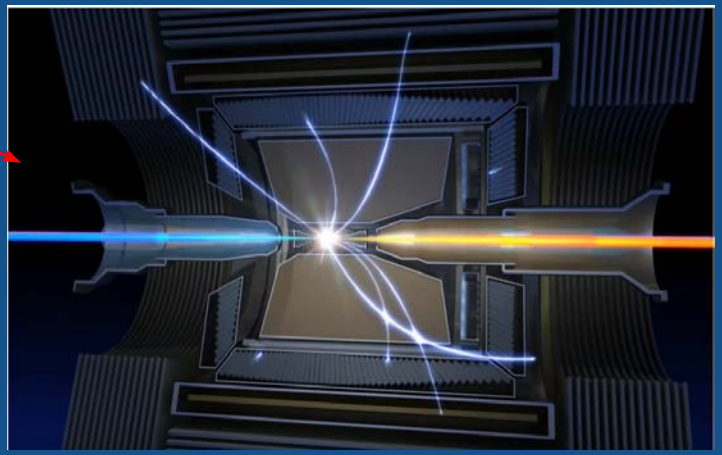
WHERE WE STARTED

A Search for New Physics – The Belle II Experiment



Tsubuka City
Located 60 mi north of Tokyo

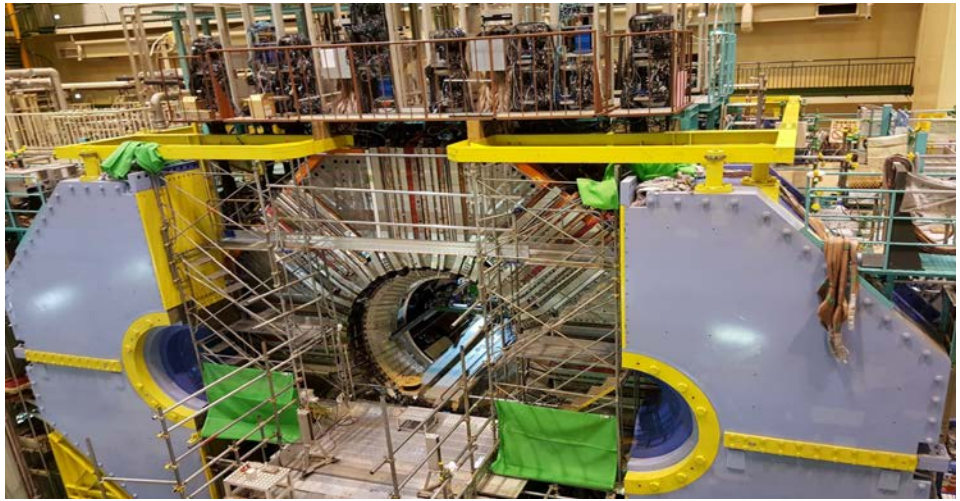
High Energy Accelerator Research Facility (KEK)
in Tsukuba



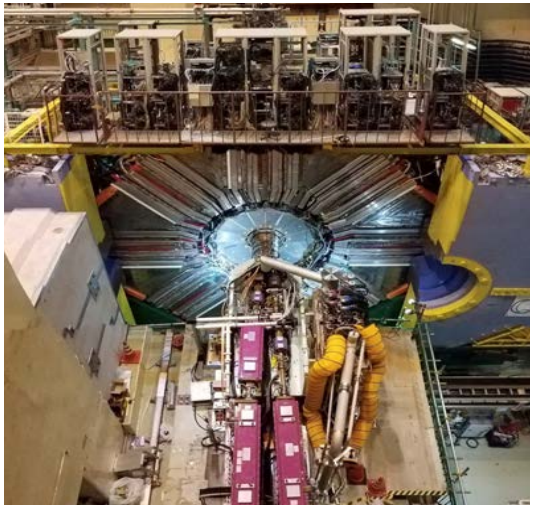
Interaction point inside the electron/positron collider

HISTORY OF BELLE II

Belle II Upgrade is a 26+ Country, 900 Member Collaboration



2015

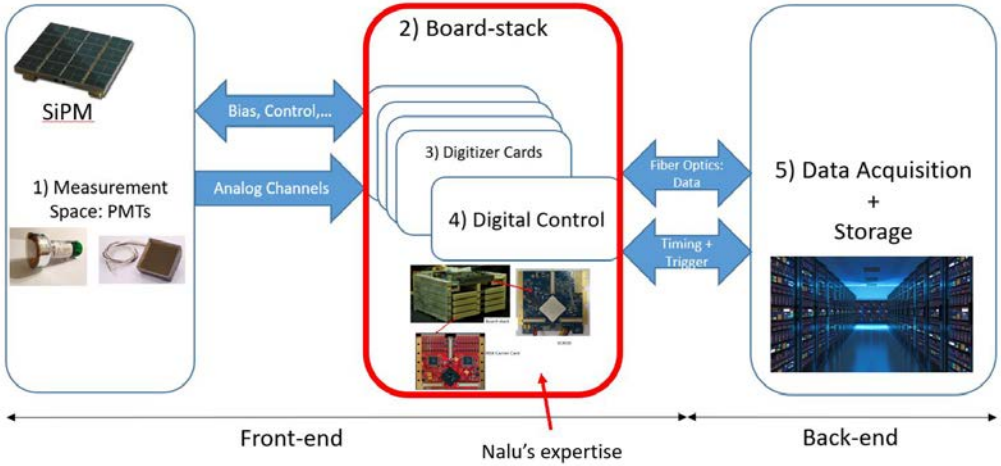


2018

Belle II: e+ e- experiment at 40x luminosity of Belle -> Detector needs to operate at severe beam background

HOW DOES A NP EXPERIMENT WORK?

LESSON ONE



LESSON TWO

Next gen Particle Physics electronics need to be:

- Radiation hard
- High performance
- Accommodate long trigger delay
- Low cost, low power
- User friendly

Solution: New System-on-Chip Integrated Circuit Design

Opportunity: Not many commercial options available

Proposed Solution (ASoC) :
Chip level integration of switched capacitor array (analog) with digital processing.

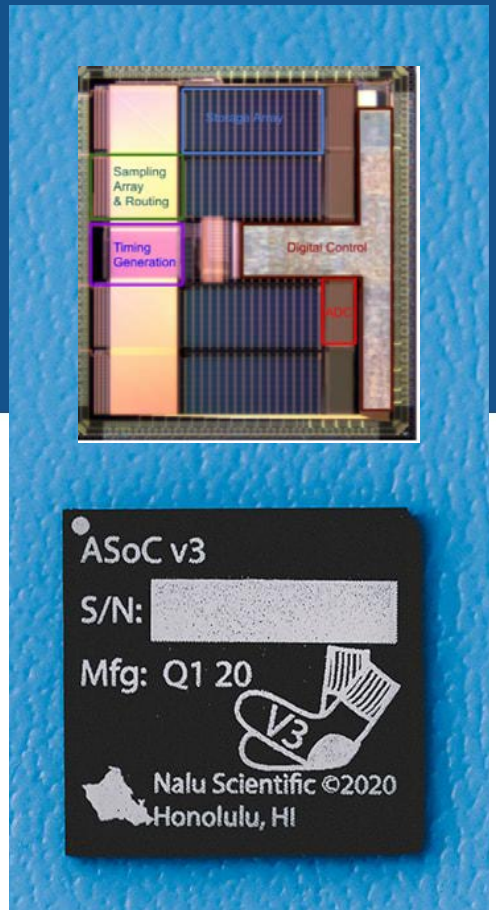
ASoC V3 DESIGN DETAILS

Compact, high performance waveform digitizer

- High performance digitizer: 3+ Gsa/s
- Highly integrated
- Commercially available, low cost, patented design
- 5mm x 5mm die size

ASoC PARAMETERS	SPECIFICATION (MEASURED)
Sample rate	2.5 - 3.6 GSa/s
Number of channels	4
Sampling depth	16 k Sa/channel
Signal range	0-2.5 V
Resolution	12 bits*, 10b ENOB
Supply Voltage	2.5 V
RMS noise	~ 1 mV
Digital Clock frequency	25 MHz
Timing resolution	1<25 ps***
Power /ch	50-125 mW/channel*
Analog bandwidth	950 MHz

- Integration/features:
- Calibration memory on chip
- PLL on chip
- Isolate analog/digital voltage rings
- Increase number of channels
- Implement serial interface
- Feature extraction on chip



ASoC PHASE II SCHEDULE

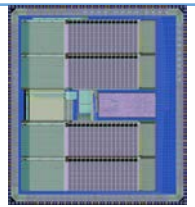
3X ASoC revision proposed

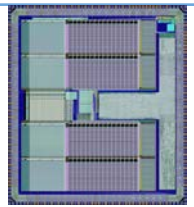
3x fabricated

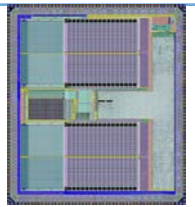
Test and characterization

Beta testing

Deliverable Summary	Status
Careful review of the final ASoC design and sending to low cost 250nm fabrication facility for tape-out.	COMPLETE
Complete and full chip commercial grade design at Nalu Scientific	COMPLETE
Design and implementation of the required PCBs and evaluation kits for immediate in-house testing of the ASoC, which will help after each tape-out	COMPLETE
Characterize the ASoC by measuring electrical properties and limits of performance and create industry grade documents and datasheets	COMPLETE
Repeat the 3 tape-out and design tweak/debug cycles until the final ASoC meets the desired performance	COMPLETE

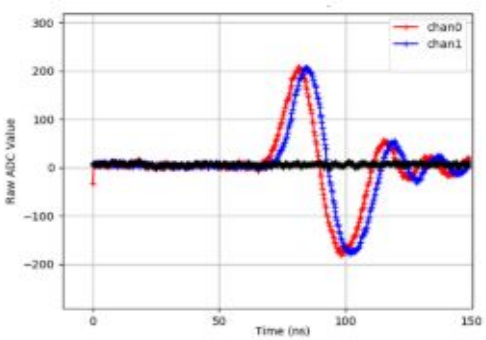




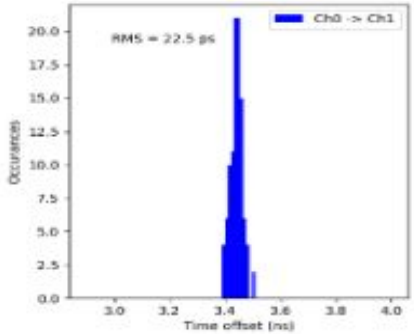


ASoC V2 MEASUREMENTS

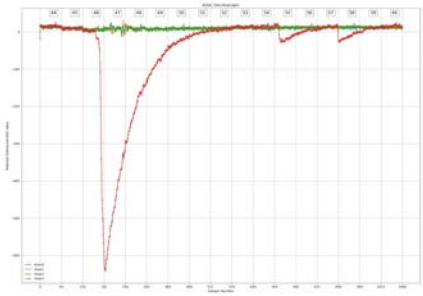
Live demo at IEEE NSS-MIC 2019



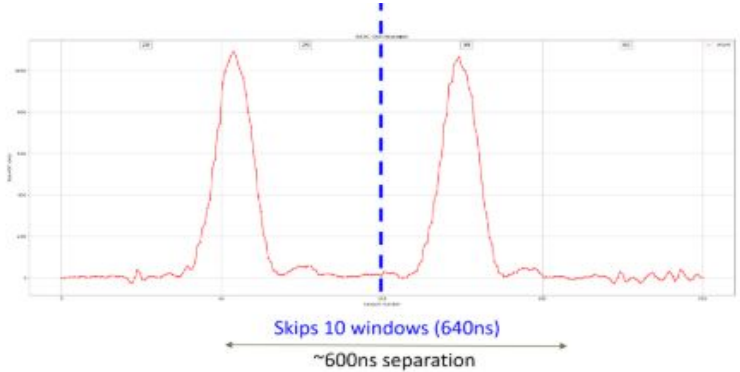
Timing resolution: 22ps

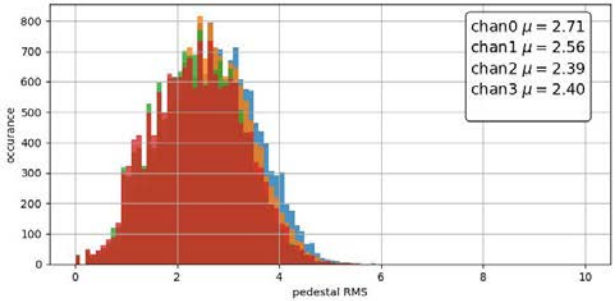


SiPM waveform readout



ROI Readout

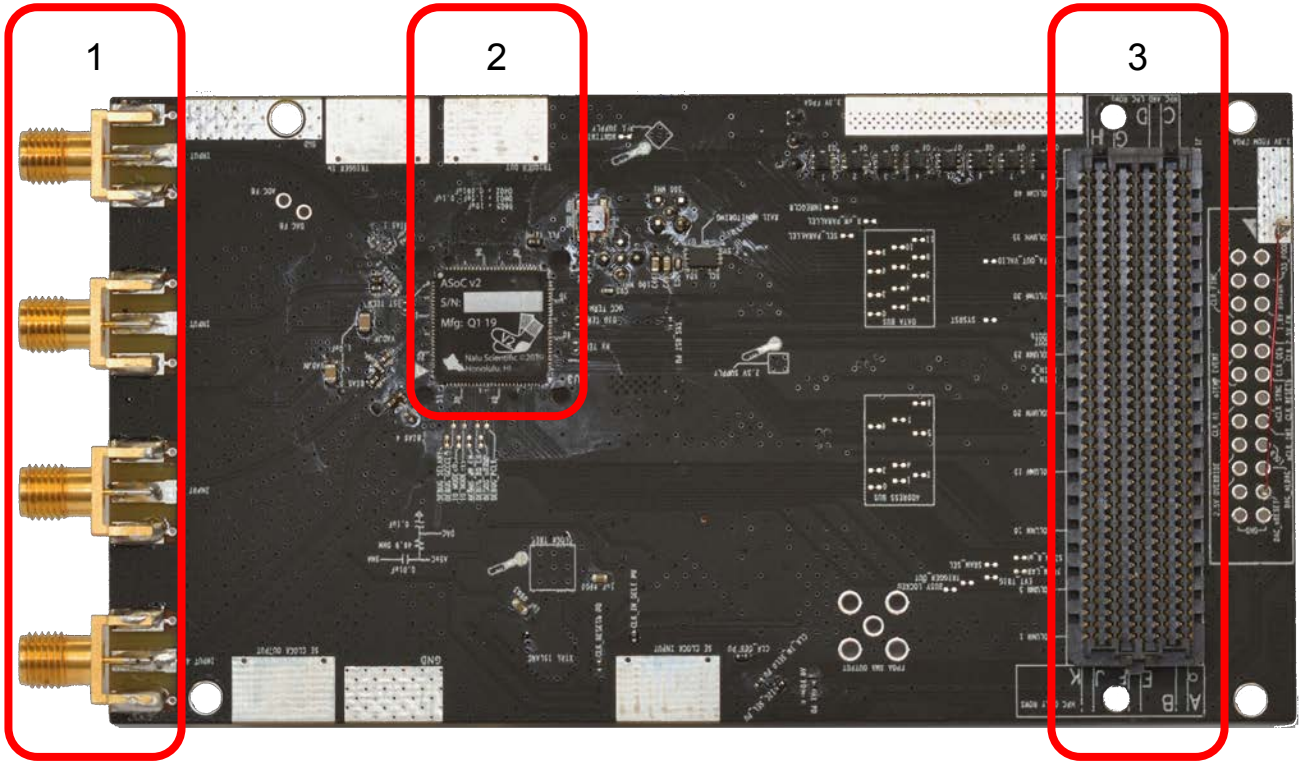


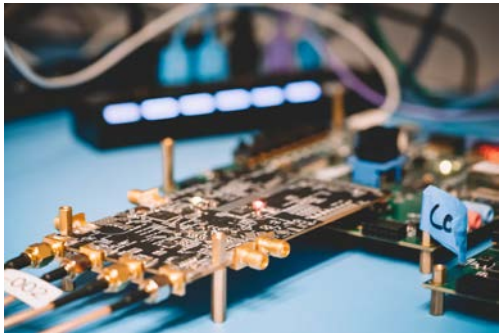


Noise residuals after pedestal subtraction - typical ~2.5 counts = 1.0mV

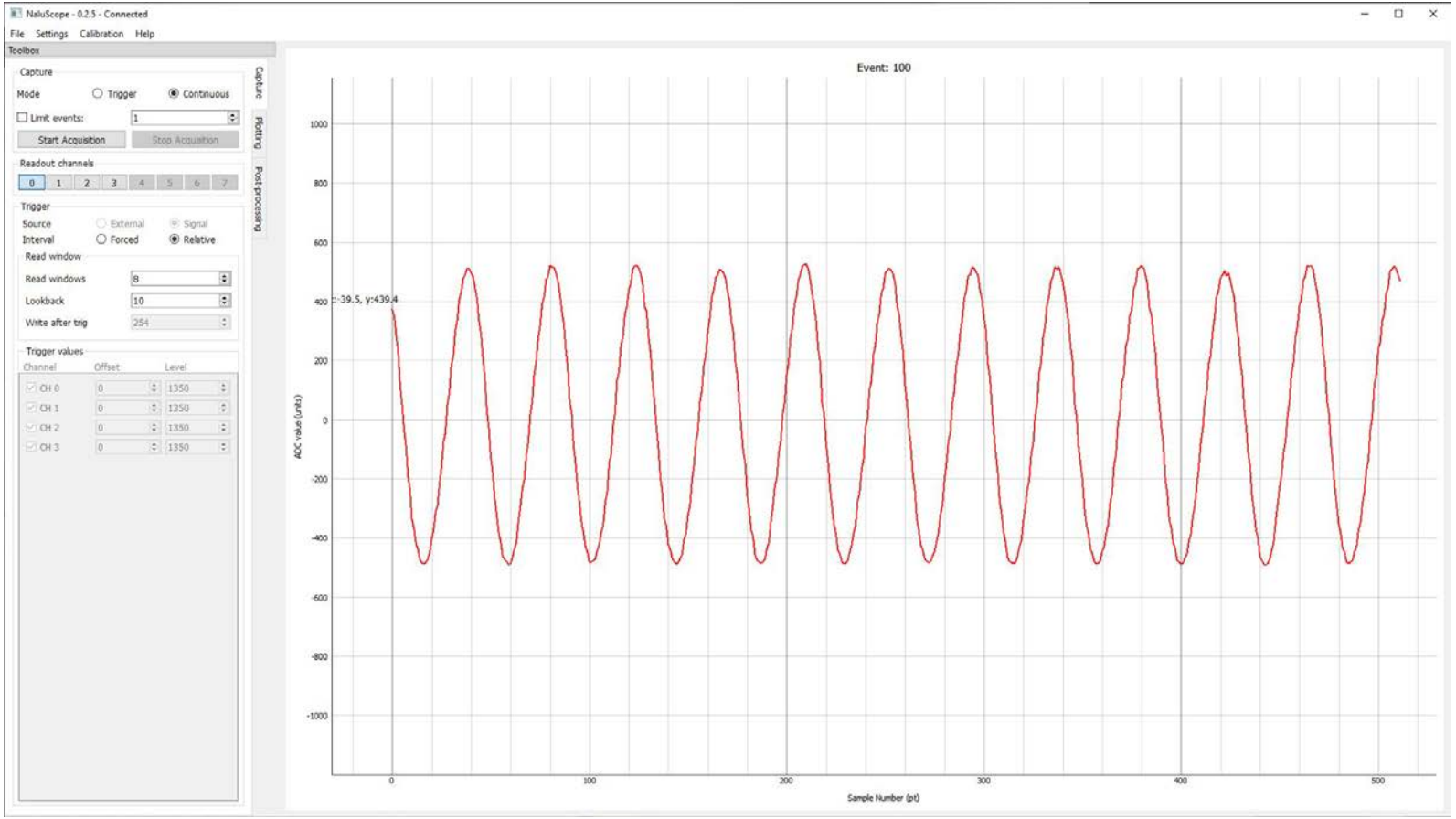
ASoC Eval Card

1. SMA inputs
2. ASoC chip
3. FMC for FPGA card



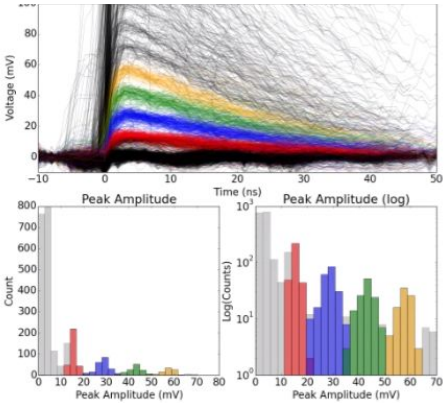


ASoC Common Software and GUI



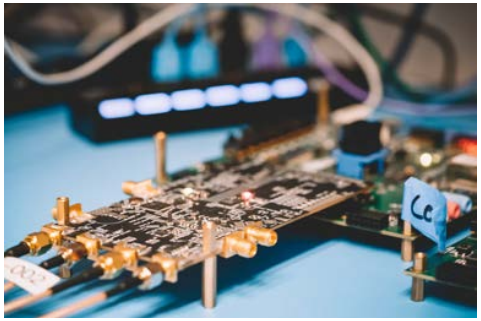
Next Steps for ASoC

- ASoC is now available:
  - Benchtop beta testing
  - Being designed into several detectors (~$200k follow on design contracts)
  - Trade studies for several experiments (~$30k follow on study contracts)
    - Power, data handling, readout rate
    - Integration issues, radiation hardness
- What we learned:
  - How to design, simulate, verify such a large chip
  - Deep knowledge of tools and PDKs
  - Interface with user community, early adopters and distributors
- What is next:
  - More testing under IRD and custom contracts
  - Core and parts of design library will live on in other chips (already cataloged)
  - Adapt testboard for feasibility tests in other areas
  - More targeted measurements
  - Rad testing



Current SoC-ASIC Projects
Open for business!

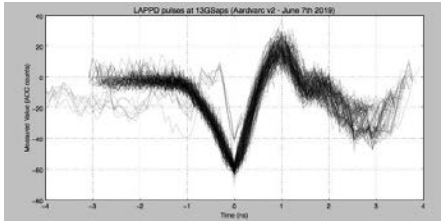
Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-3	0.6	4k	64	80-120	Feb'21
AARDVARC	8-14	2.5	32k	4-8	4-8	Rev 3 avail
AODS	1-2	1	8k	1-4	100-200	Rev 1 avail

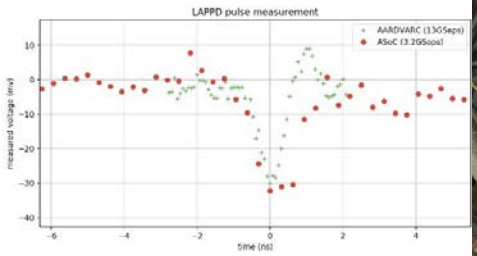


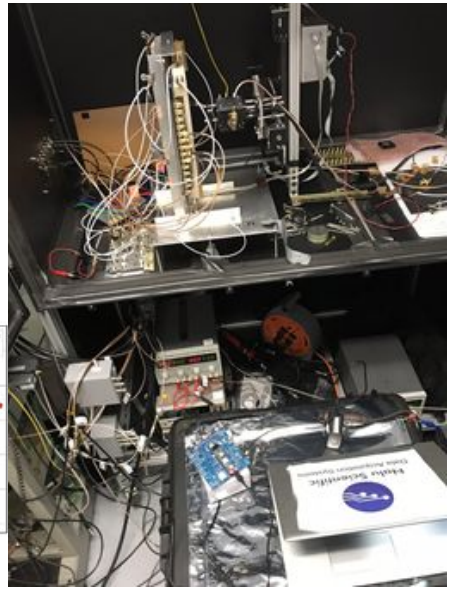
- **ASoC**: Analog to digital converter System-on-Chip
- **HDSoC**: SiPM specialized readout chip with bias and control
- **AARDVARC**: Variable rate readout chip for fast timing and low deadtime
- **AODS:** Low density digitizer with High Dynamic Range (HDR) option

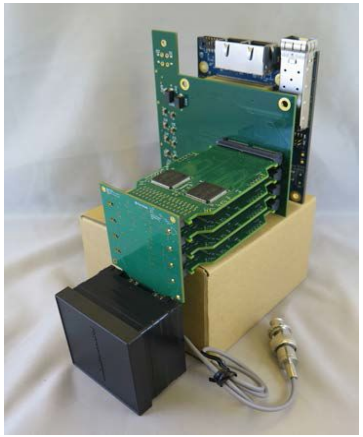
All chips, are designed with commercial grade tools and licenses and can be sold once commercialized.

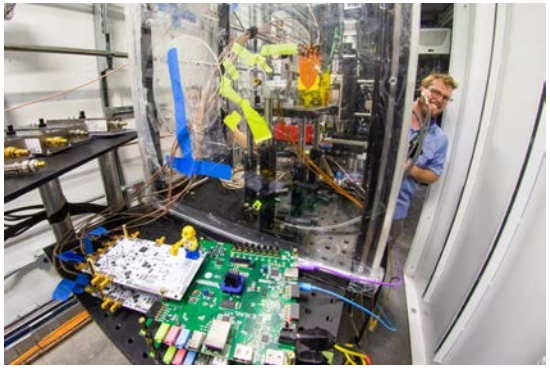
Synergies

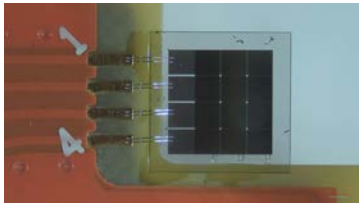










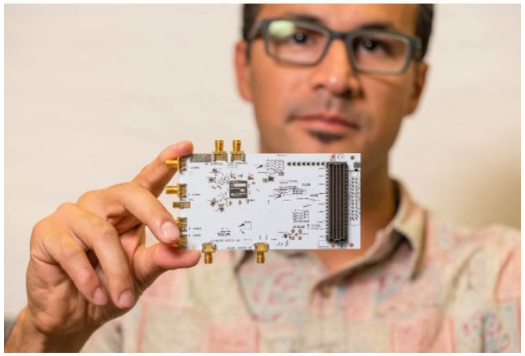


LAPPD EIC-PID Beam Diag.

Getting the Word Out

- Awards (40U40, most innovative, …)
- Attending conferences, trade shows, pitch competitions
- Media attention on restarting/diversifying economy in Hawaii esp post COVID
- New website, Social Media handles: FB, LinkedIn, Twitter

HawaiiBusiness magazine



LEADERSHIP – APRIL 6, 2020

Virtual Interview on COVID-19: Isar Mostafanezhad, Founder and CEO, Nalu Scientific

Booth and AARDVARC Live demo at US-Japan Particle Physics Symposium in Honolulu (April 2019)

Pacific Biz News 40 under 40

Next Top Startup Pitch Competition
Runner up - IMS2019 - Boston

IEEE Young Professionals Panel IMS2019 - Boston

IPAC 2019 booth- Melbourne

Hawaii Biz Magazine
Most Innovative Small Biz of the year

Hawaii Congressman Ed Case visit

Acknowledgements

- US Department of Energy: PMs and staff
- University of Hawaii Department of Physics
- Hawaii Technology Development Corporation (HTDC)
- Incom
- Sandia National Lab
- Brookhaven National Lab
- Jefferson Lab