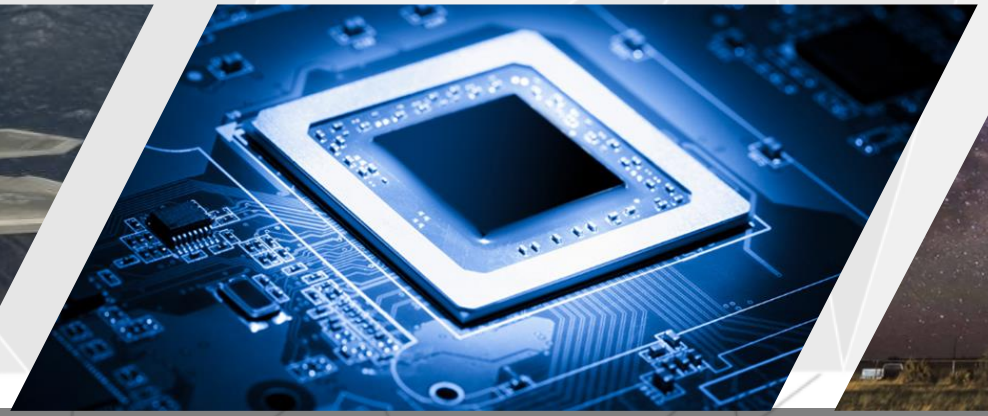
ALPHACORE

ROBUST HIGH-PERFORMANCE MICROELECTRONICS

# Multi-Channel Readout ASIC for Nuclear Physics Experiments

Presented by : Esko Mikkola (Principal Investigator)

DOE-NP SBIR/STTR Exchange Meeting
August 14, 2019


# Outline

- Alphacore Overview
- Alphacore's DOE STTR Phase II Program Overview and Status (Year 2)
- Alphacore's High-Performance Digitizers for Nuclear Physics Experiments
- Summary

# About Alphacore


- Founded in 2012 and located in Tempe, Arizona
- Product areas span:
  - High performance analog, mixed signal, and RF electronics
  - High-speed visible light and infrared camera systems
  - Radiation hard designs and radiation test services
  - Innovative devices ensuring supply chain and IoT cybersecurity

# The Alphacore Team

Alphacore's team is a combination of business and engineering professionals with long histories of delivering products and services to customers who demand state-of-the-art performance.

Our team has had successful careers at companies ranging from start-ups to multinationals including **Raytheon, Texas Instruments, Analog Devices, Bell Labs, Intel, United Technologies,** and **Honeywell**.

Current contracts with DOD (Air Force, Navy, Army, DARPA, MDA, DMEA), DOE, NASA, and NIST.

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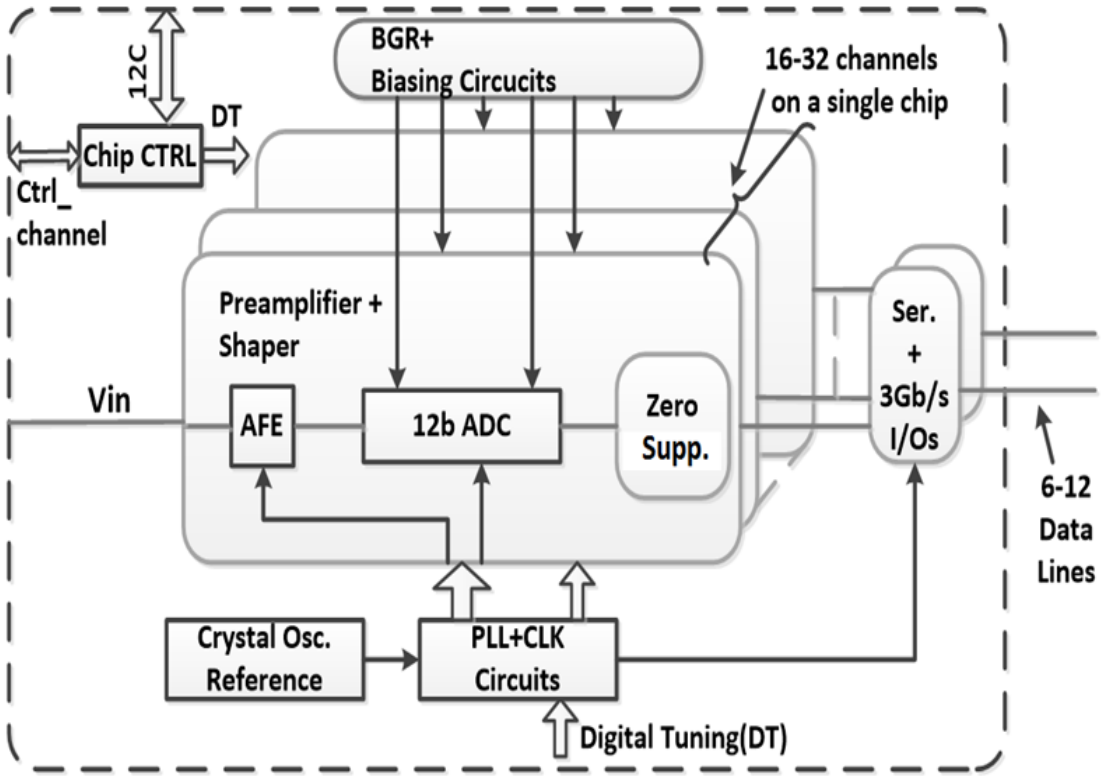
# Multi-Channel Readout IC for Nuclear Physics Experiments

## DOE STTR Phase II Year 2 Overview

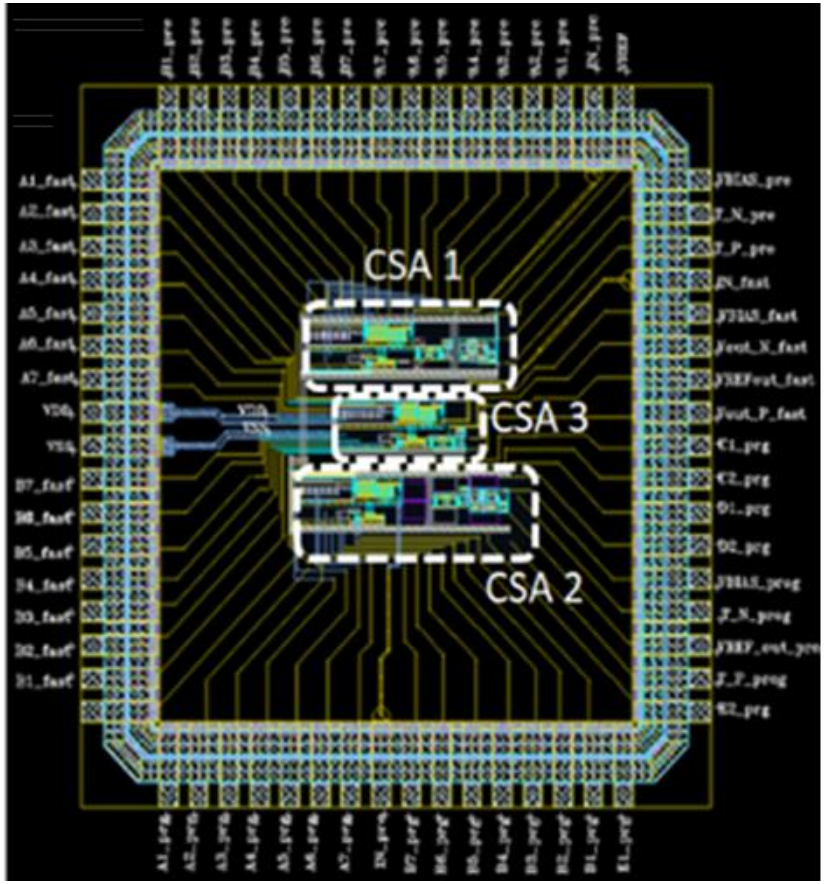
# Program Goals

- Program duration: 24 months
- Status: The funded technical period has ended
- STTR Partner: Arizona State University
- Key goal of this work is to develop versatile and low-cost detector readout solutions, both IP and ICs.
- The IP blocks can be used to relatively quickly build the exact, compact readout ASICs configurations most suitable for a target application when the need arises. Alphacore can build the exact ASIC for a customer in need using the tested IP.
- The Preamplifier and ADC ICs can be directly used for detector readout.
- Alphacore has taped out and tested the following circuits:
  - programmable, multi-channel preamplifier/shaper ICs (charge sensitive amplifiers )
  - multi-channel ADCs with varying specifications
  - I/O interface suitable for large data bandwidths




***An example of a detector readout ASIC that can be built using Alphacore's IP blocks***

# Charge Sensitive Amplifiers (CSA)

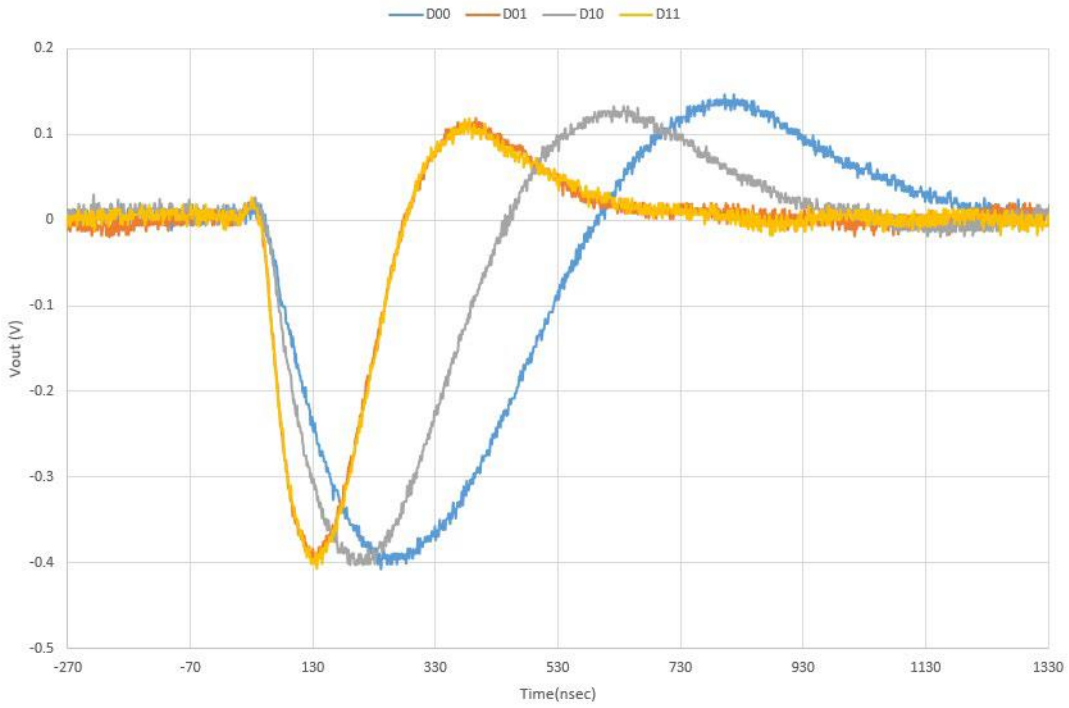



*Test chip for 3 CSAs*

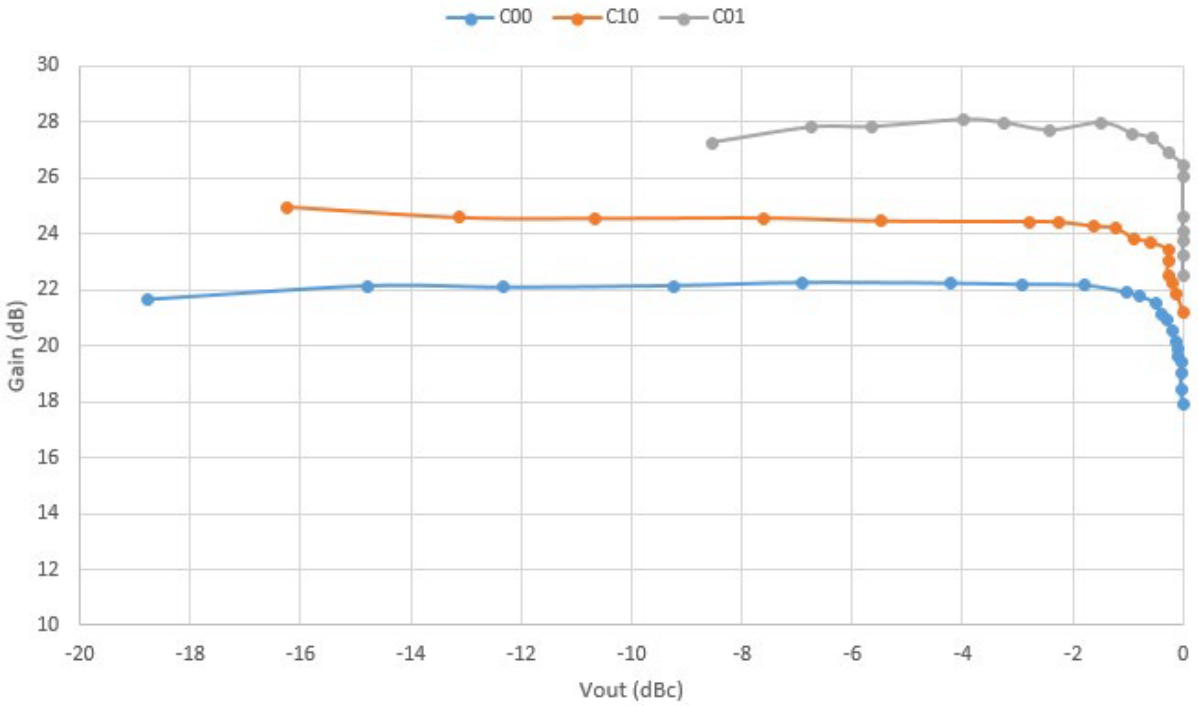
| # Simulated specifications | CSA1 with programmability | CSA2 | CSA3 |
|---|---|---|---|
| Equivalent Noise Charge(ENC) worst case (electrons) | 556 | 1.8K | 480 |
| ENC rate (electrons/pF) | 22.25 | negligible | 22.25 |
| Rise Time typical (ns) | 92 | 208 | 20 |
| Gain (mV/fC) | 30.45 | 29.8 | 2.3 |
| Rise time programmability (ns) | 50n-200 | NA | NA |
| Gain Programmability (mV/fC) | 15-60 | NA | NA |
| Fully Differential Output | Yes | Yes | Yes |
| Common Mode of Full Differential Output | 0.8-1 | 0.8-1 | 0.8-1 |
| Shaper Circuit | Yes | Yes | No |

# CSA1 Test Results

Noise was measured as 712 electrons for 0.7pF detector capacitance



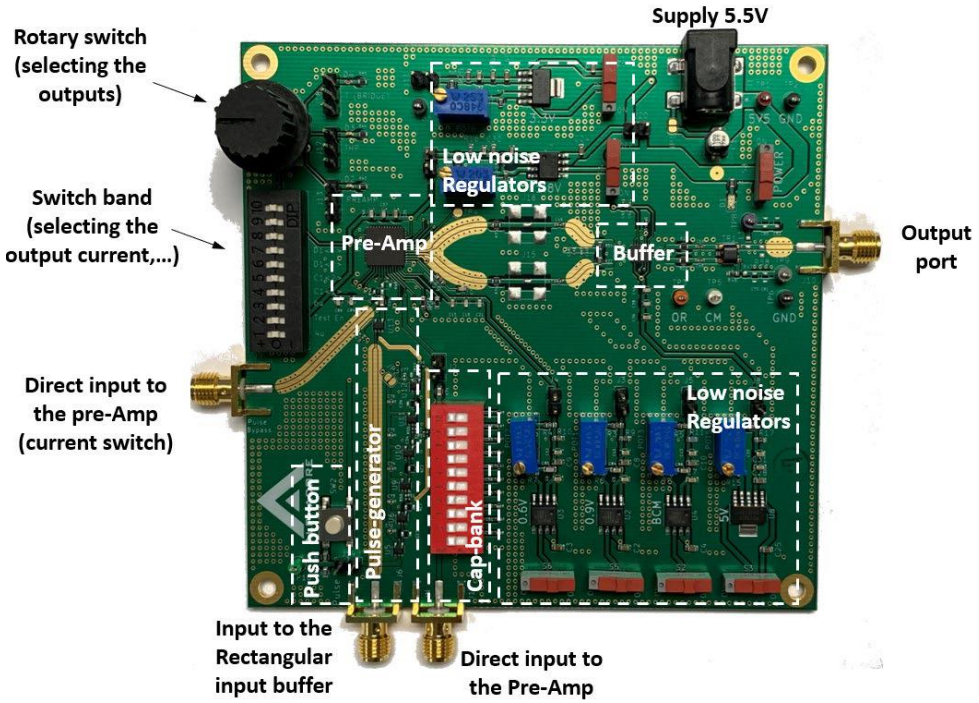

Shaping time programmability measurements



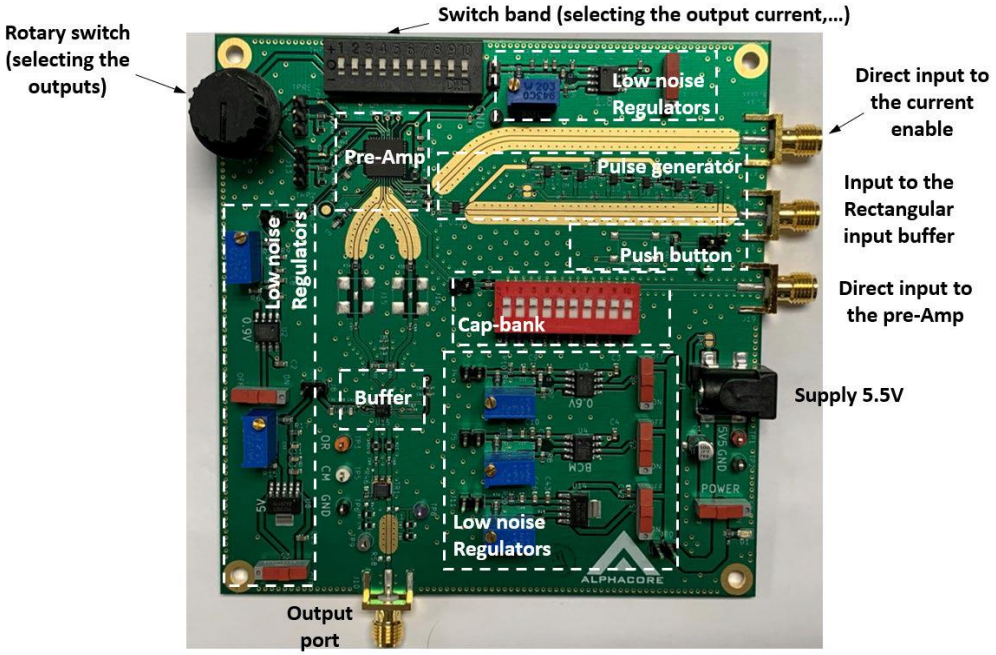

Gain programmability measurements

# CSA Evaluation Boards

CSA evaluation boards and/or packaged chips are available for customers. 16-ch preamplifiers are available as bare die.

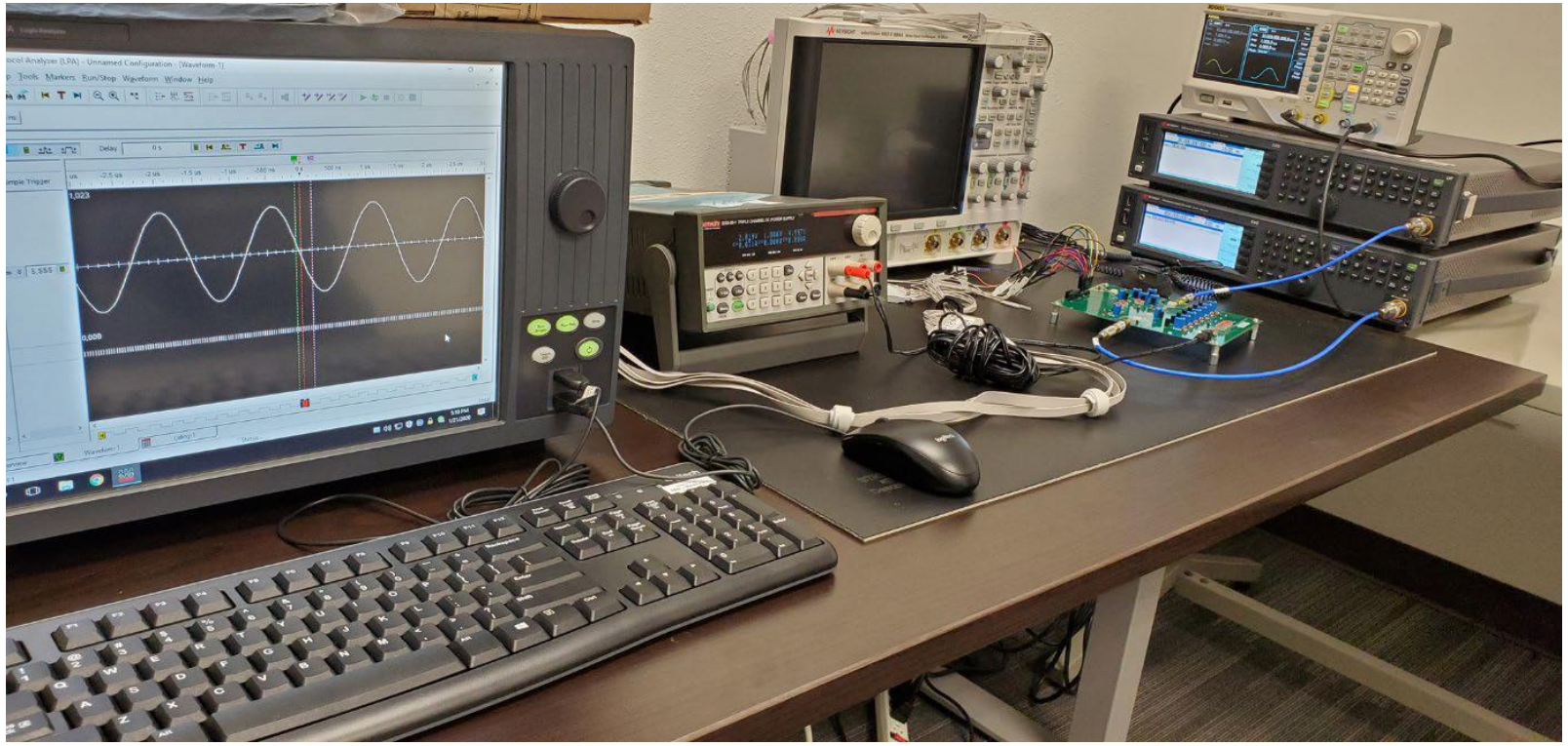



CSA evaluation board 1



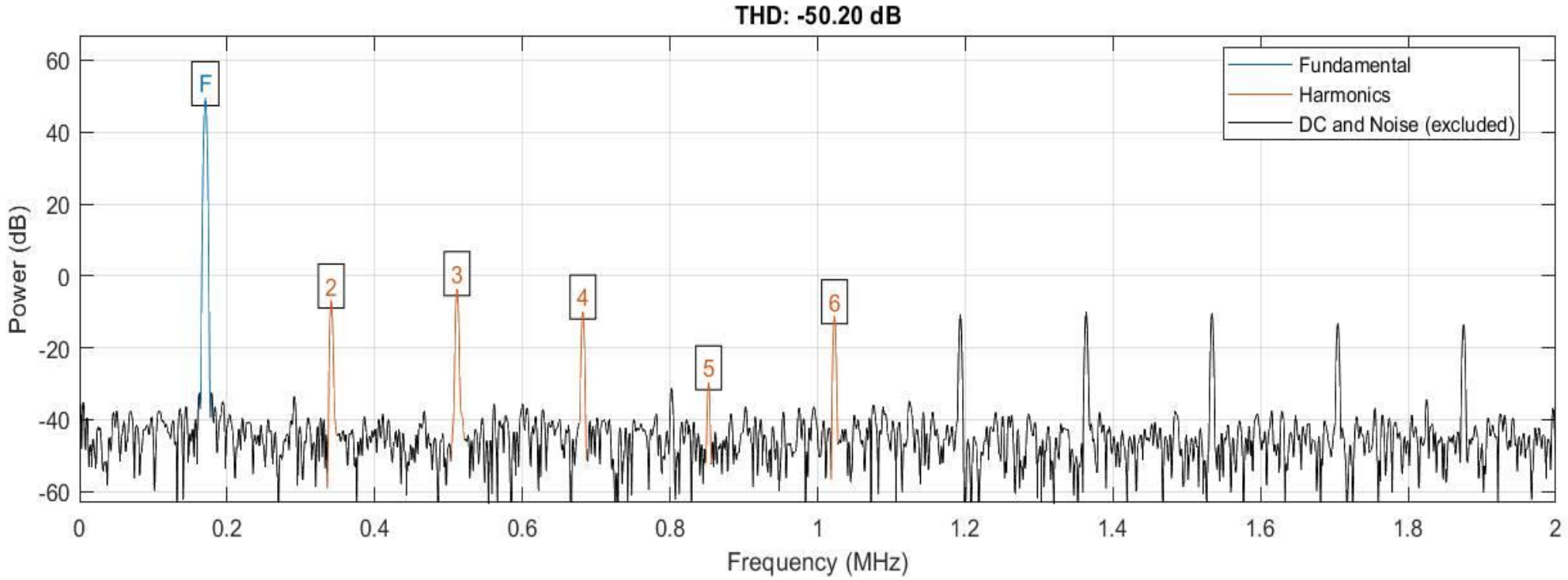

CSA evaluation board 2

# Analog to Digital Converters Test Results



ADC Test Setup

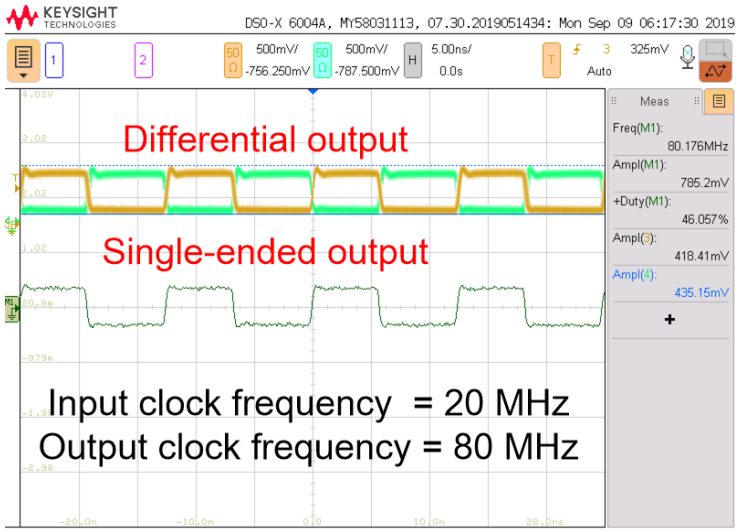
# 10-bit, 50MS/s, 7mW ADC Test Results

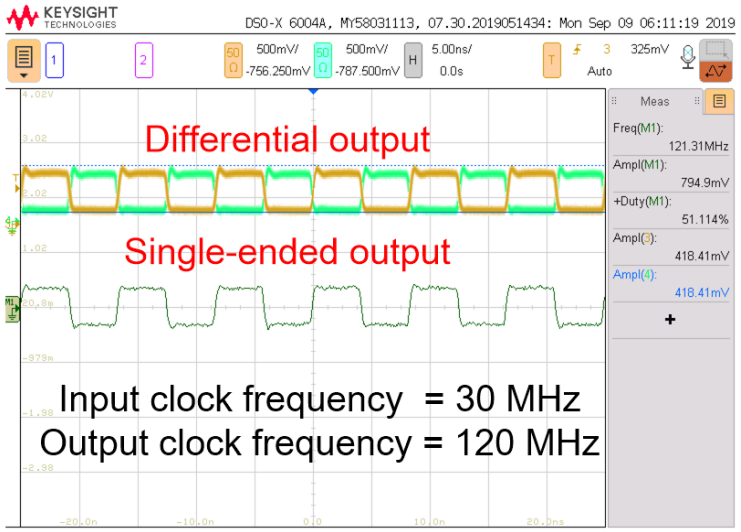


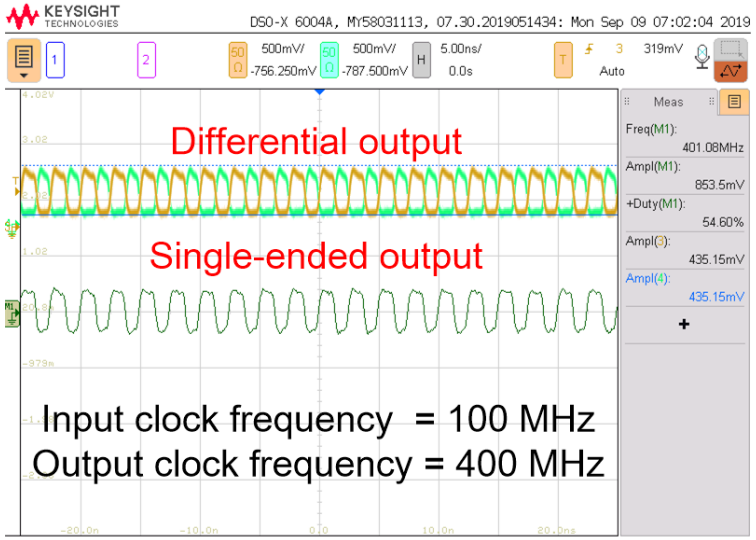

SINAD = 44.04 dB
SNR = 45.24 dB
SFDR = 52.83 dB
THD = -50.20 dB
ENOB = 7.31 Bits

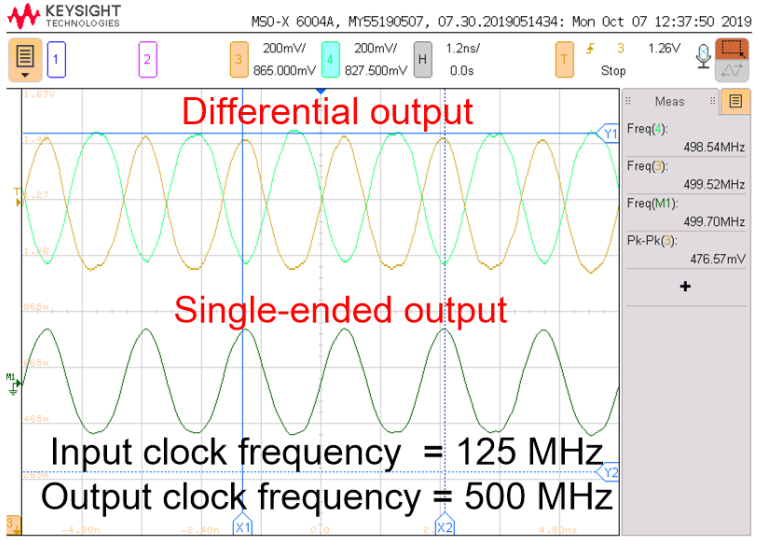
ADC test boards and/or packaged chips are available for customers. 6-ch ADCs are available as bare die.

# Low-power High-Bandwidth I/O Interface Test Results



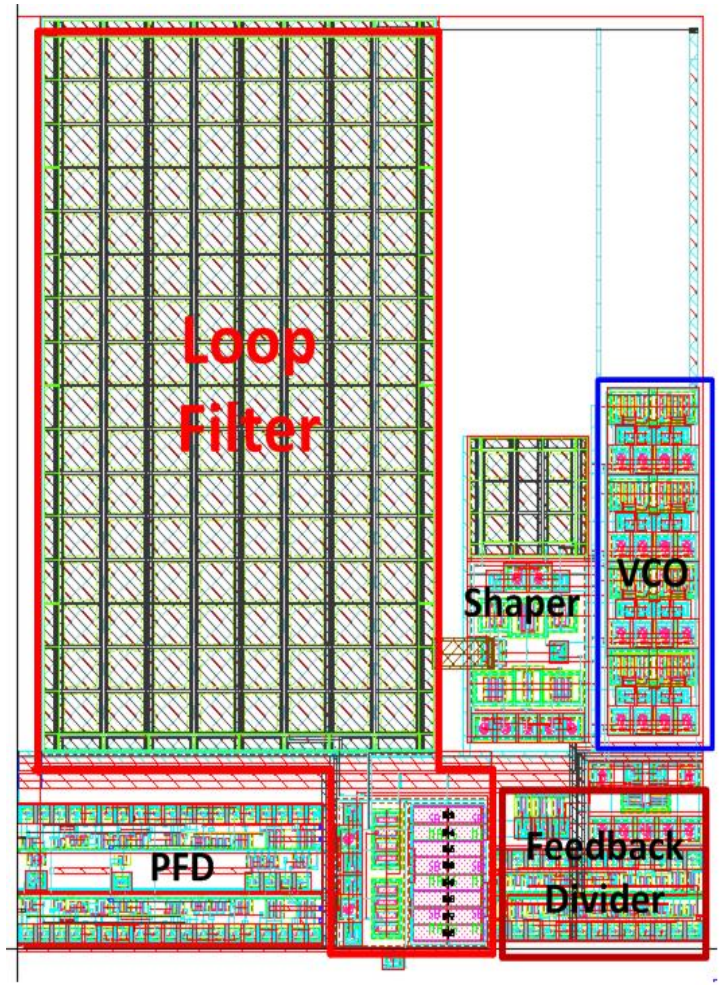



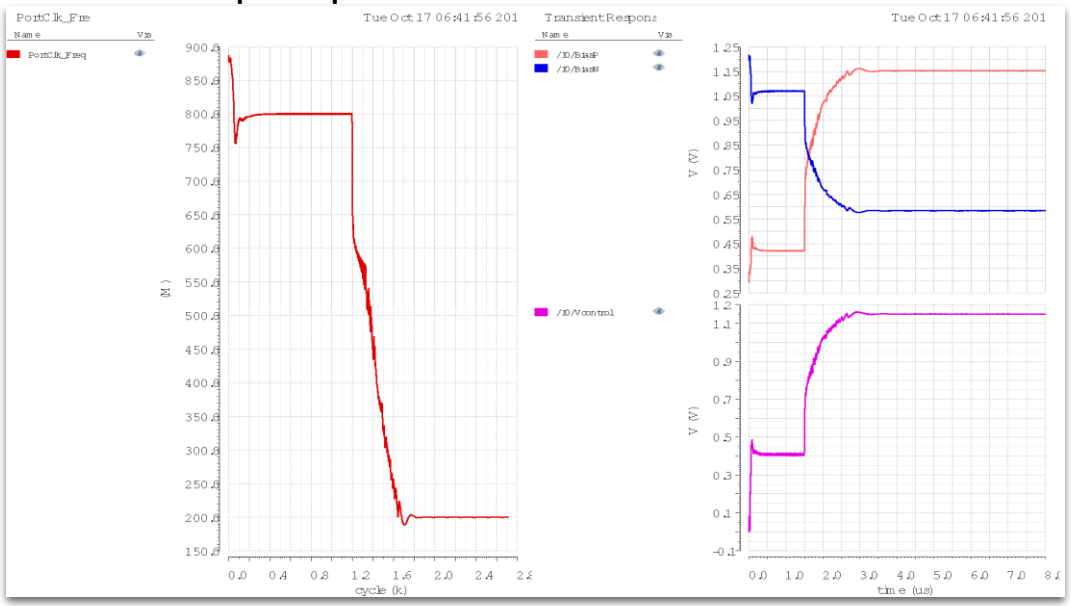
# General Purpose PLL for Serializer Test Results

## Alphacore's PLL

- Output freq. range: 80 to 800 MHz
- Power at $1.8\ V$ supply: $3.69\ mW$




Step response from 200MHz to 800MHz

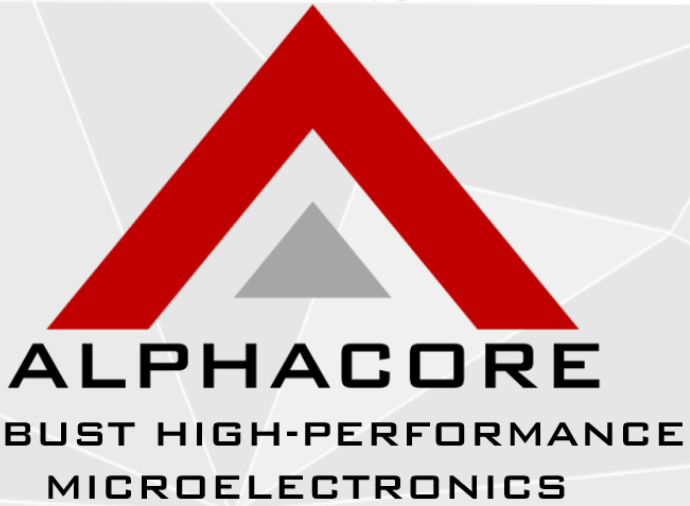


A performance summary of Alphacore's PLL

| Input Freq. (MHz) | Output Freq. (MHz) | Lock time | Phase noise | RMS jitter (ps) | Peak-to-peak Jitter(ps) |
|---|---|---|---|---|---|
| 50 | 200 | 2.3us | -144.16dBc/Hz @10MHz | 0.339 | 2.09502 |
| 75 | 300 | 1.5us | -141.688dBc/Hz @10MHz | 0.304 | 1.87872 |
| 100 | 400 | 1.2us | -144.4679dBc/Hz @10MHz | 0.178 | 1.10004 |
| 125 | 500 | 980ns | -145.7717dBc/Hz @10MHz | 0.134 | 0.82812 |
| 150 | 600 | 880ns | -145.8564dBc/Hz @10MHz | 0.119 | 0.73542 |
| 200 | 800 | 420ns | -144.3804dBc/Hz @10MHz | 0.113 | 0.69834 |
| Assume the Bit error ratio is $10^{-3}$ | | | | | |

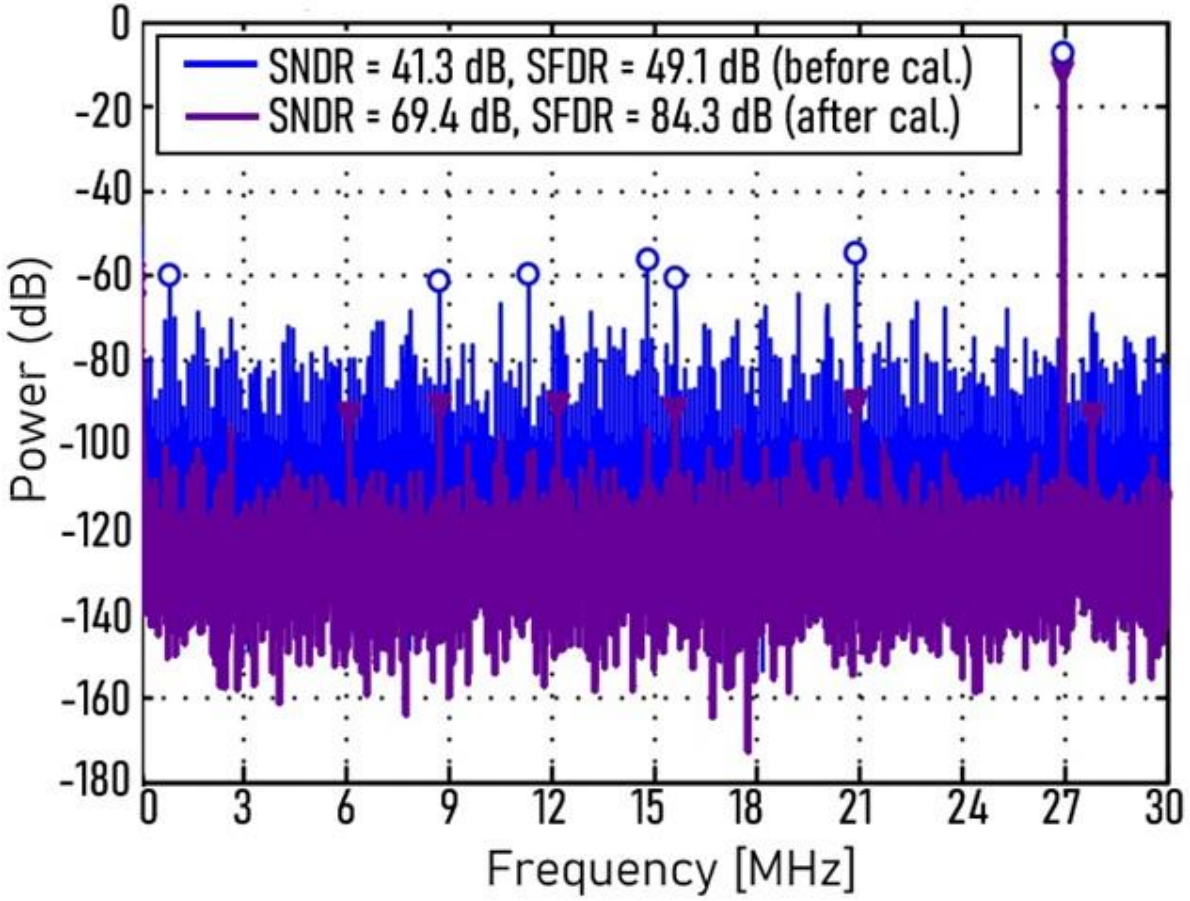



13




# Silicon Evaluated High-Performance Digitizers for Nuclear Physics Experiments

# 12-bit, 50MS/s, 63mW ADC Test Results

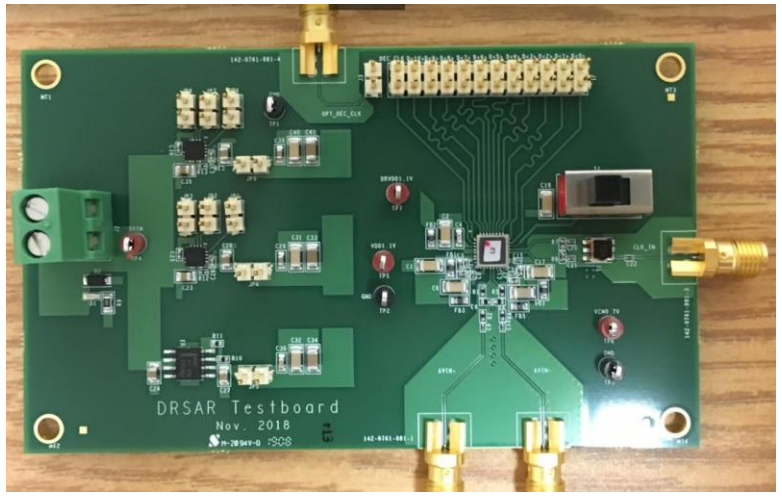


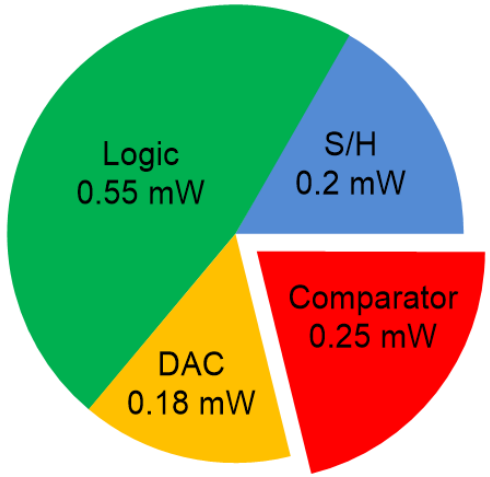

ADC test boards and/or packaged chips are available for customers.

# IP Library of 22nm and 28nm CMOS High-Performance Low-Power ADCs

- The library contains more than ten 300MS/s – 20GS/s ADCs.
- They are radiation tolerant designs and available for nuclear physics experiments.
- The ADCs can be delivered with “full raw data stream output interface” and/or with “digital waveform sampling buffer” FIFO output interface. The much simpler FIFO interface is enough for most nuclear physics experiments and it enables very low power dissipation and simpler board design.
- Next slides show examples of the library elements.
- **Please contact Alphacore for more details (test results, channel quantity, test boards, pricing...)**

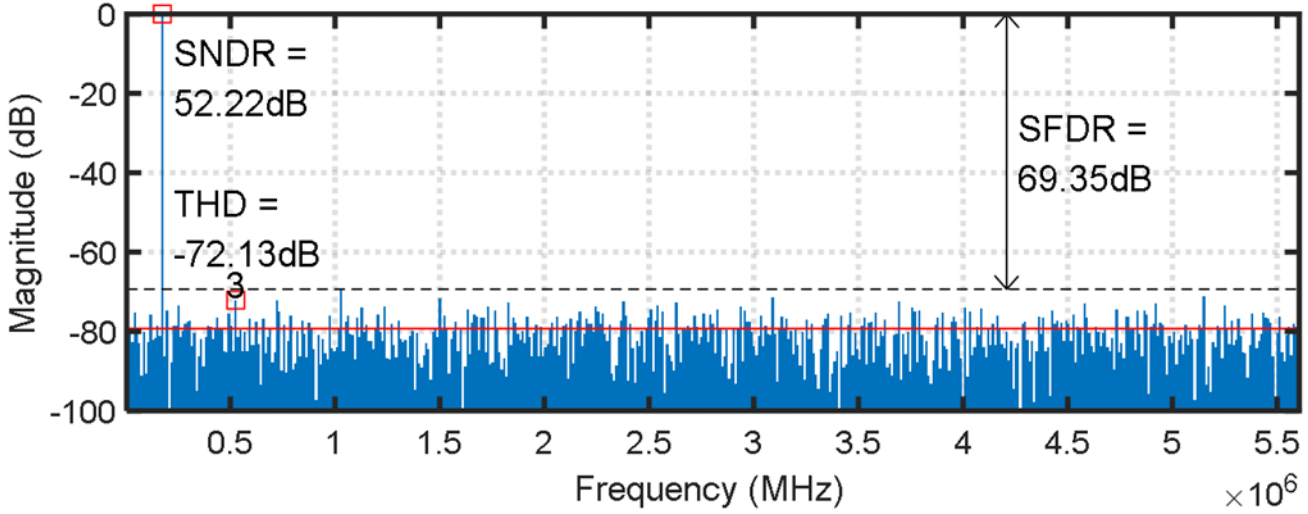
# A 10B500M, 10bit, 500MS/s, Ultra Low Power ADC

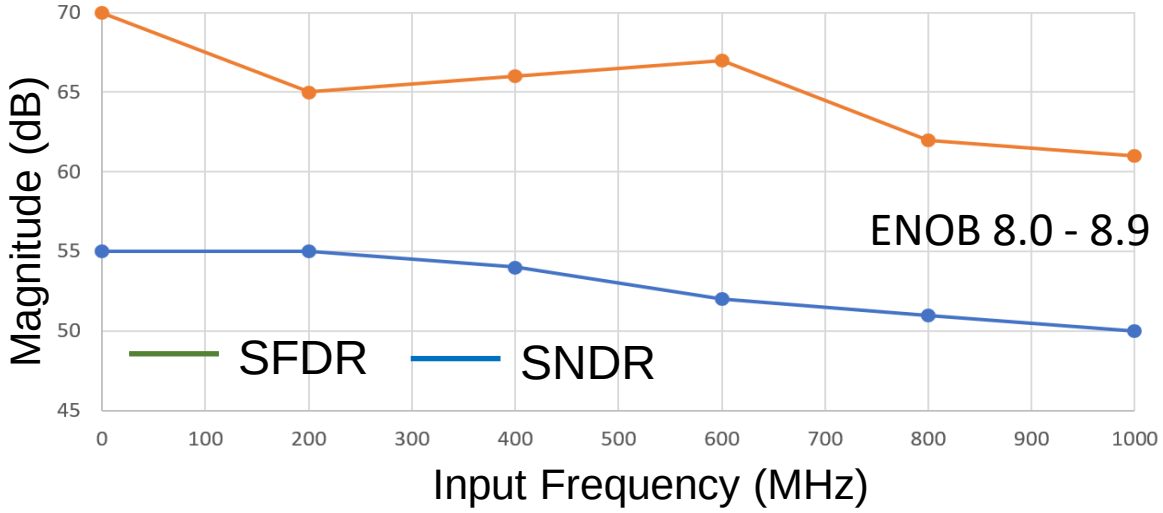



- Single channel ADC with wide input bandwidth (beyond 4th Nyquist zone)
- ENOB 8.0 - 8.9 over four Nyquist bands
- Ultra Low Power <1.18 mW (FOM <6.0fJ/conv.)
- **Can be used as the unit channel in a 10-bit, time-interleaved ADC with sample rate of tens of GS/s**

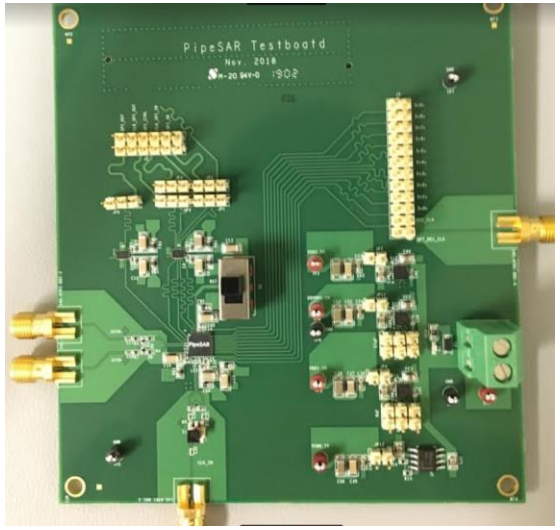
# A 10B500M, 10bit, 500MS/s, Ultra Low Power ADC



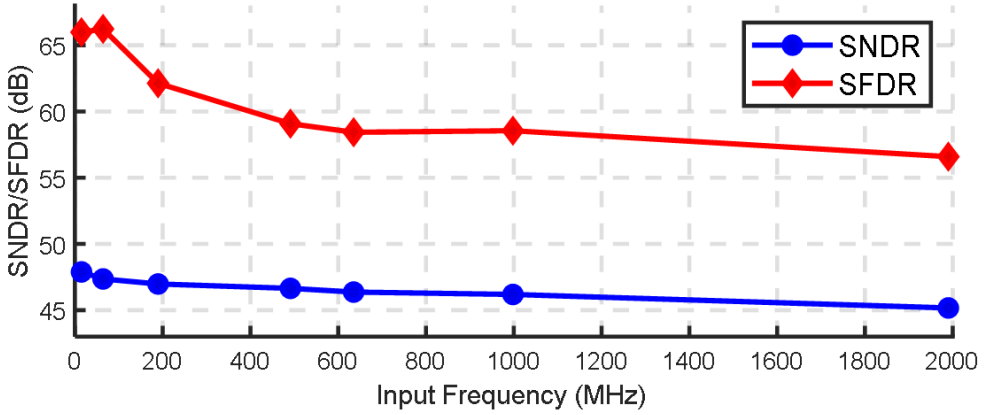

- Single channel ADC with wide input bandwidth (beyond 4th Nyquist zone)
- ENOB 8.0 - 8.9 over four Nyquist bands
- Ultra Low Power <1.18 mW (FOM <6.0fJ/conv.)
- **Can be used as the unit channel in a 10-bit, time-interleaved ADC with sample rate of tens of GS/s**

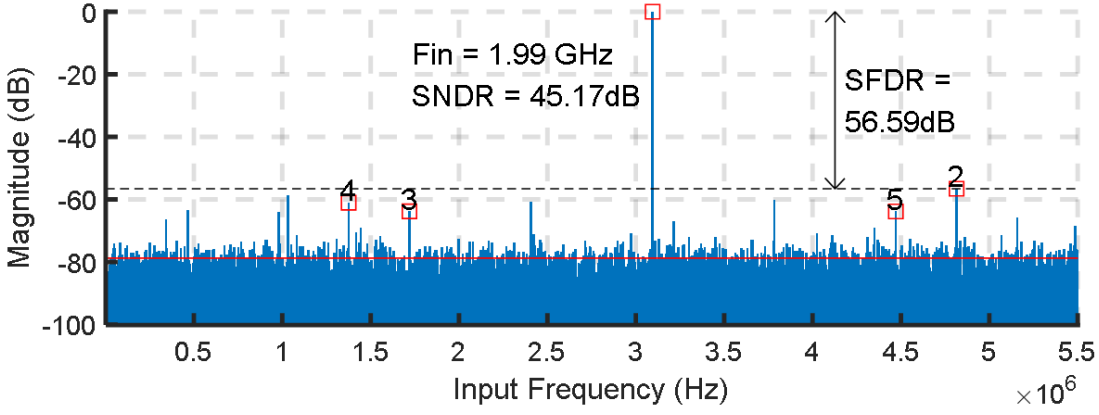
# A9B1G, Wide Input BW, 9-bit, 1GS/s ADC



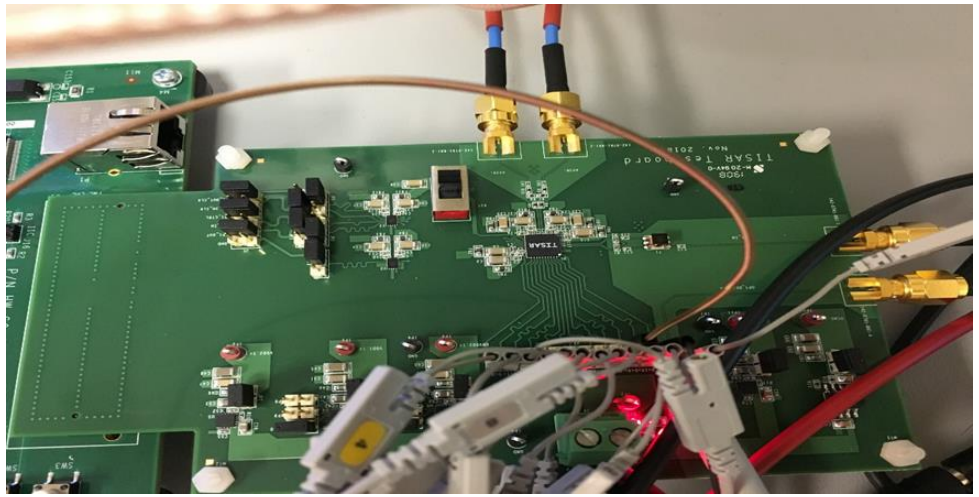

- Single channel with wide input bandwidth (beyond 4th Nyquist zone)
- ENOB stays within 7.2-7.7 over the first four Nyquist bands
- Power <2.1mW (FOM = 10fJ/conv)
- Can be used as the unit channel in a 10-bit, time-interleaved ADC with sample rate of tens of GS/s

Output decimated by a factor of 91 in this testing set up

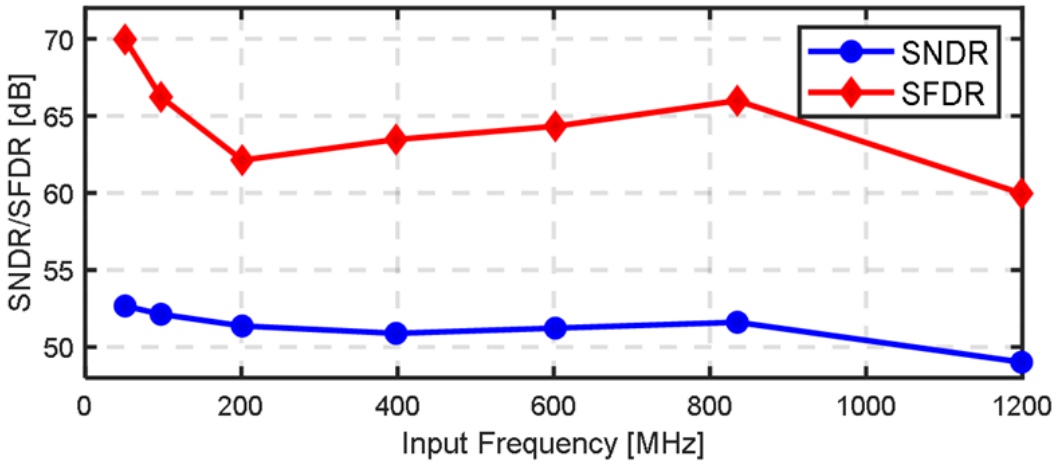


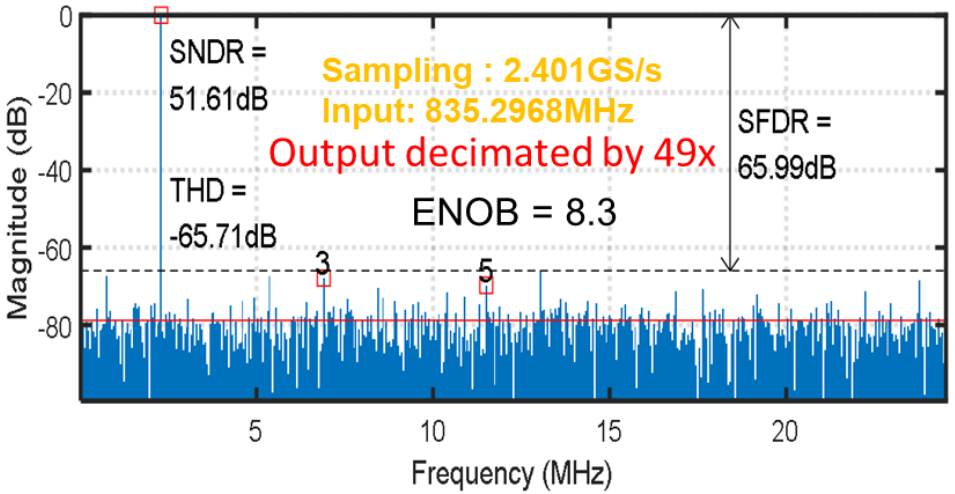



# A10B2G, 10 bit, 2.4GS/s, Ultra Low Power ADC

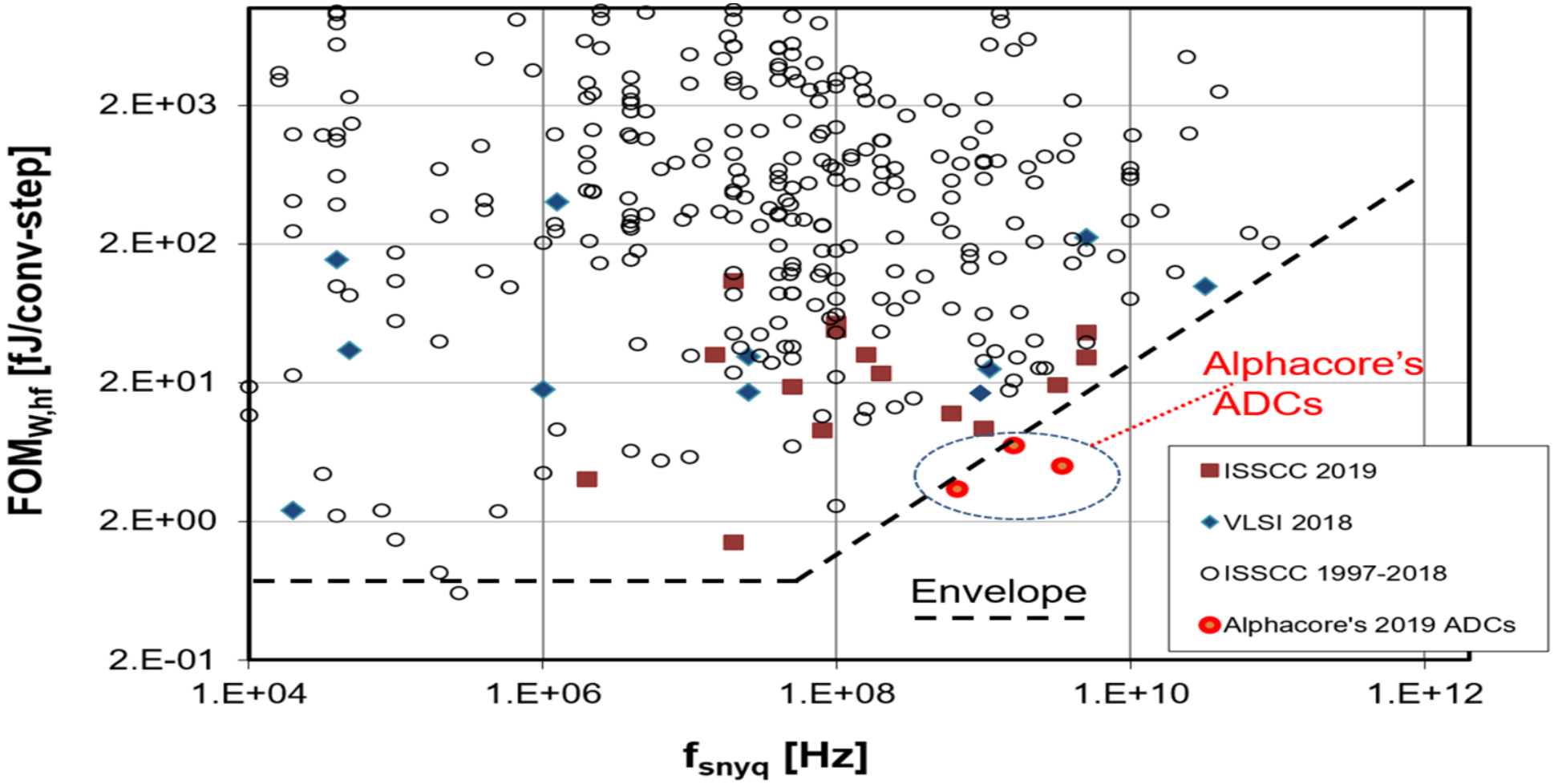


- The ADC has a 8-way interleaved architecture, with combined sampling rate of 2.4GS/s. The sampling rate is limited by on-chip clock buffers. Optimized buffers would deliver up to 3.2GS/s with 6mW of additional power.
- We can interleave 16-way(on-chip) to achieve 6.4GS/s for continuous digitization with no dead time
- The developed calibration algorithm has been shown to be very effective for the calibration of interleaving spurs, in this case yielding SFDR of 60-70 dB and ENOB that varies from 7.9 bits to 8.5 bits in the first Nyquist band.
- Power = 6 mW (FOM = 6.9fJ/conv)

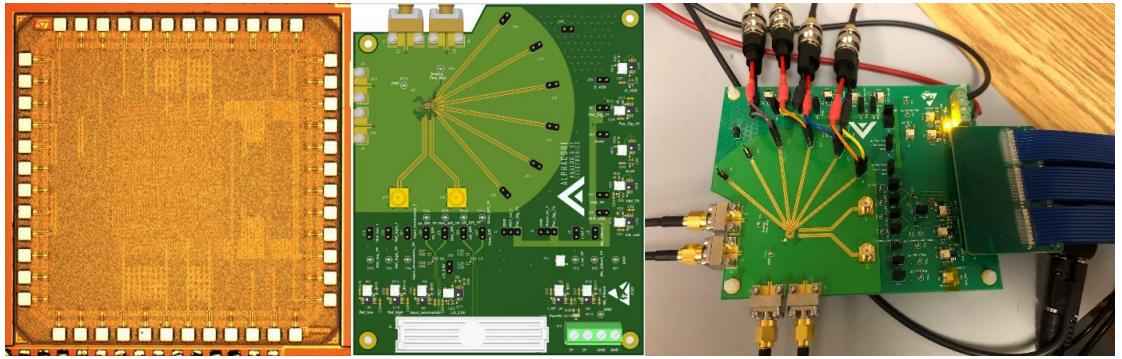


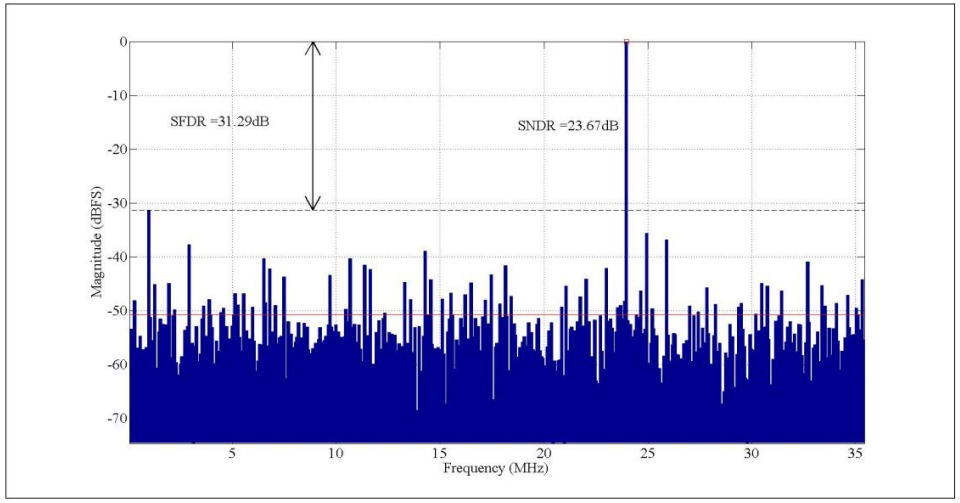
# Alphacore's Ultra Low Power ADCs Walden Chart comparison: FOM vs Speed



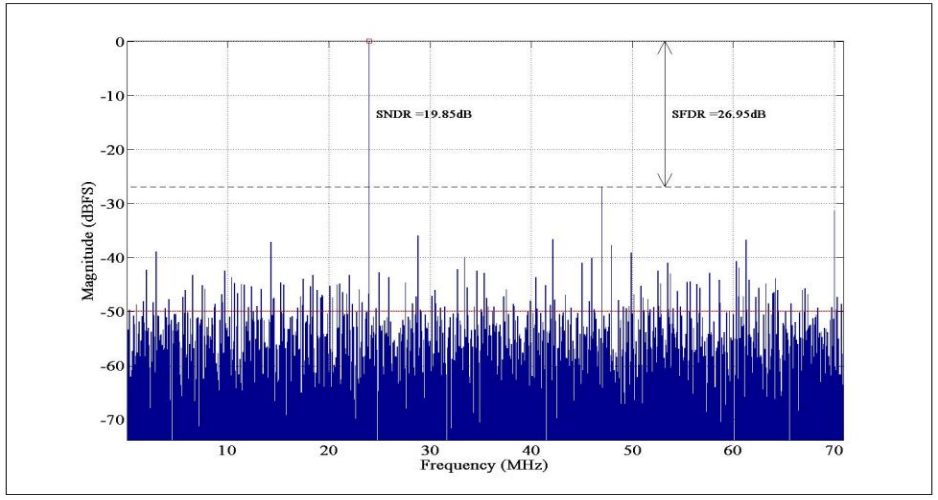
# 20GS/s 20GHz 6bit ADC



- IP functionality testing completed with a COB package.
- Development of a high-speed custom package with the lowest possible parasitics has been planned. The expected performance with a proper package is >4.5 ENOB, >20GS/s, >20GHz and <300mW.
- The COB package and our current test setup allows testing the ADC at 16GS/s and 8GHz.
- The goal is to be able to test beyond 20GS/s sample rate and 20GHz input bandwidth




*ENOB is 3.7 when tested at 9GS/s and 8GHz input bandwidth*




*Measurements achieved for sampling frequencies up to 17.2GS/s with ENOB up to 3.3 bits*

# Alphacore's IP Library

The table below summarizes Alphacore's high-performance IP cores. Radiation-tolerant versions are available for all of these cores.

| # | Type | Model | Device | Type | Foundry | Resolution [bits] | Sampling Rate [MS/s] | Input BW [MHz] | ENOB [bits] | SFDR [dBc] | Power [mW] | Status |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | IP | A10B320M | ADC | SAR | STMicro 28nm | 10 | 320 | 1,300 | 9 | 69 | 0.7 | Silicon-validated |
| 2 | IP | A10B500M | ADC | SAR | STMicro 28nm | 10 | 500 | 3,000 | 8.9 | 64 | 1.2 | Silicon-validated |
| 3 | IP | A8B620M | ADC | Hybrid | STMicro 28nm | 8 | 620 | 3,000 | 7.4 | 55 | 1.6 | Silicon-validated |
| 4 | IP | A9B1G | ADC | SAR | STMicro 28nm | 9 | 1,000 | 3,000 | 7.7 | 58 | 2.7 | Silicon-validated |
| 5 | IP | A10B2G | ADC | SAR | STMicro 28nm | 10 | 2,400 | 4,000 | 8.4 | 66 | 6 | Silicon-validated |
| 6 | IP | A6B5G | ADC | Flash | STMicro 28nm | 6 | 5,000 | 10,000 | 5.2 | 37 | 14 | Silicon-validated |
| 7 | IP | A10B5G | ADC | Hybrid | GF 22nm | 10 | 5,000 | 10,000 | 8.8 | 64 | 19 | Verified GDSII |
| 8 | IP | A8B10G | ADC | Hybrid | GF 22nm | 8 | 10,000 | 20,000 | 7.0 | 53 | 39 | Verified GDSII |
| 9 | IP | A6B12G | ADC | Hybrid | GF 22nm | 6 | 12,500 | 12,000 | 5.3 | 39 | 13 | Verified GDSII |
| 10 | IP | A4B10G | ADC | Flash | STMicro 28nm | 4 | 10,000 | 25,000 | 3.7 | 27 | 62 | Silicon-validated |
| 11 | IP | A6B10G | ADC | Flash | STMicro 28nm | 6 | 10,000 | 25,000 | 4.9 | 40 | 212 | Silicon-validated |
| 12 | IP | A4B20G | ADC | Flash | STMicro 28nm | 4 | 20,000 | 25,000 | 3.1 | 26 | 104 | Silicon-validated |
| 13 | IP | A6B20G | ADC | Flash | STMicro 28nm | 6 | 20,000 | 25,000 | 4.5 | 37 | 376 | Silicon-validated |
| 14 | IP | A6B10G | ADC | Flash | GF 22nm | 6 | 10,000 | 25,000 | 5.1 | 44 | 114 | Verified GDSII |
| 15 | IP | A6B20G | ADC | Flash | GF 22nm | 6 | 20,000 | 25,000 | 5.0 | 42 | 388 | Verified GDSII |
| 16 | IP, IC | A6B20G-IC | ADC | Flash | GF 22nm | 6 | 20,000 | 20,000 | 4.9 | 40 | 743 | Verified GDSII |
| 17 | IP | A8B40G | ADC | Hybrid | GF 22nm | 8 | 40,000 | 25,000 | 6.5 | 54 | 194 | Verified GDSII |
| 18 | IP | A16B160M | ADC | Hybrid | GF 22nm | 16 | 160 | 200 | 13.1 | 86 | 48 | Verified SPICE netlist |
| 19 | IP | D12500M | DAC | Current Steering | GF 55nm | 12 | 500 | 1,000 | 9.8 | 72 | 36 | Silicon-validated |
| 20 | IP | D6B6G | DAC | Current Steering | GF 22nm | 6 | 6,000 | 9,000 | 5.5 | 42 | 15 | Verified GDSII |
| 21 | IP | D6B12G | DAC | Current Steering | GF 22nm | 12 | 6,000 | 6,000 | 9.0 | 63 | 121 | Verified SPICE netlist |
| 22 | IP | PLL13G | PLL | Fractional N | TSMC 130nm | 5.5GHz – 13.5GHz, 350fs jitter | | | | | | Silicon-validated |

# Summary

- The DOE Nuclear Physics STTR Phase II program discussed in this presentation strengthens Alphacore's digitizer and readout ASIC family offered to Nuclear Physics, Scientific, Space and Defense customers.
- The program is at the end of the Year 2.
- This presentation also introduces Alphacore's silicon evaluated ADCs and other IP relevant to Nuclear Physics researchers.
- Alphacore encourages the researchers to contact us for IP and ICs availability.

# Acknowledgement

Work on this program was funded by Department of Energy / Nuclear Physics, Grant #DE-SC00017074.

We especially appreciate the guidance by Drs. Manouchehr Farkhondeh and Michelle Shinn.

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MICROELECTRONICS

# Questions?