AN ASIC WITH A LOW POWER MULTICHLANNEl ADC FOR ENERGY AND TIMING MEASUREMENTS
OUTLINE

• The Company, its Specialization/Expertise
• Phase II objective
• Multichannel ADC for energy and timing measurements specifications
• Motivation
• ADC core architecture and implemented calibrations
• Digital architecture
• ADC data output interface
• Event-driven backend
• ASIC layout / floorplan
• ADC power consumption and performance
• Project schedules, milestones, deliverables and conclusions
COMPANY

- Pacific MicroCHIP Corp. is incorporated in 2006.
- It is headquartered in Culver City, California
- Main focus – providing IC/ASIC design services and turnkey solutions.
CORE EXPERTISE

- Analog (ADC/DAC, CTF, VGA, BG, LDO)
- Mixed Signal (PLL, CDR, SerDes, MDrv, TIA)
- RF (LNA, Mixer/Modulator, PA)
- Digital (RTL, Synthesis, P&R, Timing Closure, DFT, Verifications)
- Layout (SiGe/CMOS) down to 7nm
PHASE II OBJECTIVE

• To design circuits and layout for the ADC ASIC.
• To fabricate the chip.
• To package the chips.
• To develop the test PCB and socket for the ASIC.
• To develop a GUI and a testbench.
• To test and characterize the ADC ASIC.
• To prepare a datasheet for marketing.
• To submit deliverables to the DoE.
FEATURES:
• 32 independent channels
• Programmable sampling rate of 200/100/50 MS/s
• 1Vpp differential input signal
• ENOB > 10-bit
• Programmable input signal bandwidth 0.1-0.3 GHz
• Integrated event-driven digital backend
• JESD204B output data interface
• Extended temperature range -40C..+125C
• Low power consumption 5 mW / channel (w/o interface)
• I2C interface for ASIC control
MOTIVATION (The Problem)

- Required minimum communication data rate between ADCs and FPGA for 32 channels is $32 \times 12\text{bit} \times 65\text{MSps}=24.96\text{Gbit/s}$
- Using multiple ASICs

Large amount of wiring increases:
- detector congestion,
- volume,
- power consumption,
- cost
MOTIVATION (The Solution)

- 32 independent ADC channels with integrated digital back-end for event detection and recording
- Only 50Mbit/s output data rate
- Raw data output through JESD204B
- Low power consumption
- Simplified PCB design and wiring
- Using less components increase reliability
- Dual output data interface
ADC CORE ARCHITECTURE

FEATURES:

• 12b SAR ADC architecture
• Segmented 3t-9b CDAC
• Optional external/internal ADC reference voltage source
• Fractional reference voltage
• Dual comparator
• Asynchronous logic
• Built-in FSM for comparator offset compensation
• Built-in FSM for CDAC non-linearity calibration

ADC CORE BLOCK DIAGRAM:

ADC TIMING DIAGRAM:

1ns

Track/sampling

4ns

Conversion

12-bit 200MS/s ADC
Clock generator
Bootstrap sampling switch
CDAC-Diff
C-DAC
C-DAC
C-DAC
REF buffer
External Ref=0.6V
BANDGAP
0.15V
0.6V
REF GEN
MUX
vi_inp
vi_inn
Clock Tree

1ns 4ns
Track/sampling Conversion

FEATURES:

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US Patent Pending
Subsequent CDAC non-linearity calibration for the 4 MSB capacitors:

C9 = C8 + C7 + C6 + C5 + C4 + C3 + C2 + C1 + 2*C0
C10 = C9 + C8 + C7 + C6 + C5 + C4 + C3 + C2 + C1 + 2*C0
C11 = C9 + C8 + C7 + C6 + C5 + C4 + C3 + C2 + C1 + 2*C0
C12 = C9 + C8 + C7 + C6 + C5 + C4 + C3 + C2 + C1 + 2*C0
• Precise CDAC calibration improves ENOB by approximately 1 bit
  (±3σ variation of CDAC capacitance considered, equal to ±1.2% variation)
• Raw ADC data output through JESD204B output interface
• Event-driven digital core output through UART interface
• I2C interface for ASIC control registers programming
• Built-in calibration FSM / CPU for calibration purposes
RAW ADC DATA OUTPUT

- Programmable ADC sampling rate of 200/100/50 MS/s
- Constant JESD204B output data rate 6.4Gbit per second
- Shared JESD204B output data interface between 2/4/8 ADCs reduces the number of interface lines, allowing high system integration density

<table>
<thead>
<tr>
<th>Mode</th>
<th>JESD204B lanes</th>
<th>ADC per lane</th>
<th>Lane data rate</th>
<th>ADC data rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>Full speed</td>
<td>16</td>
<td>2</td>
<td>6.4Gbps</td>
<td>200MS/s</td>
</tr>
<tr>
<td>Half speed</td>
<td>8</td>
<td>4</td>
<td>6.4Gbps</td>
<td>100MS/s</td>
</tr>
<tr>
<td>Quarter speed</td>
<td>4</td>
<td>8</td>
<td>6.4Gbps</td>
<td>50MS/s</td>
</tr>
</tbody>
</table>

US Patent Pending
EVENT-DRIVEN BACKEND

• This ADC output is monitored by a digital comparator with a programmable threshold.

• When the ADC input exceeds threshold, a time stamp is assigned and the peak value of the incoming ADC data is recorded.

• When the event is completed, the relevant information is assembled into a packet by the Event Builder block. When the shared FIFO is ready, events stored in the channel FIFO are read out.

*Event-driven digital backend was built in collaboration with LBNL. And we want to thank Dr. Carl Grace for his effort.*
FEATURES:

- External clock input
- Can operate from 3.2GHz or 0.2GHz reference clock
- Integrated ADC sampling clock duty cycle correction
- Synchronous clock/reset for 32 ADC channels
- Integrated CPU
- Integrated temperature sensor
# ADC POWER CONSUMPTION

<table>
<thead>
<tr>
<th>Block</th>
<th>Analog supply current, mA @ 0.9V</th>
<th>Digital supply current, mA @ 0.9V</th>
<th>I/O supply current, mA @ 1.2V</th>
<th>Ground, mA @ 0V</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC CHANNEL</td>
<td>1.65</td>
<td>7.82</td>
<td>14.88</td>
<td>25.03</td>
</tr>
<tr>
<td>ADC CORE 12b@200Msps</td>
<td>1.46</td>
<td>1.62</td>
<td>N/A</td>
<td>3.73</td>
</tr>
<tr>
<td>JESD204B PHY</td>
<td>N/A</td>
<td>4.58</td>
<td>14.88</td>
<td>19.48</td>
</tr>
</tbody>
</table>

Typical power consumption of ADC w/o DATA interface: **5mW / ch**

Typical power consumption of ADC with DATA interface: **15.7mW / ch**

*(One JESD204B output data lane used per 2 ADCs operates at 200Msps)*
Typical performance: **SFDR > 74dB, ENOB > 10.4** for Fin<100MHz
MILESTONES AND DELIVERABLES

ACTUAL STATUS:

- ASIC is designed and being fabricated. ETA for the chips 09/20.
- Eval. PCB is being developed.
- GUI and ASIC test plan are being developed.

FUTURE:

- Chip packaging
- PCB fabrication/assembly
- ADC part testing
Thank You

Application Ideas for the ADC ASIC are appreciated!