Award Number: DE-SC0018566

Pacific MicroCHIP Corp.

AN ASIC WITH A LOW POWER MULTICHANNEL ADC FOR ENERGY AND TIMING MEASUREMENTS

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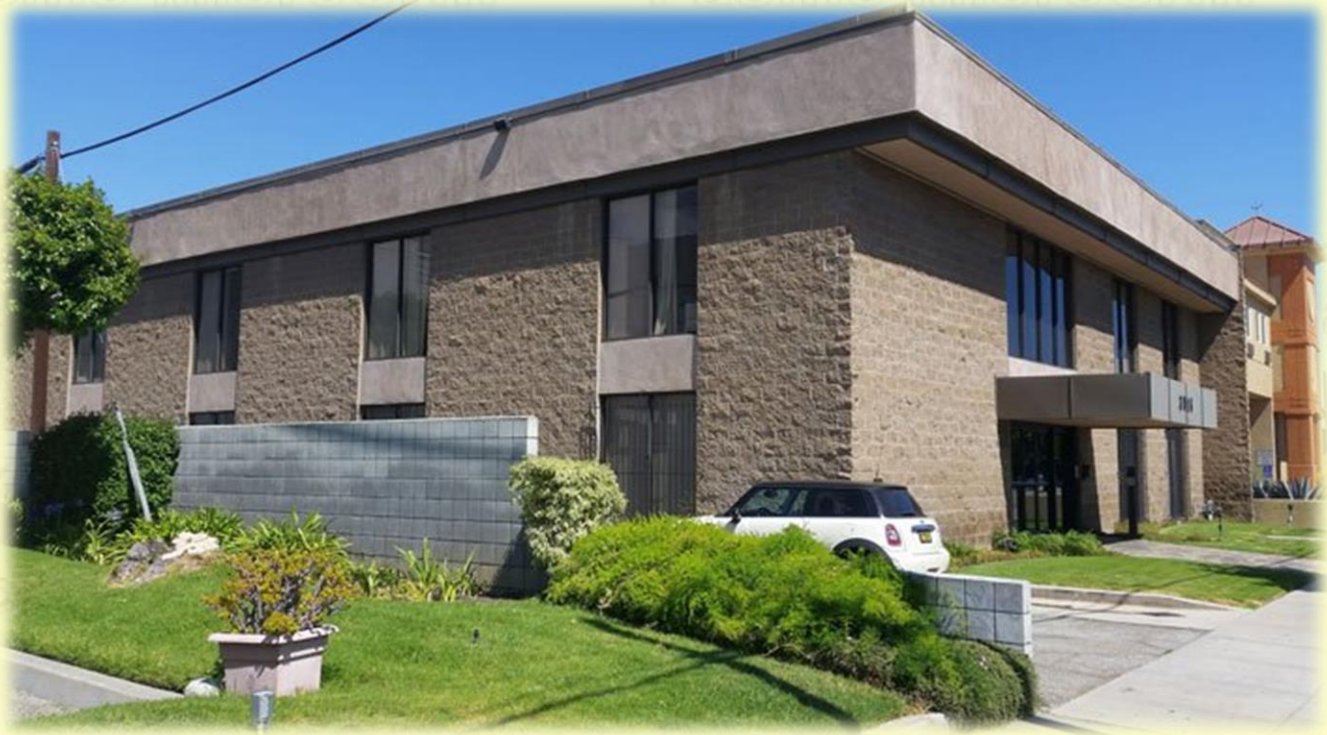
OUTLINE

Pacific MicroCHIP Corp.

- The Company, its Specialization/Expertise
- Phase II objective
- Multichannel ADC for energy and timing mesurements specifications
- Motivation
- ADC core architecture and implemented calibrations
- Digital architecture
- ADC data output interface
- Event-driven backend
- ASIC layout / floorplan
- ADC power consumption and performance
- Project schedules, milestones, deliverables and conclusions

COMPANY

- Pacific MicroCHIP Corp. is incorporated in 2006.
- It is headquartered in Culver City, California
- Main focus – providing IC/ASIC design services and turnkey solutions.



CORE EXPERTISE

- Analog (ADC/DAC, CTF, VGA, BG, LDO)
- Mixed Signal (PLL, CDR, SerDes, MDrv, TIA)
- RF (LNA, Mixer/Modulator, PA)
- Digital (RTL, Synthesis, P&R, Timing Closure, DFT, Verifications)
- Layout (SiGe/CMOS) down to 7nm

PHASE II OBJECTIVE

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- To design circuits and layout for the ADC ASIC.
- To fabricate the chip.
- To package the chips.
- To develop the test PCB and socket for the ASIC.
- To develop a GUI and a testbench.
- To test and characterize the ADC ASIC.
- To prepare a datasheet for marketing.
- To submit deliverables to the DoE.

ASIC SPECIFICATION

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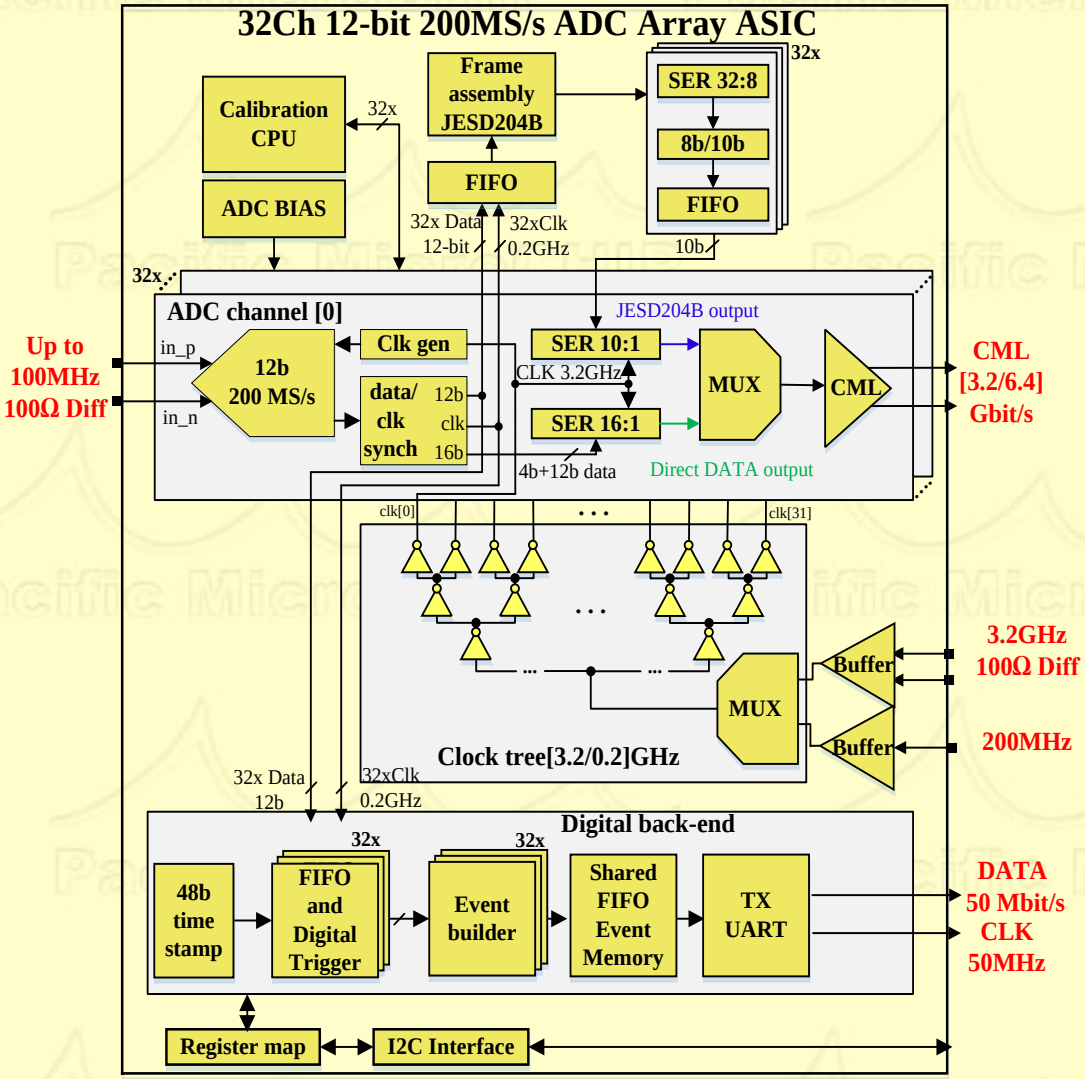
FEATURES:

- 32 independent channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input signal
- ENOB > 10-bit
- Programmable input signal bandwidth 0.1-0.3 GHz
- Integrated event-driven digital backend
- JESD204B output data interface
- Extended temperature range -40C..+125C
- Low power consumption 5 mW / channel (w/o interface)
- I2C interface for ASIC control

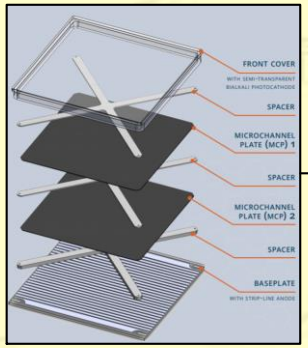


MOTIVATION (The Problem)

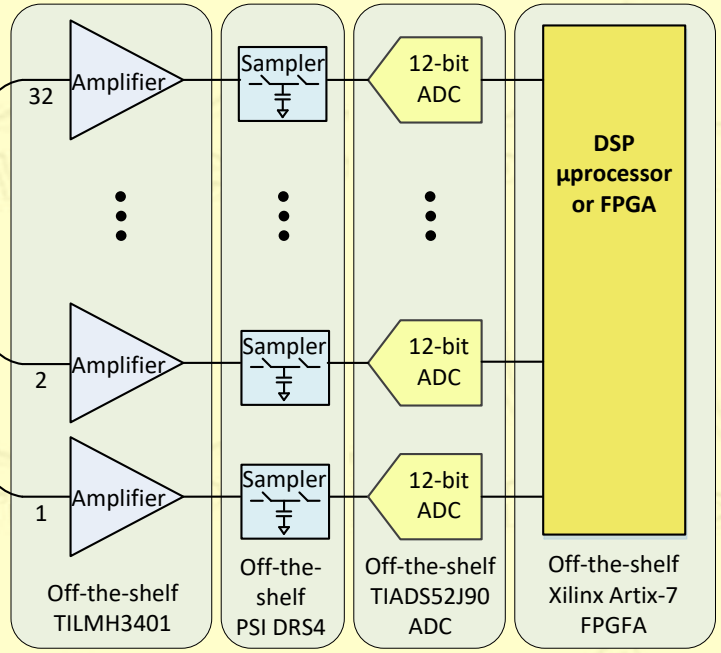
https://incomusa.com/lappd/

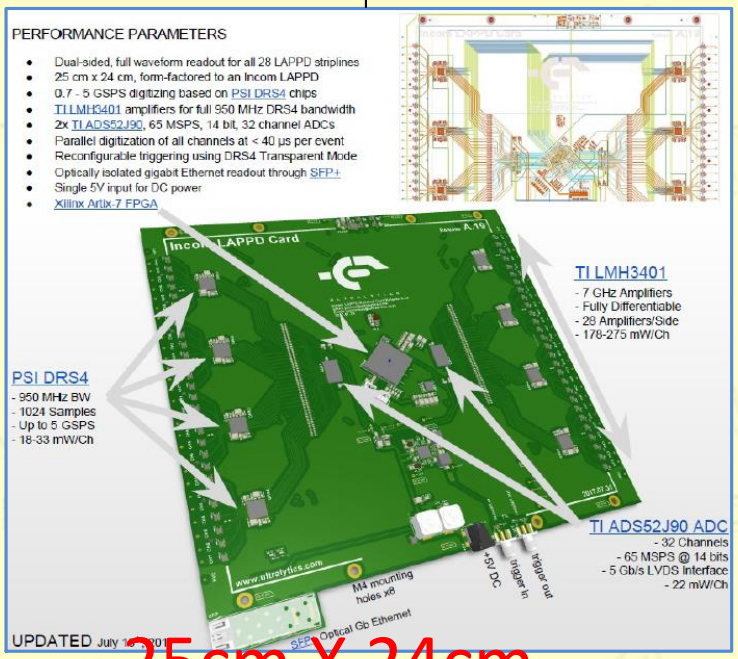
Available off-the-shelf solution

https://www.ultralytics.com/store/lappd



Large Area Picosecond Photodetector (LAPPD)





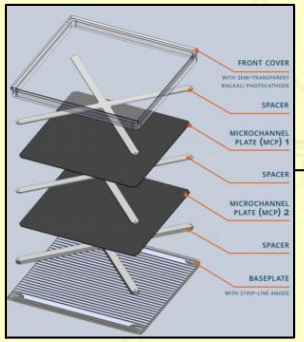
25cm X 24cm

- Required minimum communication data rate between ADCs and FPGA for 32 channels is **32** x **12bit** x **65MSps**=**24.96Gbit/s**
- Using multiple ASICs

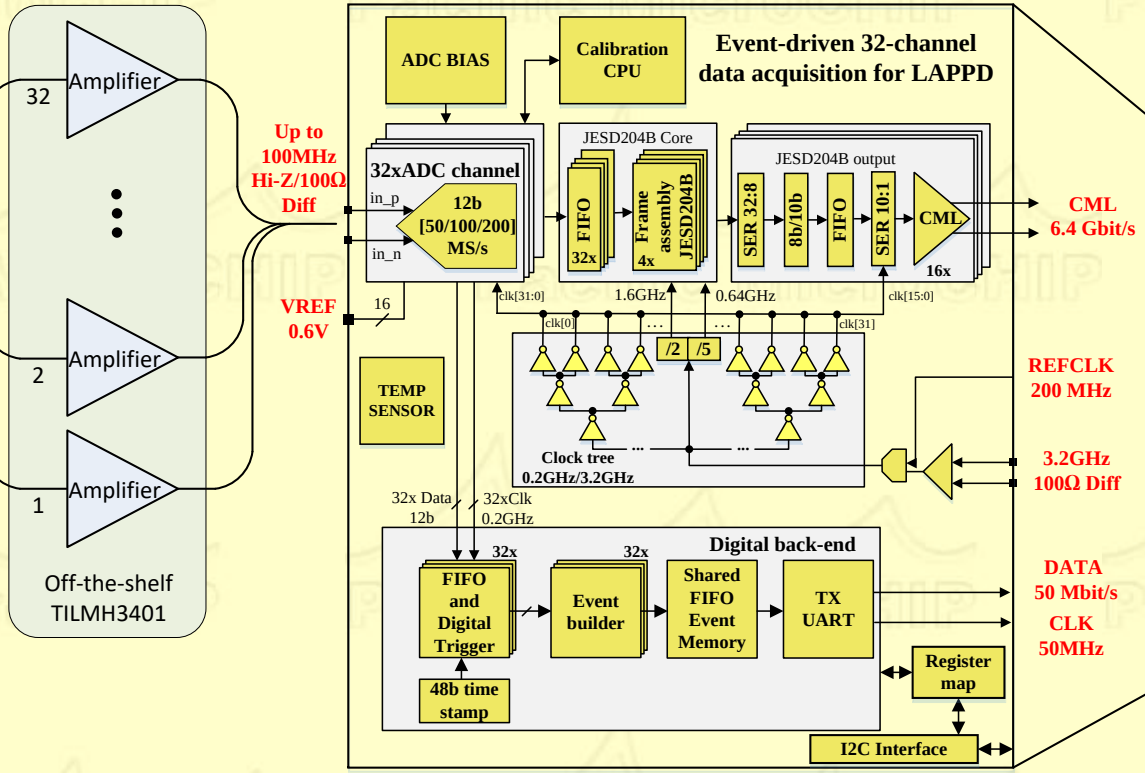
Large amount of wiring increases:

- detector congestion,
- volume,
- power consumption,
- cost

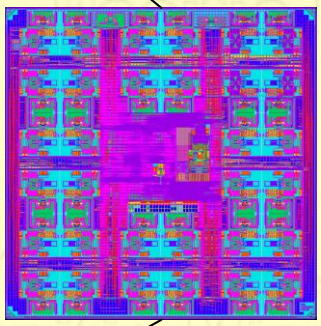
MOTIVATION (The Solution)



Large Area Picosecond Photodetector (LAPPD)



2.7mm x 2.7mm



- 32 independent ADC channels with integrated digital back-end for event detection and recording
- Only 50Mbit/s output data rate
- Raw data output trough JESD204B

- Low power consumption
- Simplified PCB design and wiring
- Using less components increase reliability
- Dual output data interface

ADC CORE ARCHITECTURE

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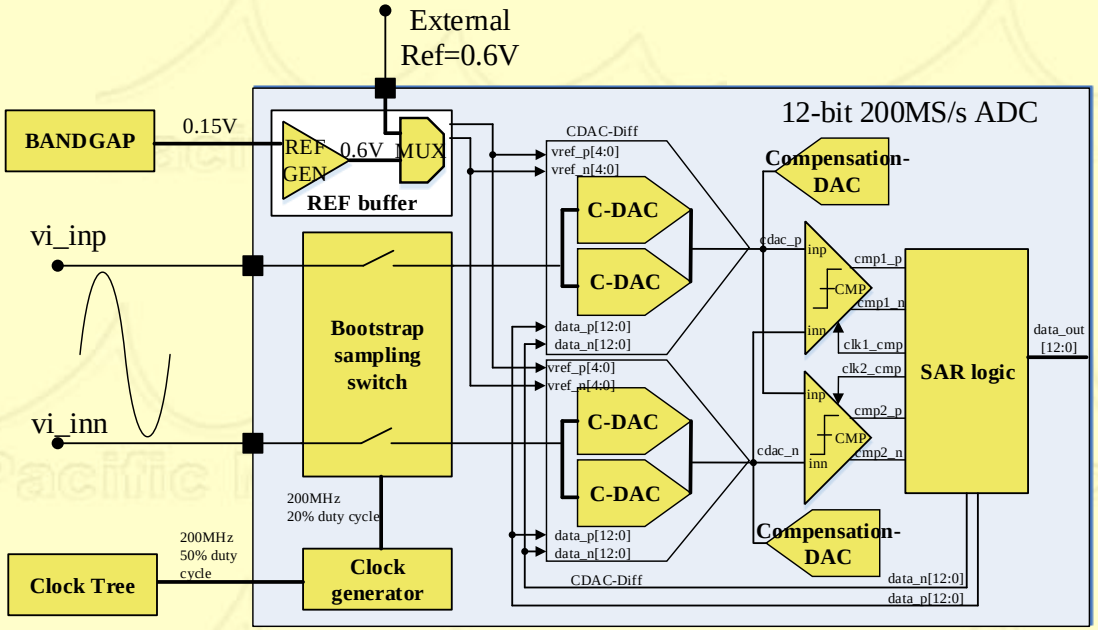
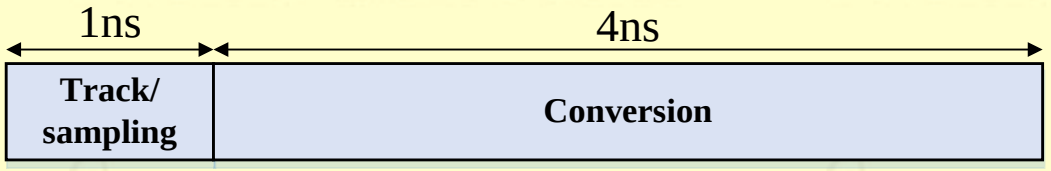
FEATURES:

- 12b SAR ADC architecture
- Segmented 3t-9b CDAC
- Optional external/internal ADC reference voltage source
- Fractional reference voltage
- Dual comparator
- Asynchronous logic
- Built-in FSM for comparator offset compensation
- Built-in FSM for CDAC non-linearity calibration

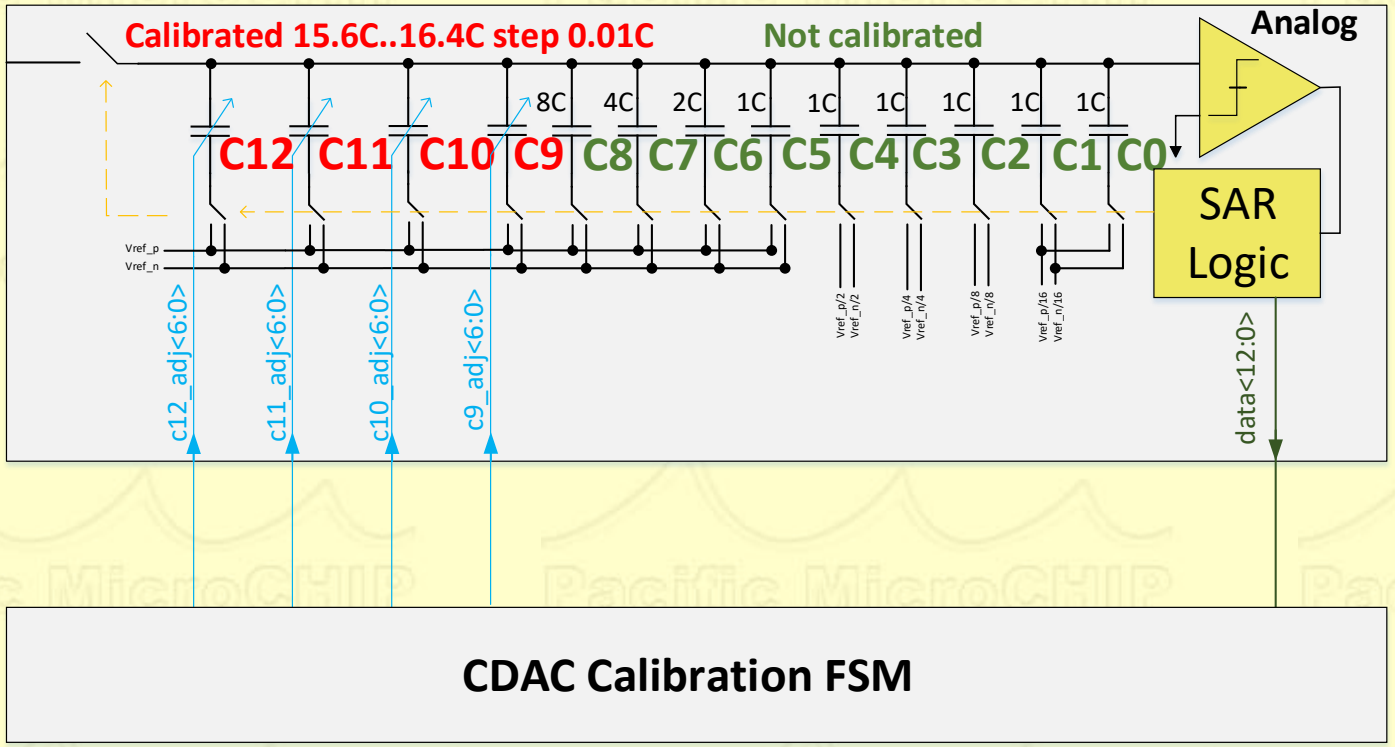
ADC CORE BLOCK DIAGRAM:



ADC TIMING DIAGRAM:



CDAC CALIBRATION DIAGRAM



Subsequent CDAC non-linearity calibration for the 4 MSB capacitors:

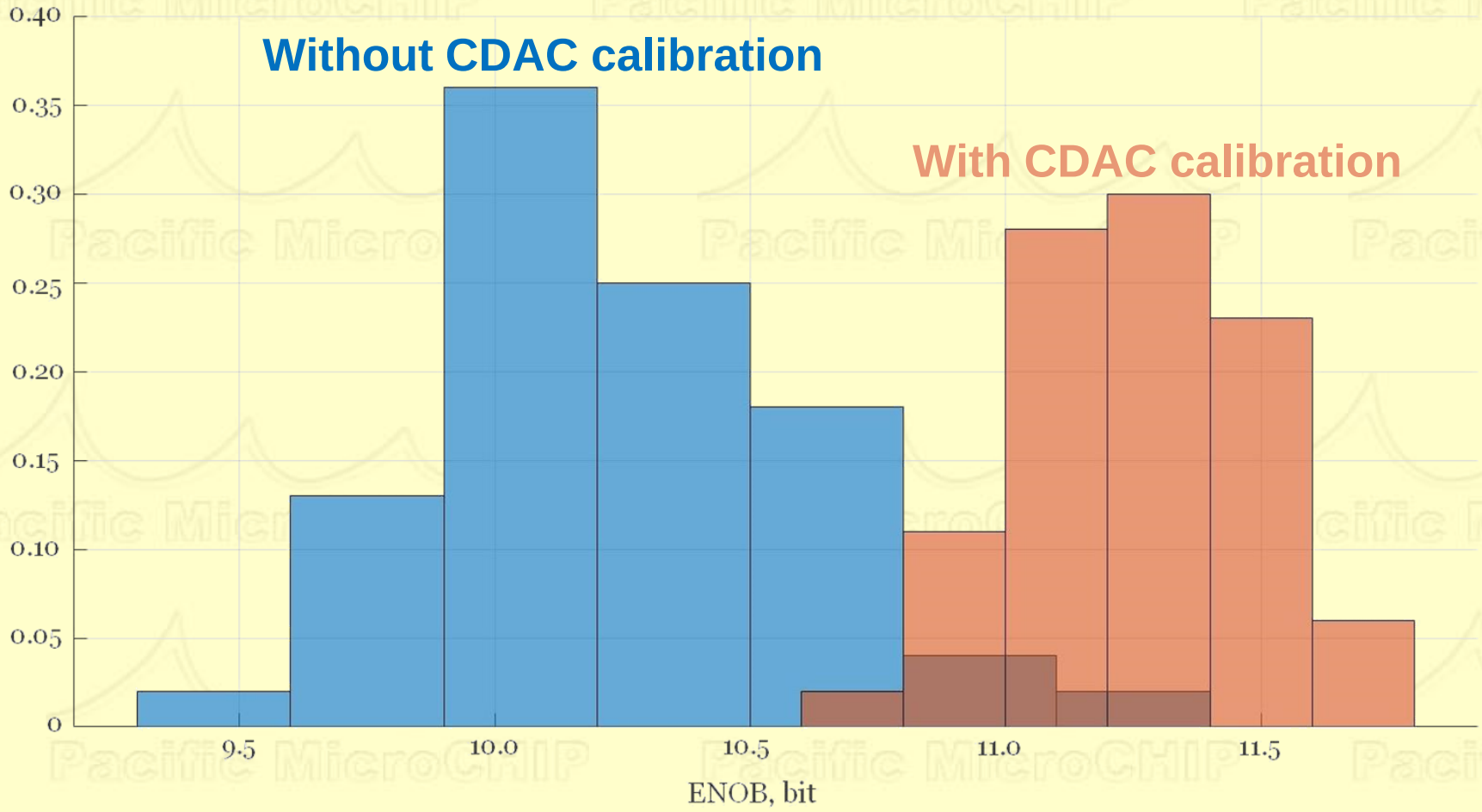
C9=C8+C7+C6+C5+C4+C3+C2+C1+2*C0

C10=C9+C8+C7+C6+C5+C4+C3+C2+C1+2*C0

C11=C9+C8+C7+C6+C5+C4+C3+C2+C1+2*C0

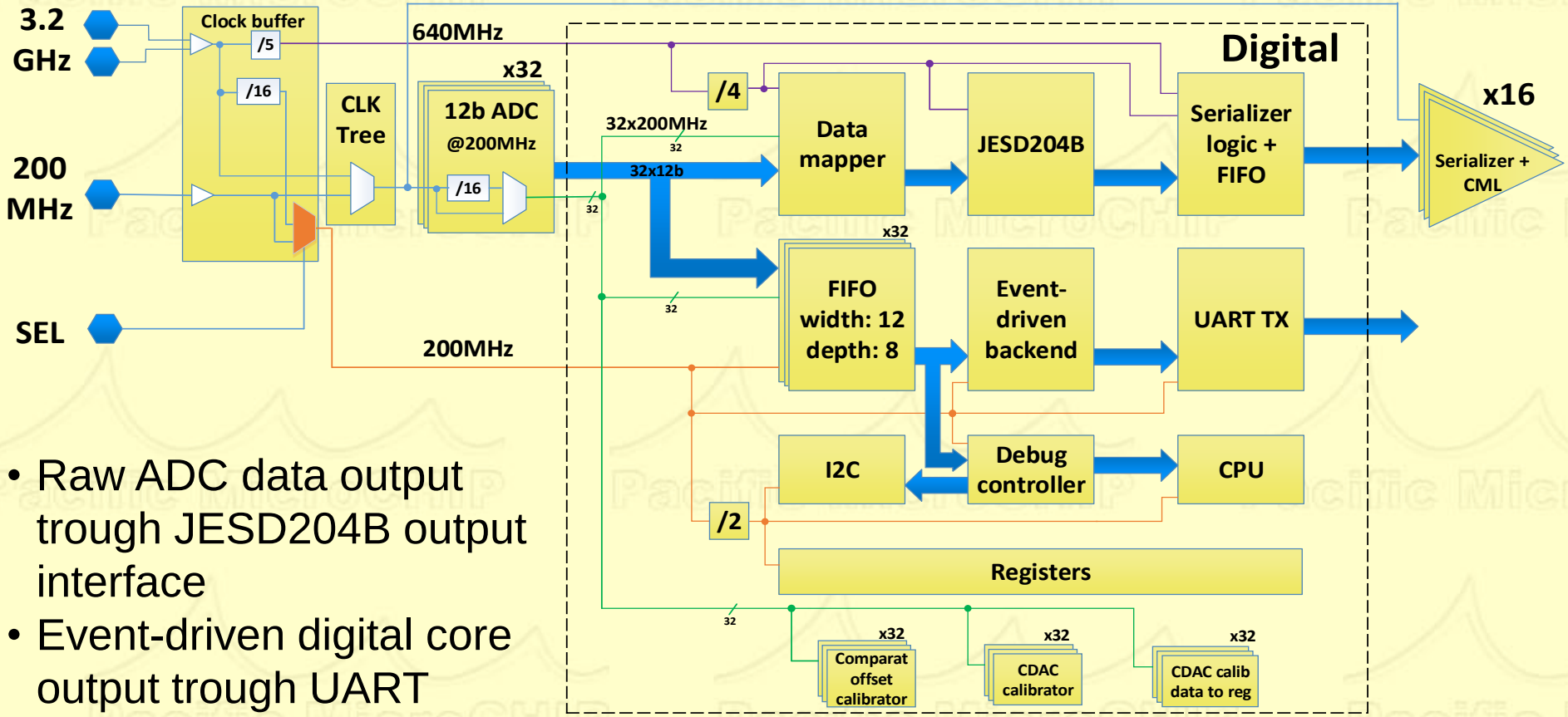
C12=C9+C8+C7+C6+C5+C4+C3+C2+C1+2*C0

CDAC CALIBRATION RESULTS



- Precise CDAC calibration improves ENOB by approximately 1 bit (±3σ variation of CDAC capacitance considered, equal to ±1.2% variation)

DIGITAL ARCHITECTURE



- Raw ADC data output trough JESD204B output interface
- Event-driven digital core output trough UART interface
- I2C interface for ASIC control registers programming
- Built-in calibration FSM / CPU for calibration purposes

RAW ADC DATA OUTPUT

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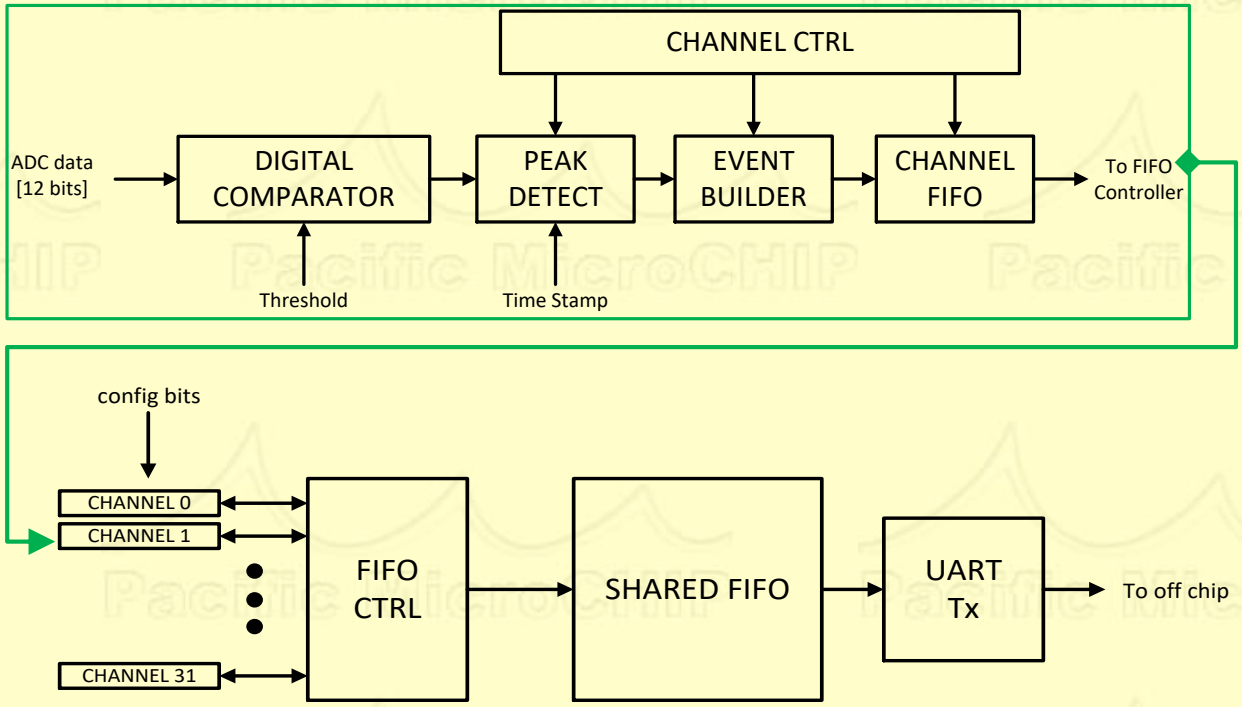
Mode	JESD 204B lanes	ADC per lane	Lane data rate	ADC data rate
Full speed	16	2	6.4Gbps	200MS/s
Half speed	8	4	6.4Gbps	100MS/s
Quarter speed	4	8	6.4Gbps	50MS/s

- Programmable ADC sampling rate of 200/100/50 MS/s
- Constant JESD204B output data rate 6.4Gbit per second
- Shared JESD204B output data interface between 2/4/8 ADCs reduces the number of interface lines, allowing high system integration density

EVENT–DRIVEN BACKEND

- This ADC output is monitored by a digital comparator with a programmable threshold
- When the ADC input exceeds threshold, a time stamp is assigned and the peak value of the incoming ADC data is recorded.



Event-driven digital backend was built in collaboration with LBNL. And we want to thank Dr. Carl Grace for his effort.

- When the event is completed, the relevant information is assembled into a packet by the Event Builder block. When the shared FIFO is ready, events stored in the channel FIFO are read out.

MULTICHANNEL ADC ASIC LAYOUT

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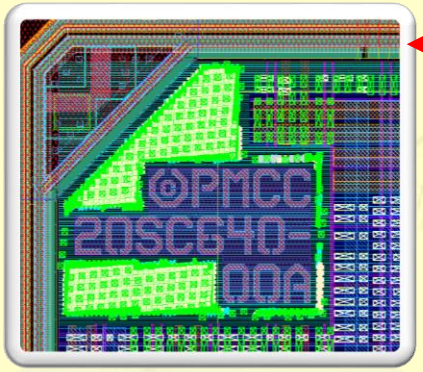
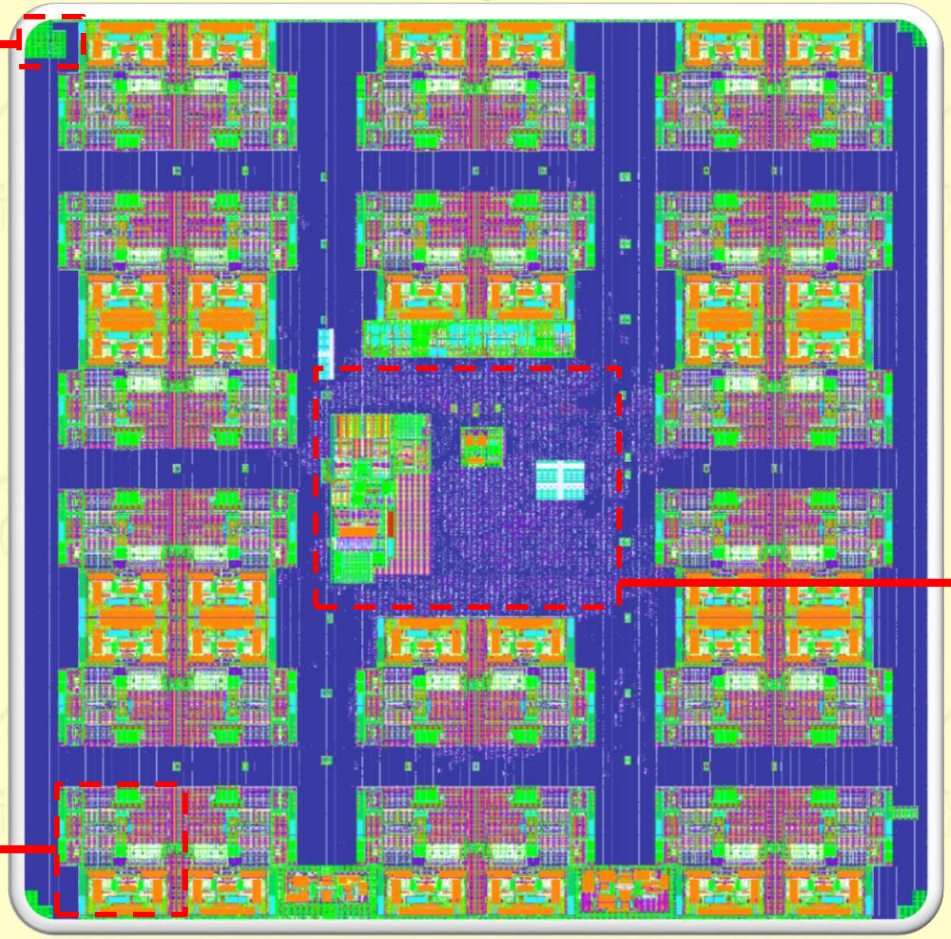
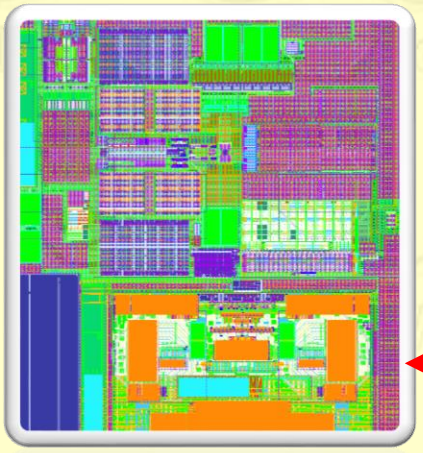
Logo



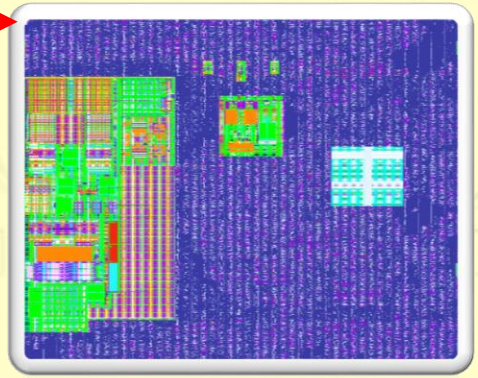
ASIC top level



ADC channel



Bias & digital core



ASIC FLOORPLAN

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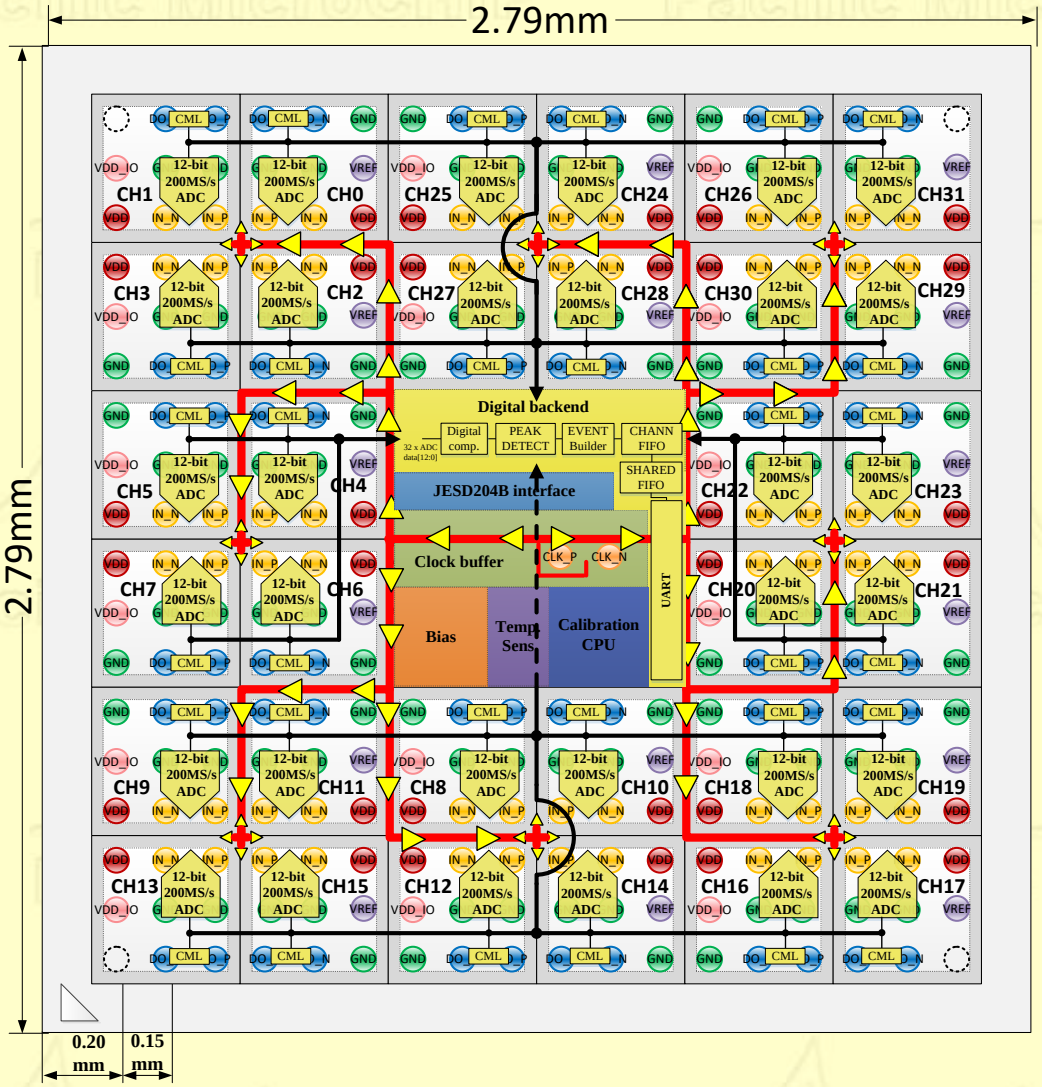
FEATURES:

- External clock input
- Can operate from 3.2GHz or 0.2GHz reference clock
- Integrated ADC sampling clock duty cycle correction
- Synchronous clock/reset for 32 ADC channels
- Integrated CPU
- Integrated temperature sensor



ADC POWER CONSUMPTION

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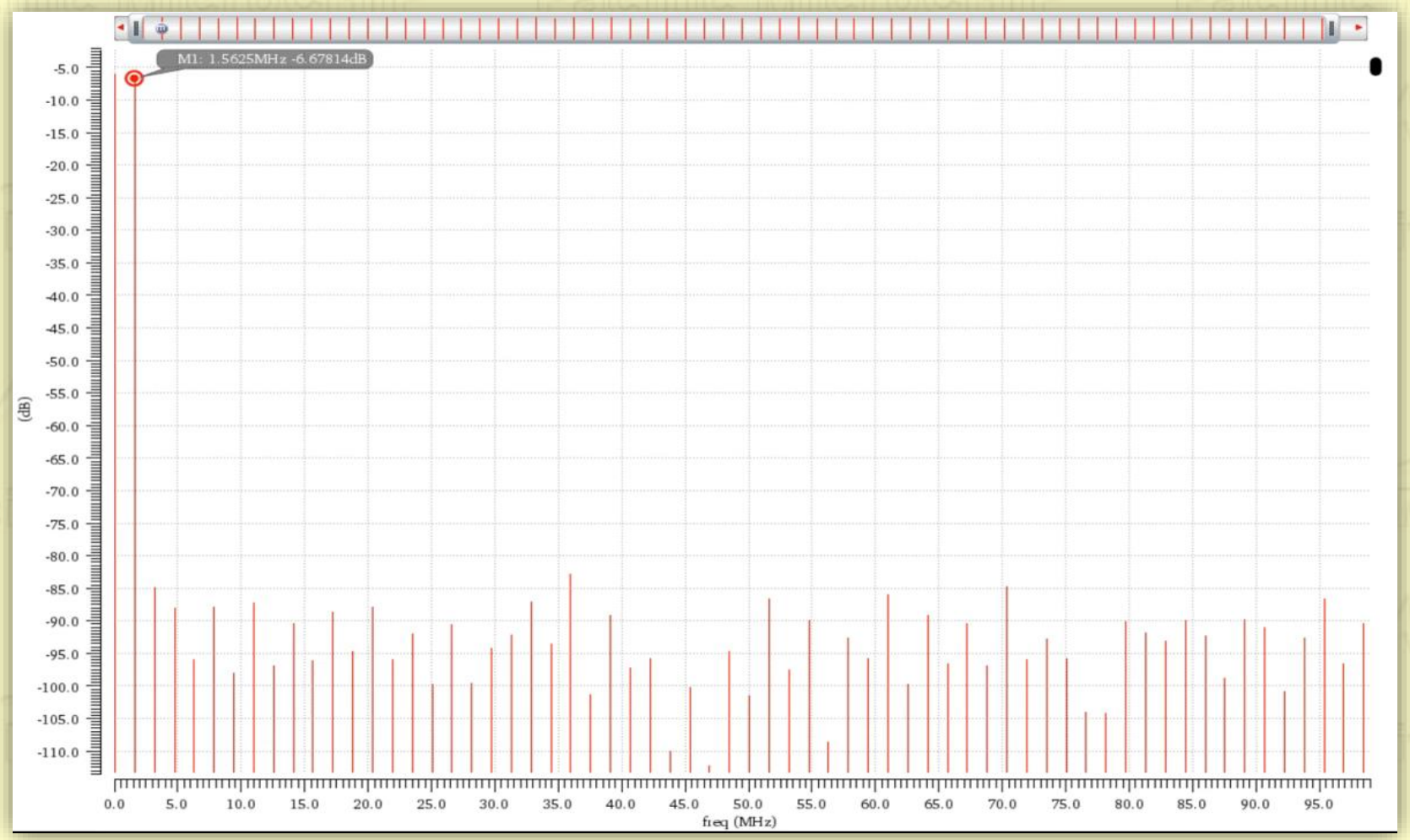
Block	Analog supply current, mA @ 0.9V	Digital supply current, mA @ 0.9V	I/O supply current, mA @ 1.2V	Ground, mA @ 0V
ADC CHANNEL	1.65	7.82	14.88	25.03
ADC CORE 12b@200Msps	1.46	1.62	N/A	3.73
JESD204B PHY	N/A	4.58	14.88	19.48

Typical power consumption of ADC w/o DATA interface: **5mW / ch**

Typical power consumption of ADC with DATA interface: **15.7mW / ch**

(*One JESD204B output data lane used per 2 ADCs operates at 200Msps*)

ADC OUTPUT SPECTRUM VS INPUT FREQUENCY



Typical performance: **SFDR > 74dB**, **ENOB > 10.4** for Fin<100MHz

MILESTONES AND DELIVERABLES

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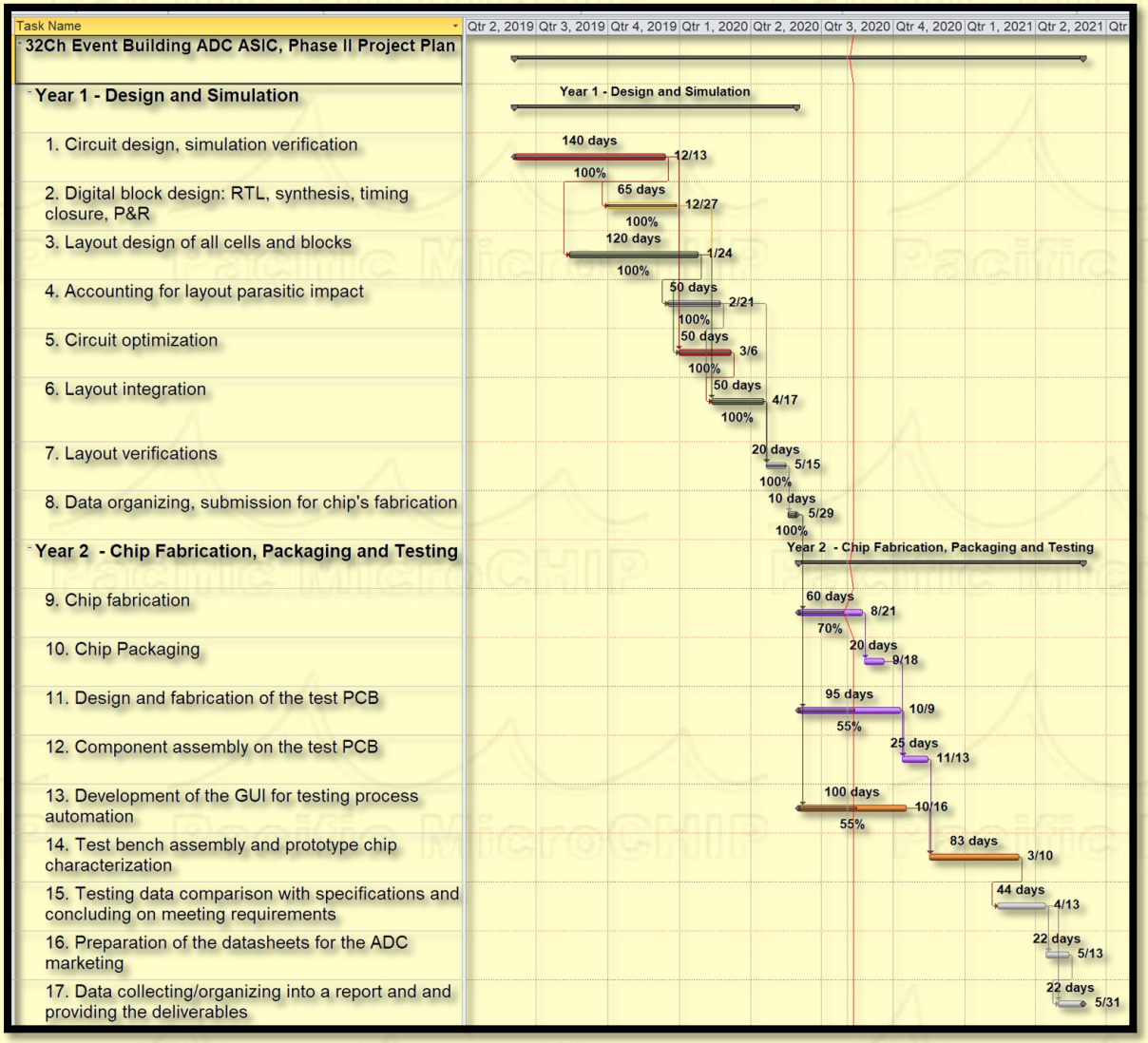
ACTUAL STATUS:

- ASIC is designed and being fabricated. ETA for the chips 09/20.
- Eval. PCB is being developed.
- GUI and ASIC test plan are being developed.

FUTURE:

- Chip packaging
- PCB fabrication/assembly
- ADC part testing



Thank You

Application Ideas for the ADC ASIC are appreciated!