

Pacific MicroCHIP

Pacific MicroCHII

12-bit 32 Channel 500MSps Low Latency ADC

Award Number: DE-SC0017213 Ph II project, Year 2 (under NCE)

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Presentation Outline



- The Company, Its Specialization/Expertise
- A 12-bit 32 Ch 500MS/s ADC (being developed)
- Relevance to the NP Program
- Project Goals
- Chip Specifications and Architecture
- Comparison to ADCs Available on the Market
- Physical Implementation
- Chip Carrier and Packaging
- Testing Setup and Results
- Project Schedules and Milestones
- Future Plans

The Company



- Pacific MicroCHIP Corp. was incorporated in 2006.
- It is headquartered in Culver City, California.
- Main focus of the Company providing IC/ASIC design services and turnkey solutions.



Office in Culver City, CA

Our Offerings



IC/ASIC Design Services:

- Circuit Design (analog, RF/mixed, digital)
- Simulation
- Physical Design
- Chip Assembly

Turnkey Solutions:

- IC Design
- Chip Fabrication Logistics
- Package Development (involving a 3rd party)
- Chip Packaging (involving a 3rd party)
- PCB Development for Testing/Eval. (involving a 3rd party)
- Testing/Characterization (an in-house lab)
- Delivery of Chips, Parts and Board Level Solutions

Relevance to the NP Program Partile MicroBill

<u>NP detectors require thousands of signal processing channels =></u> need for digitizers to:

- Shrink in size our ASIC combines 32 independent ADCs per chip.
- Reduce power consumption expected 25mW / ADC (w/o JESD buffers).
- Reduce wire congestion our ADCs have a serial interface that can be shared between 2 or 4 ADCs

Upgrades in these systems demand for:

- Digitizing accuracy our ADC features 12-bit resolution.
- Adequate sampling speed our ADC features up to 0.5GS/s.
- Low conversion latency we offer 8ns.

Targeted specific applications:

- Low latency particle beam control systems.
- Imaging and spectroscopy systems for gamma-ray detectors.
- Multichannel detectors based on tube and silicon photo multipliers.

Project Goals for Phase II Partie Monthering

Within this project we will:

- Design circuits and layout for the ADC ASIC.
- Fabricate the chip.
- Develop a special chip carrier.
- Package the chips.
- Develop a test PCB and a DUT socket.
- Develop a GUI and a test bench.
- Test and characterize the ADC ASIC.
- Prepare a datasheet for marketing.
- Submit deliverables to the DoE.

12-bit 32 Channel 500MSps Low Latency ADC



Specifications (expected performance):

- 32 independently operated ADC channels
- 500 MS/s sampling rate
- 0.6Vpp differential input swing
- 10-bit ENOB
- 250MHz input signal bandwidth
- -40C..+125C temperature range
- 25mW/channel power consumption (with interface)

- JESD204B output data interface
- 8ns latency (direct ADC data output mode)
- 32x8Gb/s output data rate
- I2C interface for ASIC control
- 7.7mm² ASIC layout footprint
- A solder bumped die in a BGA package
- 28nm CMOS technology

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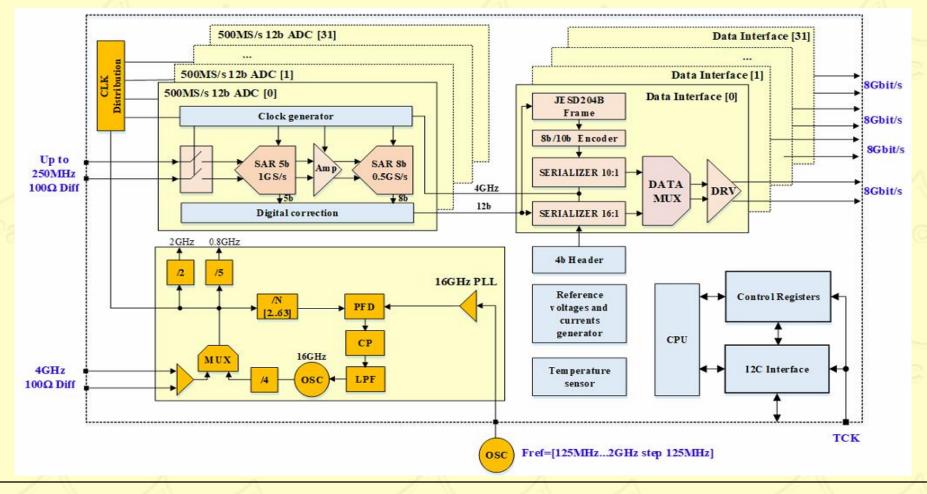
US Patent Pending

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12-bit 32 Channel 500MSps Low Latency ADC



ASIC Block Diagram



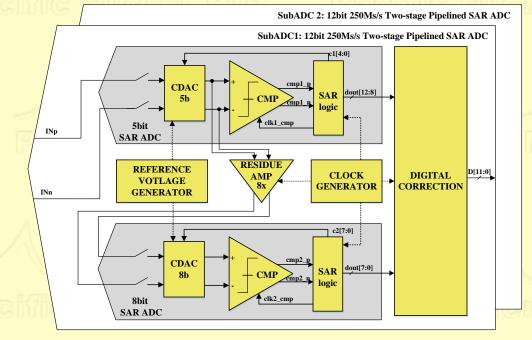
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12-bit 500MSps ADC Core

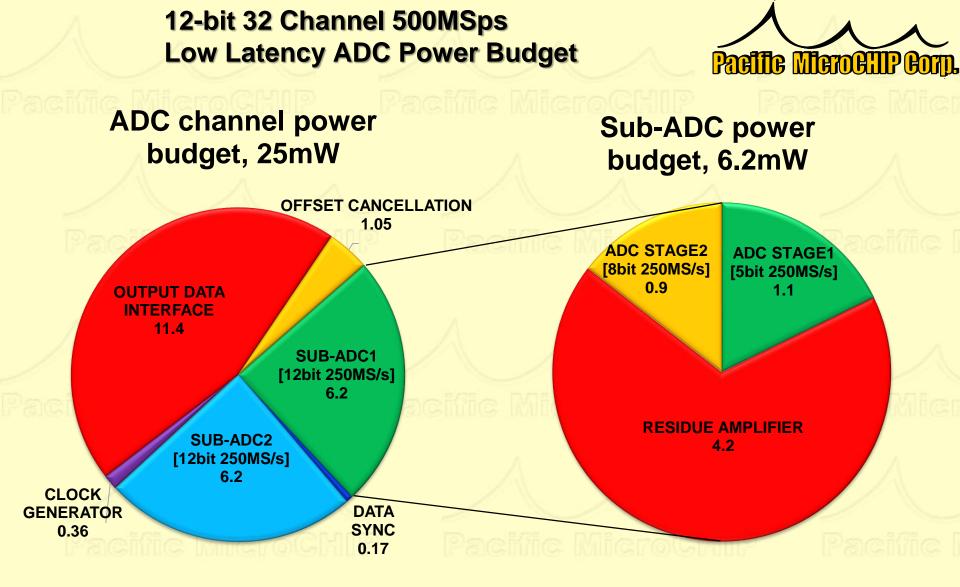


- Two-times time-interleaved ADC core
- Sampling clock skew adjustment
- Two-stage pipelined SAR architecture
- Programmable residue amplifier gain
- Programmable ADC FS range
- Bootstrapped input switches
- 1-bit redundancy between ADC stages



| | | • | • | |
|-------------------------|-------------|------------------|------------------|----------|
| | STAGE1 (5b) | TRACK CONVERSION | RESIDUE TRANSFER | |
| Sub-ADC 1 🚽 RESIDUE AMP | | OFF | AMPLIFICATION | |
| | STAGE2 (8b) | CONVERSION | TRACKING | |
| Ping-Pong | | < 2ns | 0.5ns 1.5ns | → LYZCII |
| | STAGE1 (5b) | RESIDUE TRANSFER | TRACK CONVERSION | |
| Sub-ADC 2 RESIDUE AMP | | AMPLIFICATION | OFF | |
| | STAGE2 (8b) | TRACKING | CONVERSION | A |

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Comparison to ADCs Available on the Market

| # | Vendor | # of Channels | Sample Rate, MS/s | Power Cons. per Channel | Architecture & Latency | |
|----|------------------------------------|------------------|-------------------------|----------------------------|---------------------------|--|
| 1. | TI 12-bit ADS52J90 | 32 | 40 | 41mW | Pipeline 2.5us | |
| 2. | TI 12-bit ADS5403IZAYR | 1 | 500 | 1W | Pipeline 240ns | |
| 3. | TI 12-bit ADS54T04IZAYR | 2 | 500 | 1.15W | Pipeline 240ns | |
| 4. | ADI 12-bit AD9234BCPZRL7 | 2 | 500 | 1.5W | Pipeline 240ns | |
| 5. | Pacific Microchip Corp. 12-bit* | 32 | 500 | 25mW | SAR/Pipeline 8ns | |

* Expected performance

ASIC's Physical Implementation



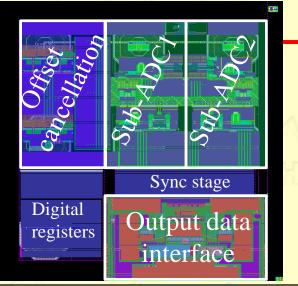
Chip periphery:

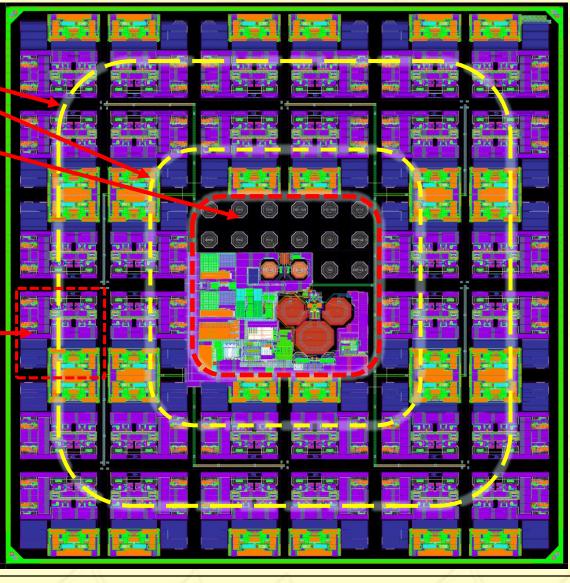
32 independent ADC channels located in 2 circles

Central part:

- PLL with a clock tree
- Temperature sensor
- CPU for calibration
- I2C interface for control

Single ADC channel





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Fabricated Chips





• PLL Temperature Sensor CPU for Calibration I2C Control Interface

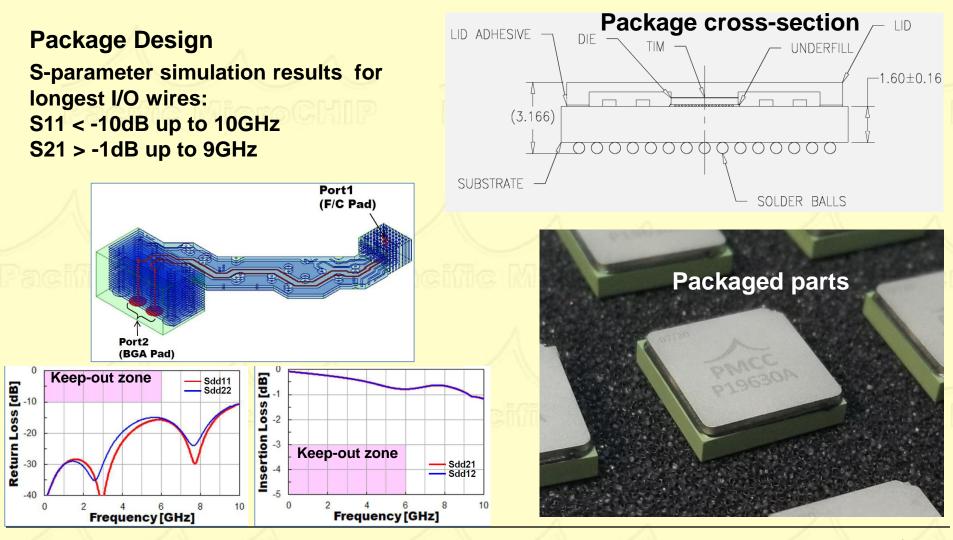
ADC Channel (1 out of 32) Output Data Buffer Digital Registers Sub-ADC1 Sub-ADC2 **Offset Cancelation Common Block With:** - 60

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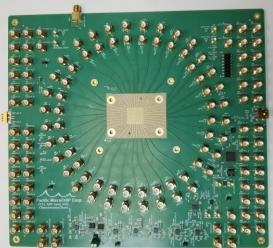
Chip Packaging



BGA 15.2 x 15.2 mm, 18 x 18 balls, 0.8mm ball pitch



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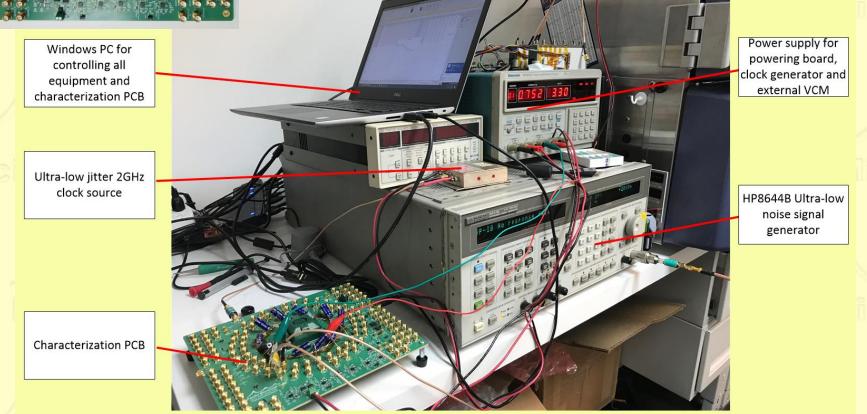


Testing Setup



← Test Board

- Exposed area in the center for DUT socket
- 32 differential inputs in a circle for delay equalization
- 32 differential outputs at the PCB's edge (less critical to PCB losses)



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Preliminary Testing Results



Power Consumption

| mA] P [mW] |
|------------|
| |
| 45 400.5 |
| 9 16.2 |
| 38 79.2 |
| 64 676.8 |
| 50 54.0 |
| 1226.7 |
| 38.3 |
| |

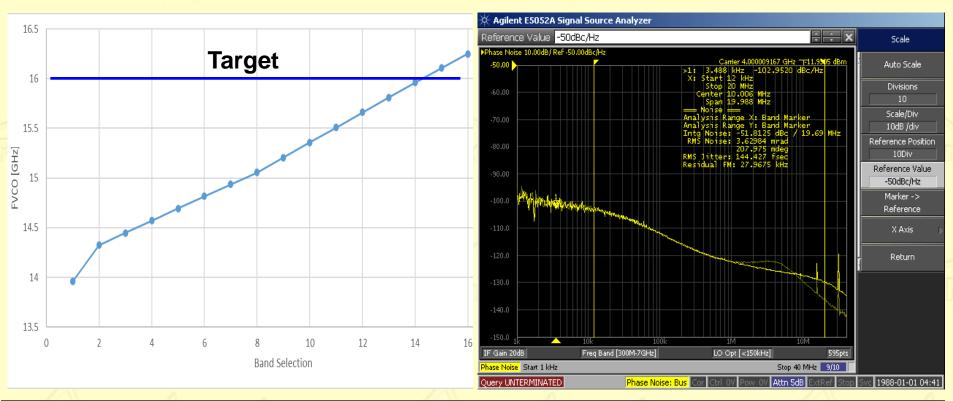
Notes: Power of the JESD204B interface is included. An input signal is applied only to a single ADC out of 32. The VDDD consumption is expected to increase when a signal is applied.

Preliminary Testing Results

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PLL Performance

Targeted frequency achieved on the 14th band. It will be tuned up in the 2nd prototype. Phase noise tested at 16GHz/4. 144fs RMS jitter (12K-20MHz range). Jitter does not depend significantly on PLL BW.

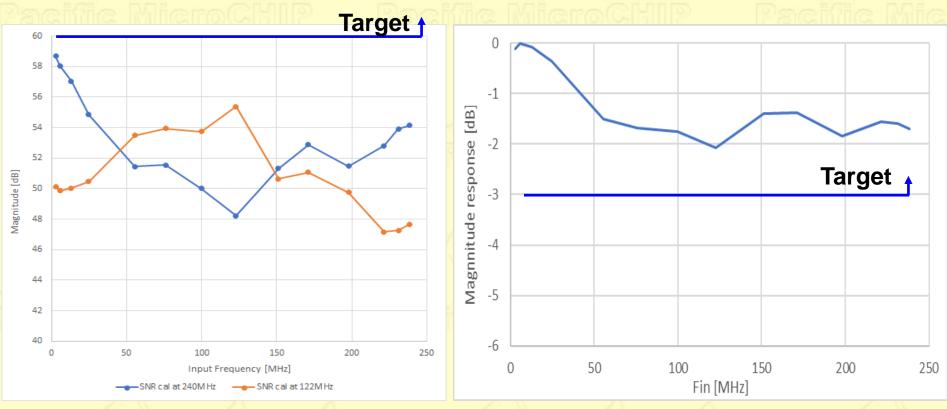


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Preliminary Testing Results



ADC Performance



ENOB vs. Input signal frequency. When ADC is calibrated at 240MHz: 9.5 ENOB @ 5MHz 7.2 ENOB @ 250MHz (Nyquist) When ADC is calibrated at 122MHz: 8.5 ENOB @ 122MHz

Project Schedule



| Task Name | 2, 2018 May Jun | | | Qtr 1, 2019 | | | | Qtr 1, 2020 | | Qtr 3, 2020 | Qtr 4, 2020 Oct Nov Dec . |
|--|--------------------|------------------|----------|---------------------|--------------|------------|----------------------|------------------|---------------|----------------|------------------------------|
| Low Latency 32 Ch ADC ASIC's Development - Phase II Project Plan | - | | | | npi inay ban | | | | The may bar | | |
| ⁻ Design and Simulation | | | Des | sign and Simulati | on | | | | | | |
| 1. Circuit design, simulation verification | | 145 days 100% | | 12/7 | | | | | | | |
| 2. Digital block design: RTL, synthesis, timing closure, P&R | | | 65 days | 12/21 | | | | | | | |
| 3. Layout design of all cells and blocks | | | 120 days | 1/18 | | | | | | | |
| 4. Accounting for layout parasitic impact | | | | 50 days 2/152/15 | | | | | | | |
| 5. Circuit optimization | | | | 100 days | 5/10 | | | | | | |
| 6. Layout integration | | | | | | days 0% | 9/27 | | | | |
| 7. Layout verifications | | | | | | 10 | days 10/11 00% | | | | |
| 8. Data organizing, submission for chip's fabrication | | | | | | | 0 days | | | | |
| [•] Chip Fabrication, Packaging and Testing | | | | | | | - | Chip Fabricati | on, Packaging | and Testing | , |
| 9. Chip fabrication | | | | | | | 60 day ∢ | s 1/17 | | | |
| 10. Chip carrier development, fabrication. | | | | | | | « — | 162 days 100% | | /9 | |
| 11. Chip Packaging | | | | | | | | 100 % | - * | 0 days 100% | |
| 12. Design, fabrication and assembly of the testing board | | | | | | | « — | 70 days 100% | | -7/7 | |
| 13. Packaged ASIC (DUT) assembly on the PCB | | | | | | | | 100 % | | 5 days | 5 |
| 14. Development of the GUI for testing process automation | | | | | | | * | 85 days 100% | | 7/14 | |
| 15. Prototype chip characterization | | | | | | | | | | 20 day | 9/22 |
| 16. Testing data comparison with specifications and concluding on meeting requirements | | | | | | | | | | 30 da | ys 10/6 |
| 17. Preparation of the specifications/description of the ASIC's IP block for marketing | | | | | | | | | | | 22 days 11/5 0% |
| 18. Data collecting/organizing and providing a technical report | | | | | | | | | | | 21 days 11/20 0% |

Future Plans



- Finish testing the chip's 1st prototype (End of Ph II).
- Transition to Phase IIA to redesign the chip, increase its performance, fix issues identified during testing.
- Fabricate the final chip.
- Test/evaluate it.
- Prepare the chip description and datasheets.
- Organize the ADC ASIC design as an IP block and advertise it.
- Provide the chip to the DoE community and commercial customers.



We would appreciate any application ideas and customer leads for the presented 32ch ADC !

THANK YOU !

