ALPHACORE

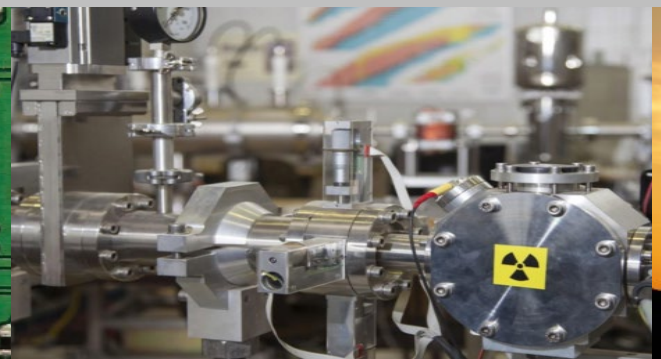
# Multi-Channel Readout ASIC for Nuclear Physics Experiments

**Presented by : Phaneendra Bikkina (Principal Engineer)**

**DOE-NP SBIR/STTR Exchange Meeting**
**August 14, 2019**



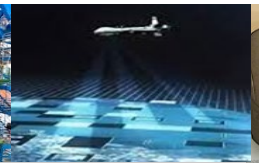





# Agenda



- Alphacore Overview
- Alphacore's DOE STTR Phase II Program Overview and Status (Year 1)
- Alphacore's Other Digitizers for Nuclear Physics Experiments
- Alphacore's Other Electronics Solutions for Nuclear Physics Experiments
- Other Relevant IP
- Summary

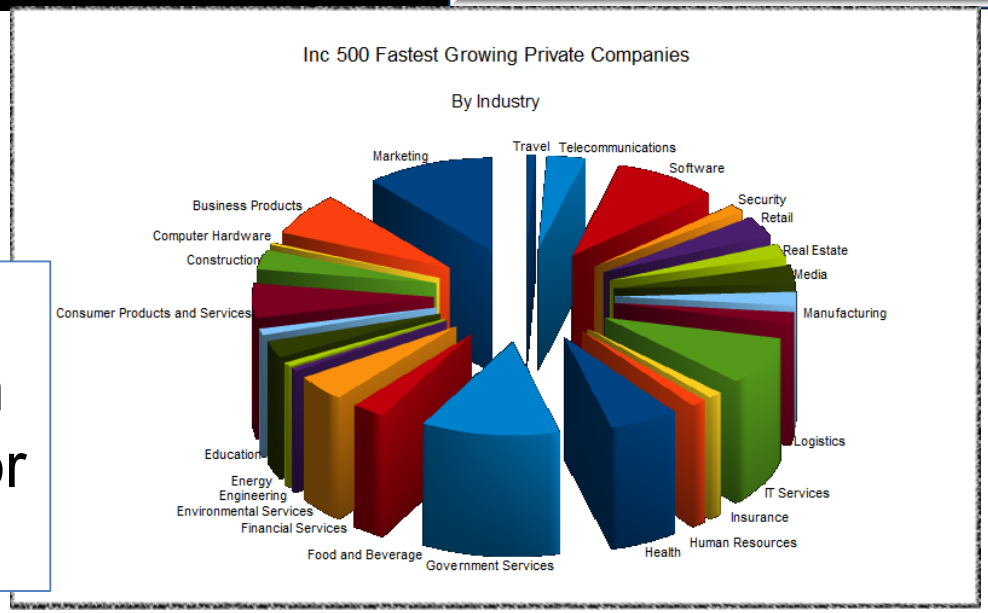

# About Alphacore

ALPHACORE

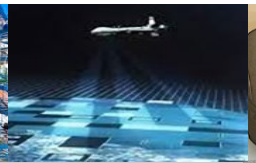
**Robust High Performance Microelectronics**

- Founded in 2012 and located in Arizona's "Silicon Desert"
- Providing technology that enable major advances in:
  - Homeland Security
  - Defense
  - Aerospace
  - Scientific Research
  - Medical Imaging
- Product areas span:
  - High performance analog, mixed signal, and RF electronics (rad-hard & conventional)
  - High-speed visible light and infrared camera systems
  - Robust GaN-based power electronics for space and high-energy physics experiments
  - Innovative devices ensuring supply chain and IoT cybersecurity

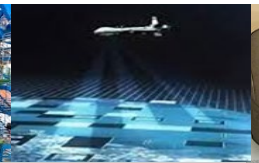
Top 5 electronics in Inc. 500 list for 2017






# Alphacore's Team



Alphacore's team is a combination of business and engineering professionals with long histories of delivering products and services to customers who demand state-of-the-art performance.

Our 70-person team has led successful careers at companies ranging from start-ups to multinationals including **Raytheon, Texas Instruments, Analog Devices, IDT, Bell Labs, Intel, United Technologies,** and **Honeywell**. Our Team includes 8 PhD-level full time employees and we sponsor 10 PhD students

# Multi-Channel Readout IC for Nuclear Physics Experiments

# Multi-Channel Readout IC for Nuclear Physics Experiments: DOE STTR Phase II Year 1 Overview

ALPHACORE

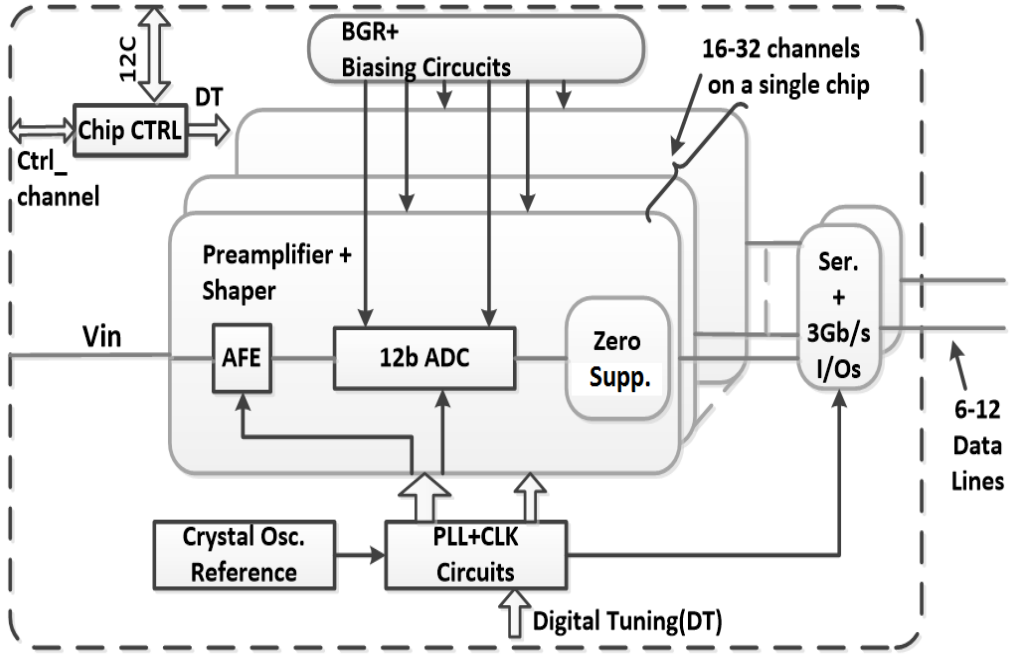
Robust High Performance Microelectronics

- Program duration : 24 months
- Key goal of this work is to develop versatile and low-cost detector readout IC solutions.

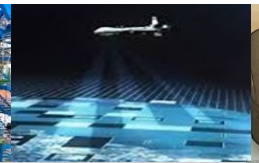
- Two step approach that will lead to two fabrication runs

- In step 1 (tapeout 1), our approach is to produce three different types of chips in low cost 180nm process:
  - multi-channel preamplifier/shaper IC (charge sensitive amplifiers )
  - multi-channel ADC IC
  - multi-channel combined IC that has preamplifiers, shaping amplifiers and ADCs with Serializers

- In step 2 (tapeout 2), our approach is to optimize the performance based on measurement results of tapeout 1 and add additional features to the ASICs:
  - zero suppression logic
  - increased resolution/performance of the ADCs
  - optimized programmable charge sensitive amplifiers

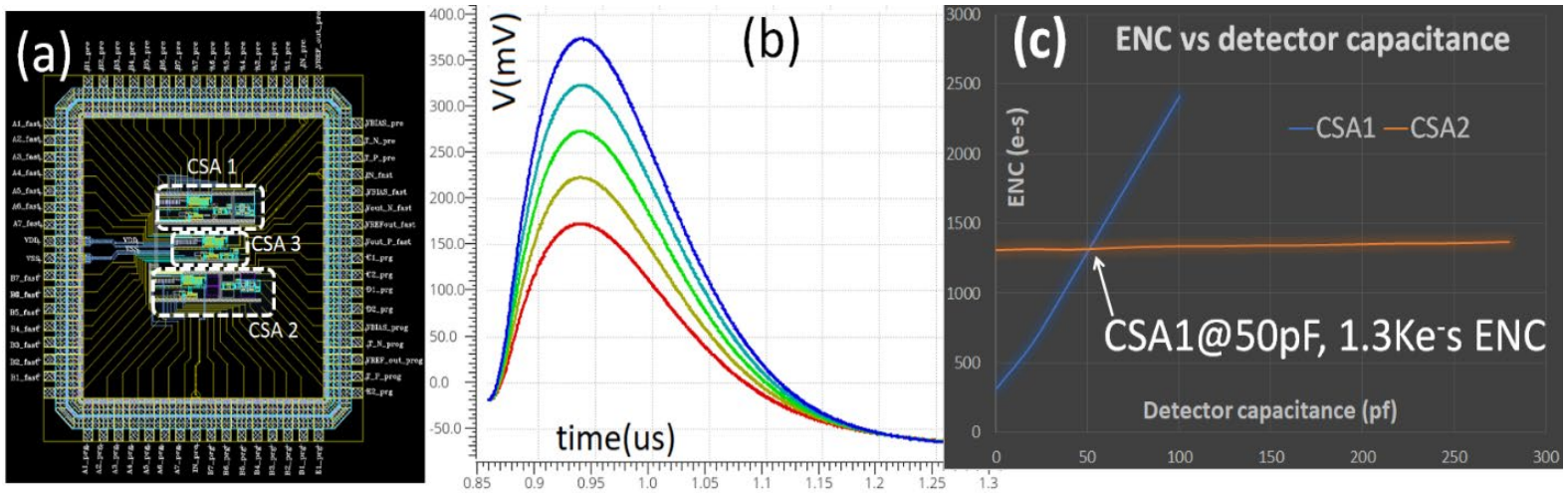



*Top level architecture of Alphacore's proposed multi-channel ROIC chip that has Preamplifiers and Shapers, 12b/100MSPS ADCs, zero suppression logic, serializers and 1.6Gb/s I/Os. Zero suppression will reduce the data throughput very effectively in experiments where input pulse rate is low.*

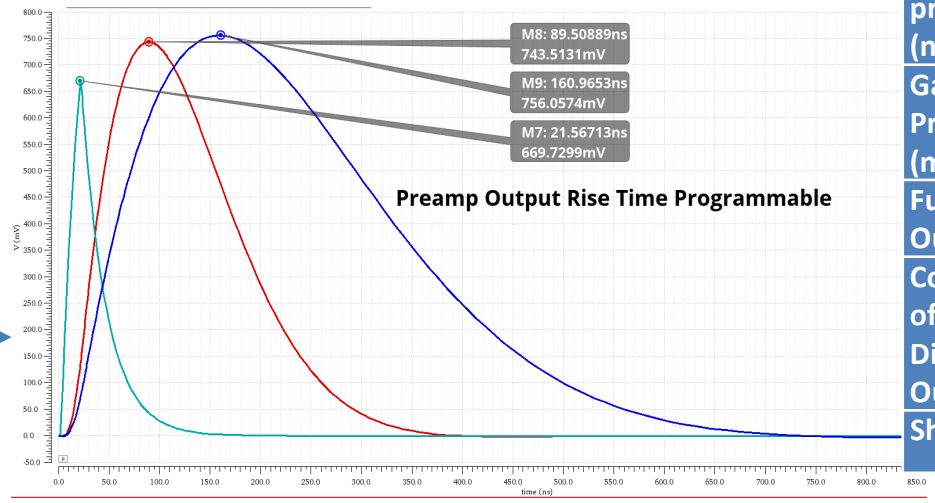




# Charge Sensitive Amplifiers



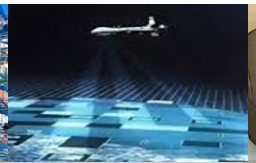



a) Test chip for 3 CSAs b) transient simulations of CSAs for varying input current pulses c) comparison of ENC of CSA1 and CSA2.



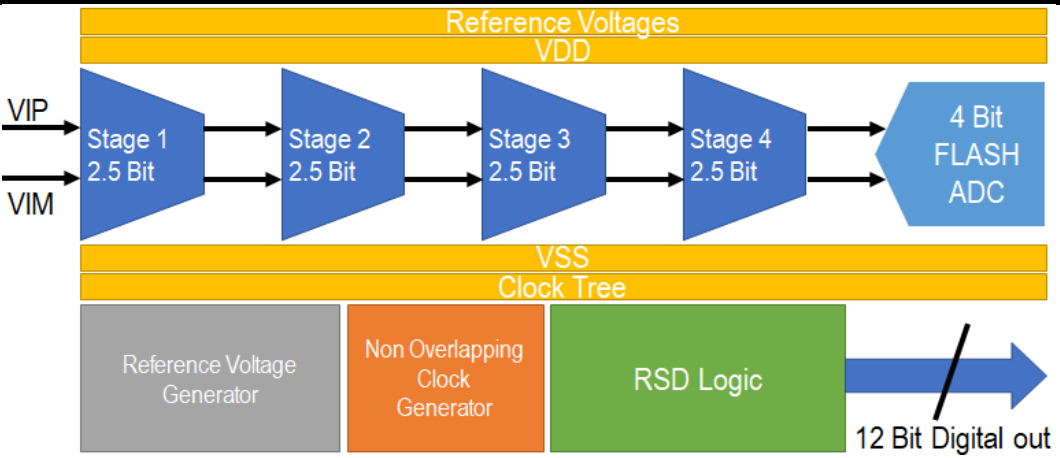

Rise time change by using the programmability function

| # | CSA1 | CSA1 with programmability | CSA2 | CSA3 |
|---|---|---|---|---|
| Equivalent Noise Charge(ENC) worst case (electrons) | 533 | 556 | 1.8K | 480 |
| ENC rate (electrons/pF) | 22.25 | 22.25 | negligible | 22.25 |
| Rise Time typical (ns) | 92 | 92 | 208 | 20 |
| Gain (mV/fC) | 30.45 | 30.45 | 29.8 | 2.3 |
| Rise time programmability (ns) | NA | 50n-200 | NA | NA |
| Gain Programmability (mV/fC) | NA | 15-60 | NA | NA |
| Fully Differential Output | Yes | Yes | Yes | Yes |
| Common Mode of Full Differential Output | 0.8-1 | 0.8-1 | 0.8-1 | 0.8-1 |
| Shaper Circuit | Yes | Yes | Yes | No |

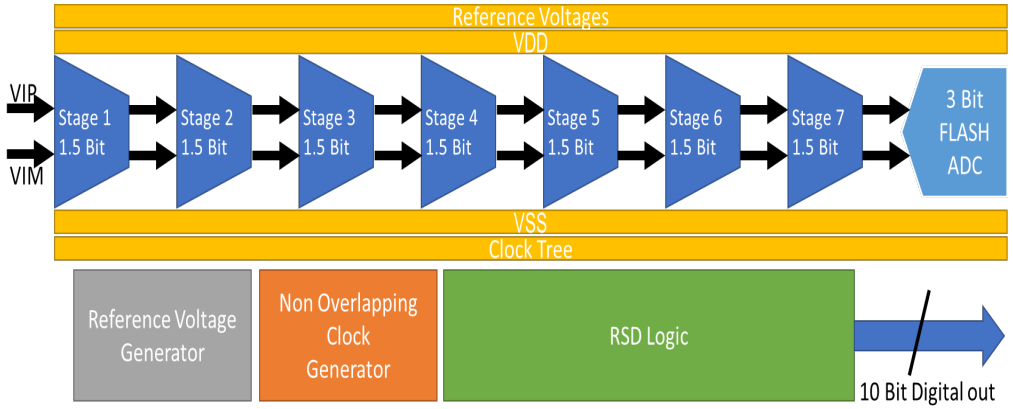




# Analog to Digital Converters

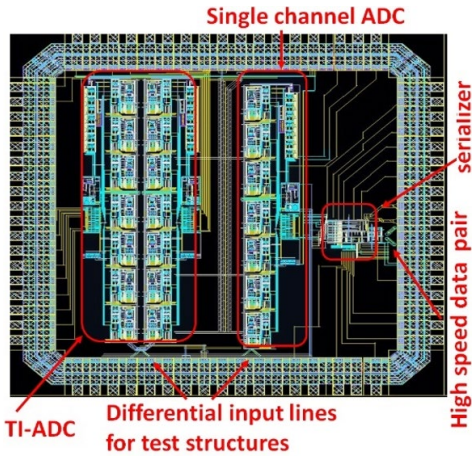
Robust High Performance Microelectronics



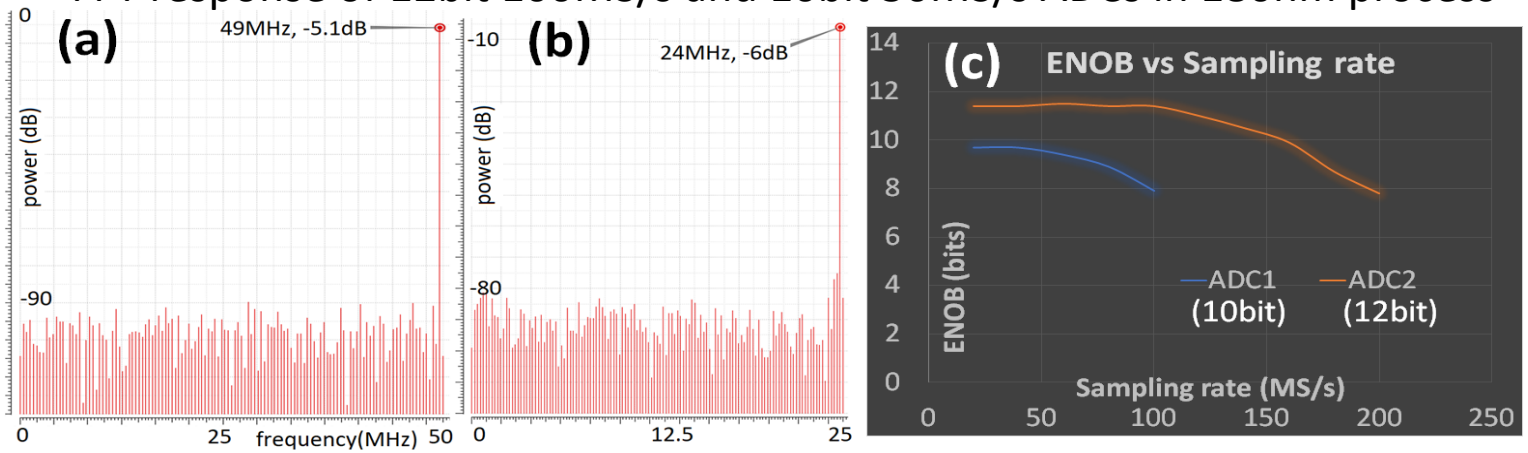

12bit 100MS/s ADC. Power < 90mW



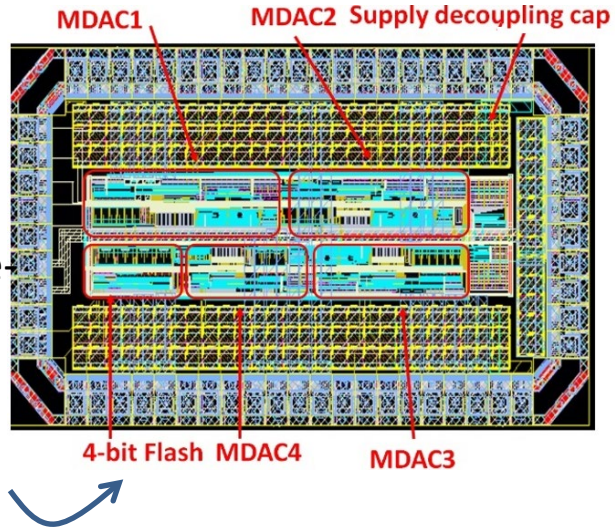

10bit 50MS/s ADC Power < 7mW

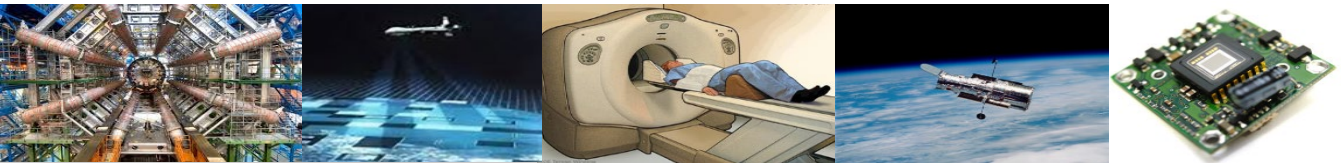



FFT response of 12bit 100MS/s and 10bit 50MS/s ADCs in 180nm process




10bit 50MS/s ADC (top) in different configurations (including time-interleaving) and 12bit 100MS/s ADC (bottom)

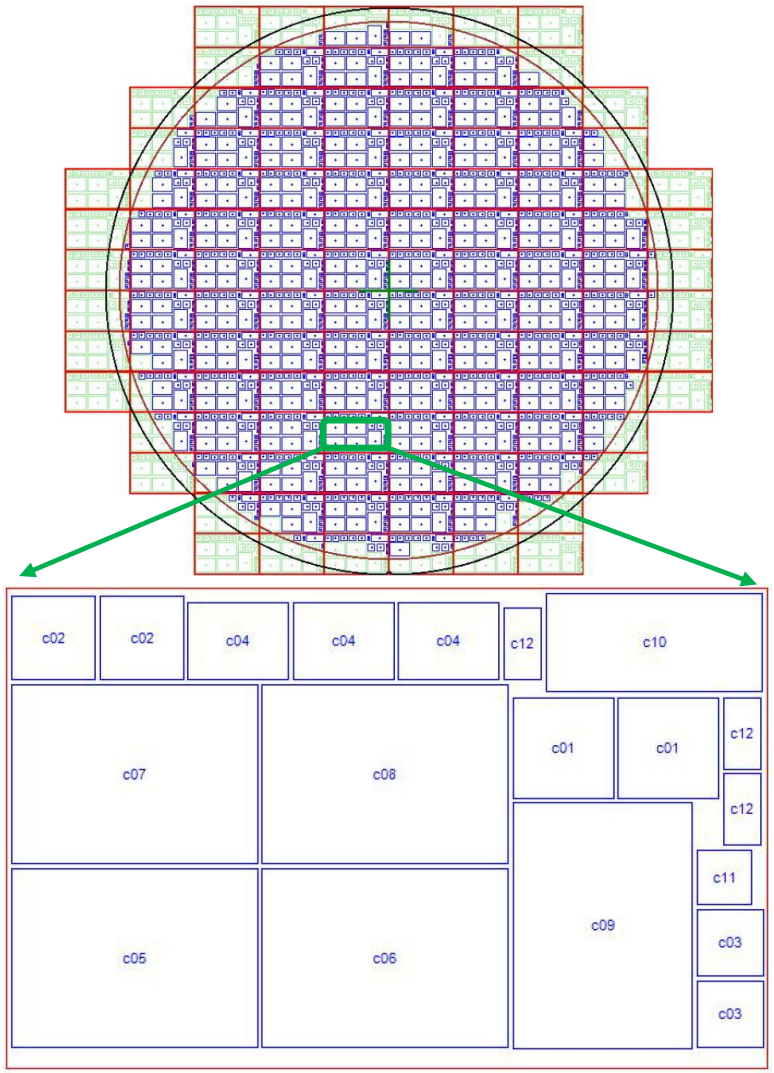


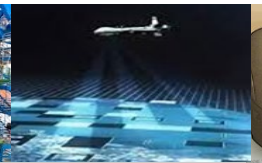
# Multi-Channel Readout IC for Nuclear Physics Experiments: Step 1, Tapeout 1

ALPHACORE

Robust High Performance Microelectronics




| Chip Name | Chip Part Number | Design |
|---|---|---|
| ADC | XF01D18_7017_03 | Standalone 12 bit ADC |
| CHIP1 | XF18002K18_7030_01 | Preamps Top_Level_preamp_test Top_Level_preamp_fast_test Top_Level_preamp_programmable_test Top_Level_preamp_cc_test Top_Level_preamp_cc_programmable_test |
| CHIP2 | XF18002K18_7030_02 | TI ADC+single channel TestADC +Serializer |
| CHIP3 | XF18002K18_7030_03 | 16to1 Serializer test structure |
| CHIP4 | XF18002K18_7030_04 | 3 different versions of pre-amps+10 BITADC |
| CHIP5 | XF18002K18_7030_05 | Multi Channel Preamp_Fast (16) |
| CHIP6 | XF18002K18_7030_06 | Multi Channel Preamp_Programmable |
| CHIP7 | XF18002K18_7030_07 | Multi Channel Preamp_programmable_cc |
| CHIP8 | XF18002K18_7030_08 | Multi Channel 10-Bit ADC+Serializer |
| CHIP9 | XF18002K18_7030_09 | Multi 12BIT ADC+Serializer |

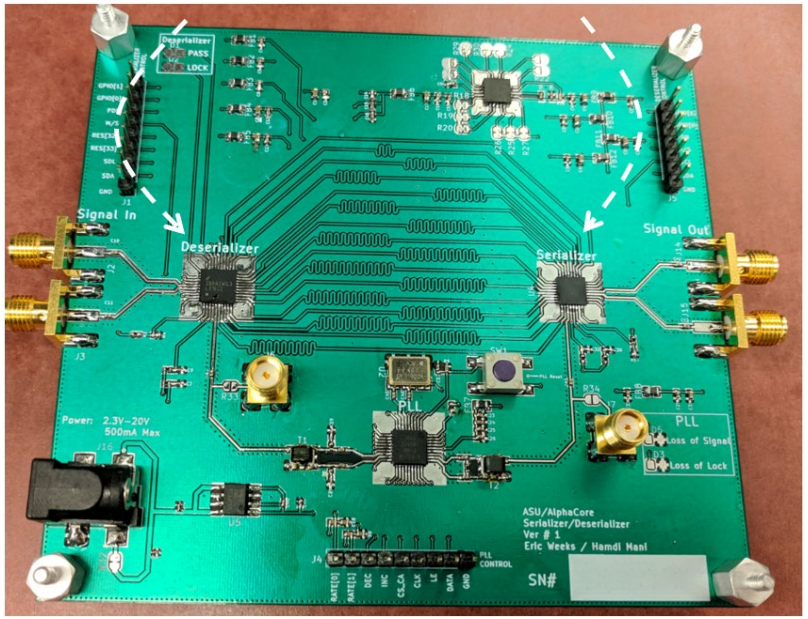

# Current Status



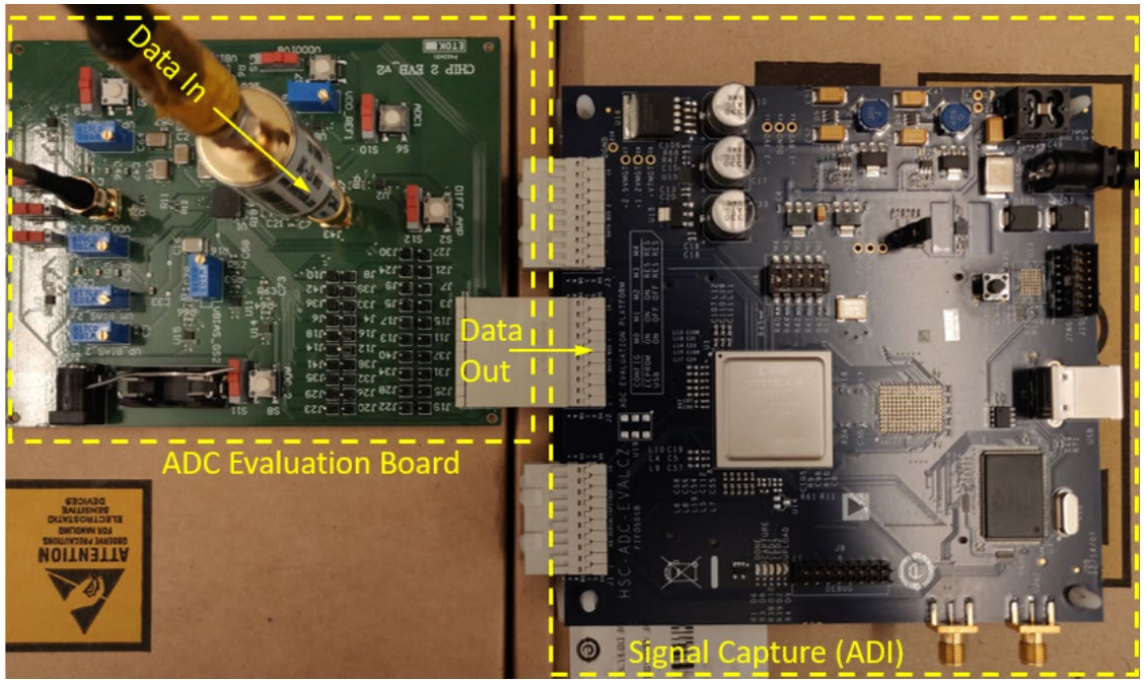
- All test chips fabricated.
- Critical test chips boards assembled. These include:
  - 10bit 50MS/s ADC test chip
  - 12bit 100MS/s ADC test chip
  - CSA test chip test Serializer test chip

Testing started last week. Under progress. **Expected to complete by end of September.**

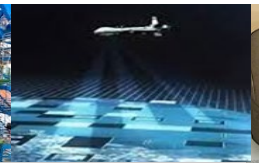
Deserializer Serializer




ADC evaluation board with data capture and processing board





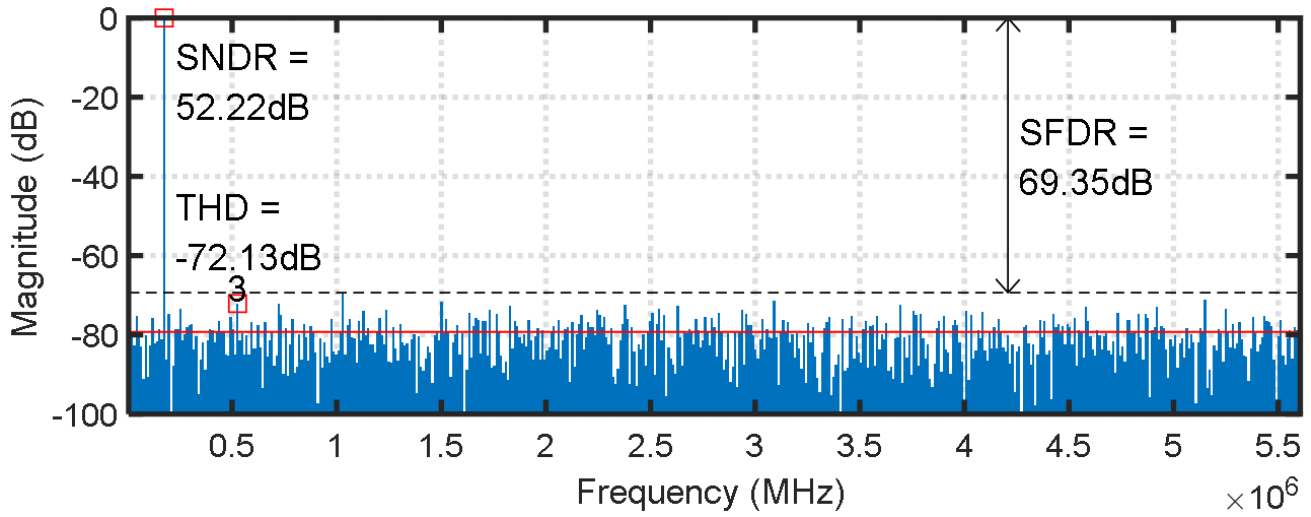



# Alphacore's Other Silicon Evaluated Digitizers for Nuclear Physics Experiments

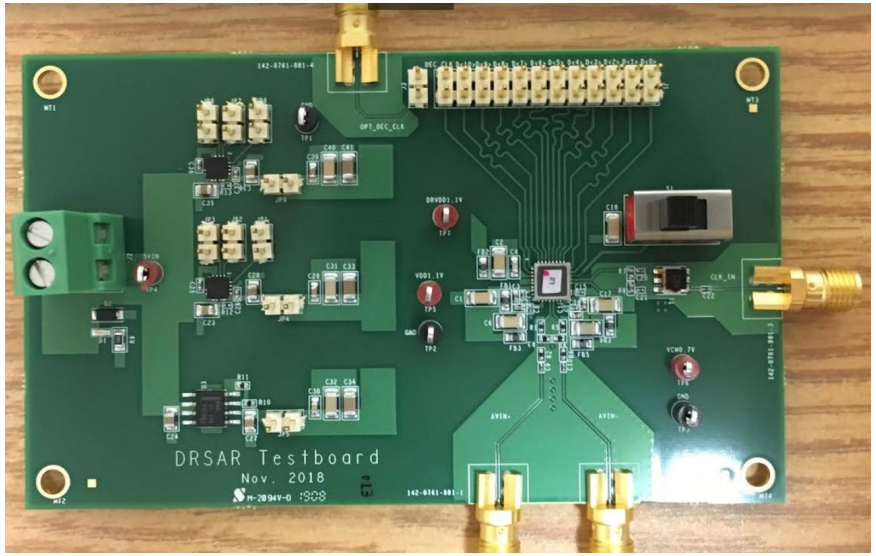
# A 10B500M, 10bit, 500MSa/s, Ultra Low Power ADC

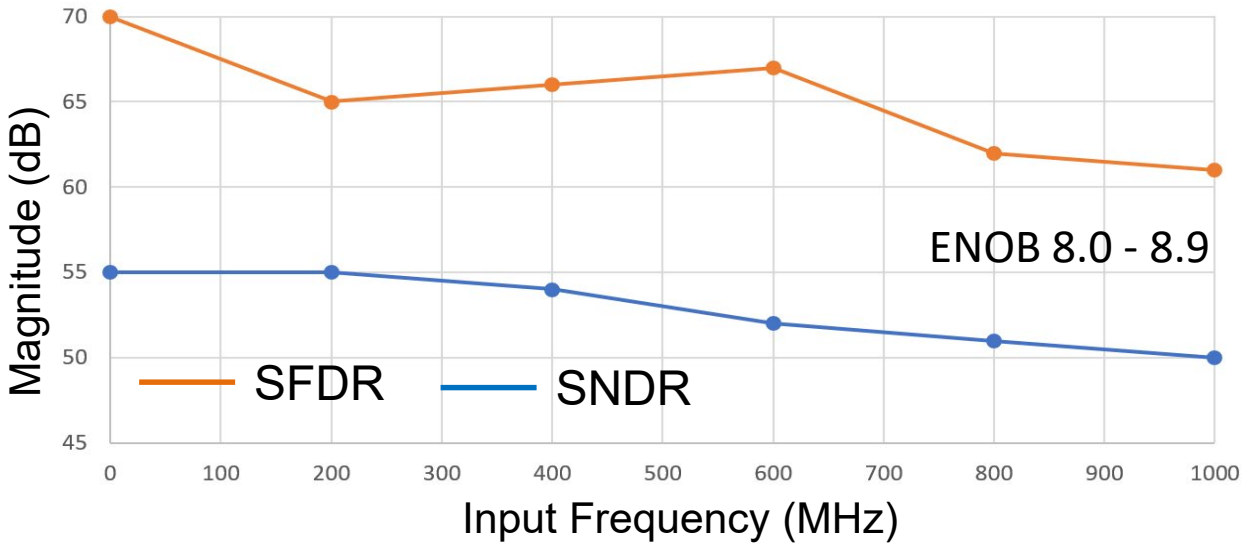
ALPHACORE

Robust High Performance Microelectronics




Output decimated by a factor of 49 in this testing set up



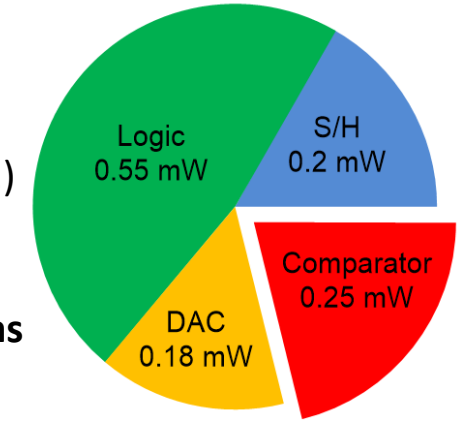




Single channel ADC with wide input bandwidth (beyond 4th Nyquist zone)

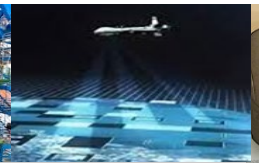
ENOB 8.0 - 8.9 over four Nyquist bands

Ultra Low Power <1.18 mW (FOM <6.0fJ/conv.)

**Can be used as the unit channel in a 10-bit, time-interleaved ADC with sample rate of tens of GSa/s**

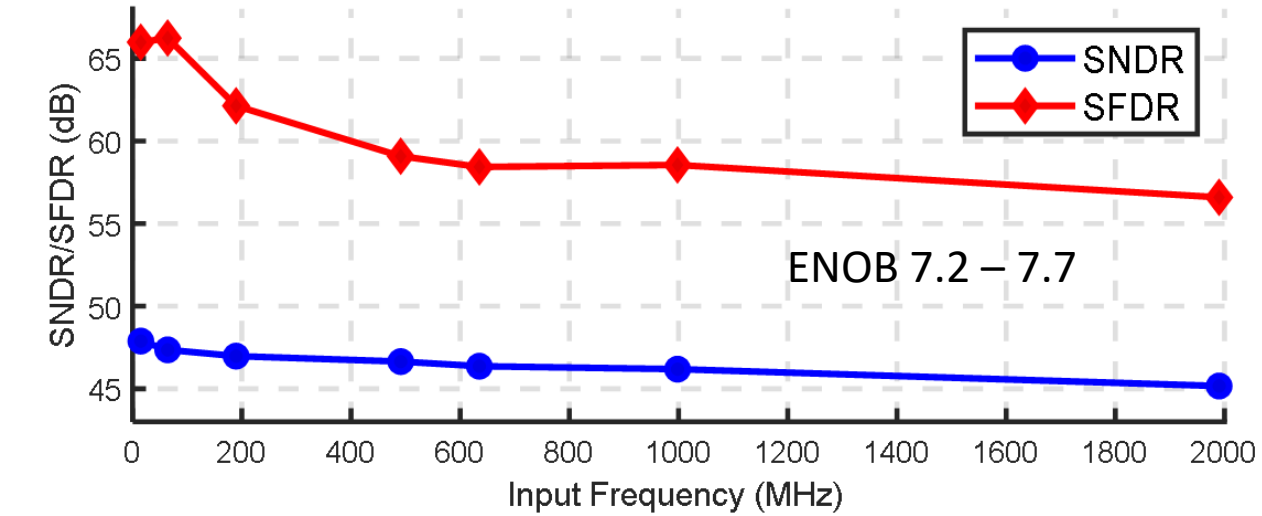


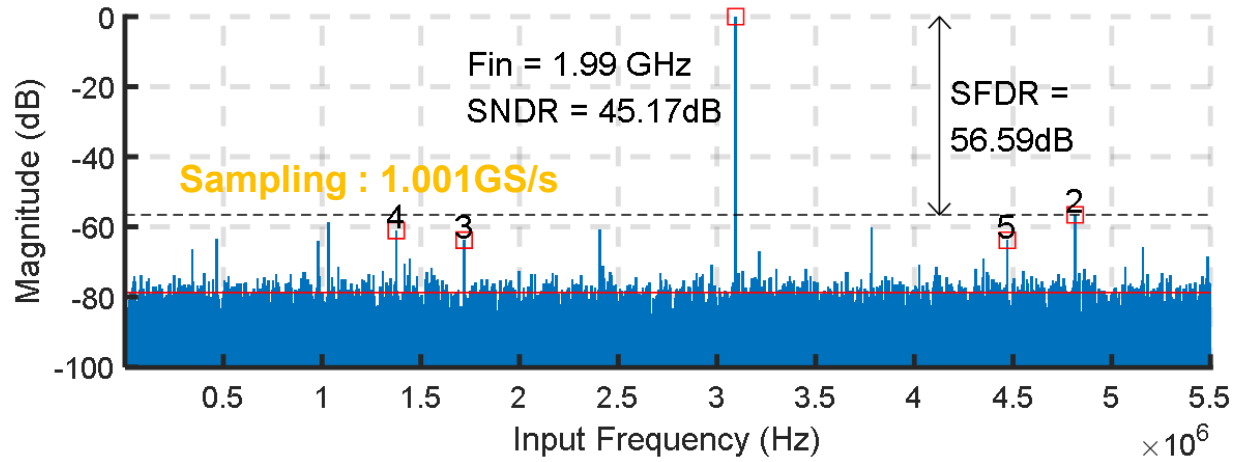

Power dissipation breakdown



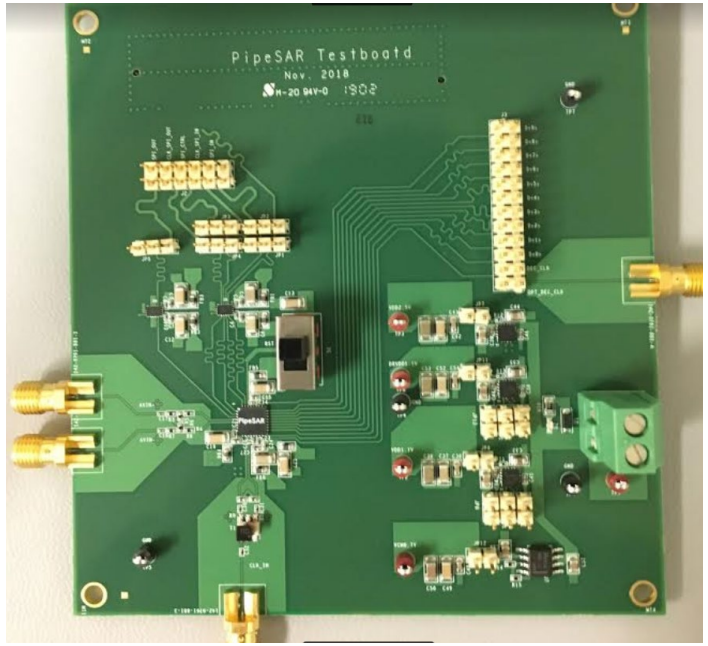
# A9B1G, Wide Input BW, 9-bit, 1GSa/s ADC






Output decimated by a factor of 91 in this testing set up

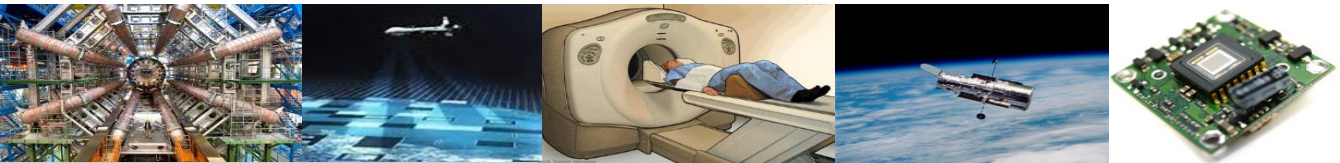



Single channel with **wide input bandwidth** (beyond 4th Nyquist zone)

ENOB stays within 7.2-7.7 over the first four Nyquist bands

Power <2.1mW (FOM < 10fJ/conv)

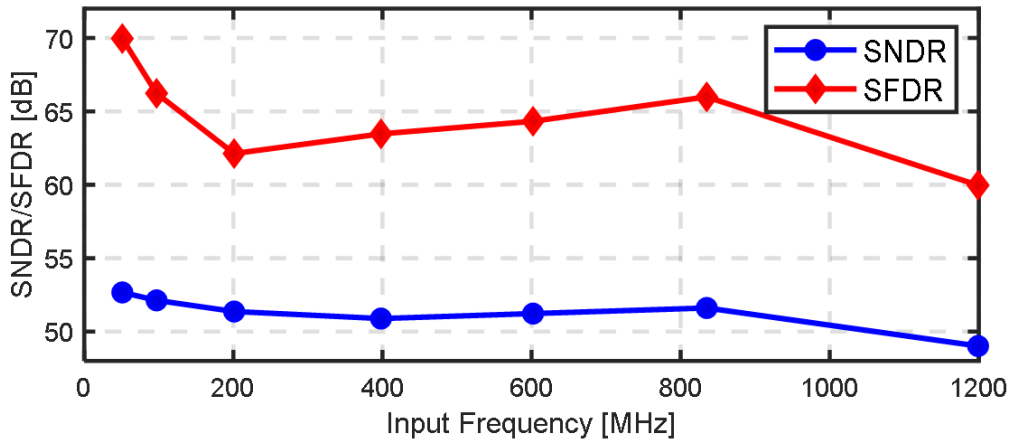
Can be used as the unit channel in a 10-bit, time-interleaved ADC with sample rate of tens of GSa/s

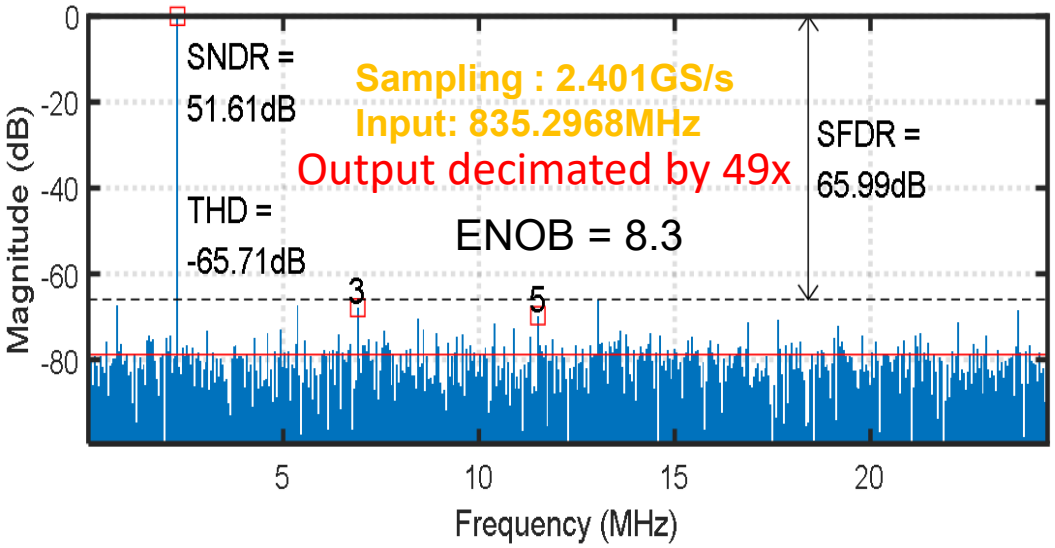


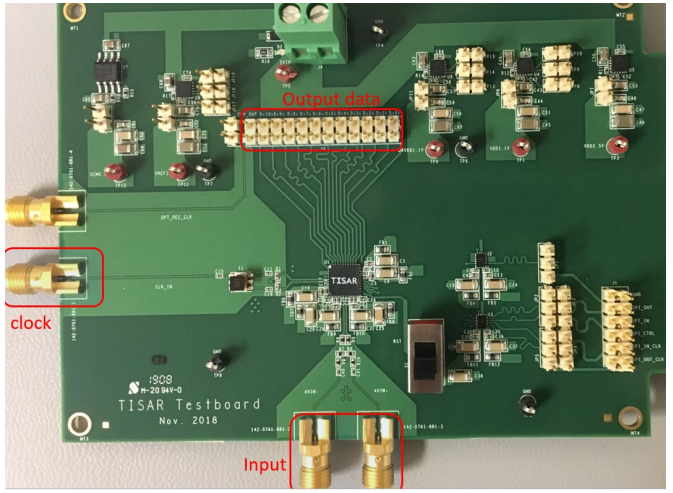
# A10B2G, 10 bit, 2.4GSa/s, Ultra Low Power ADC

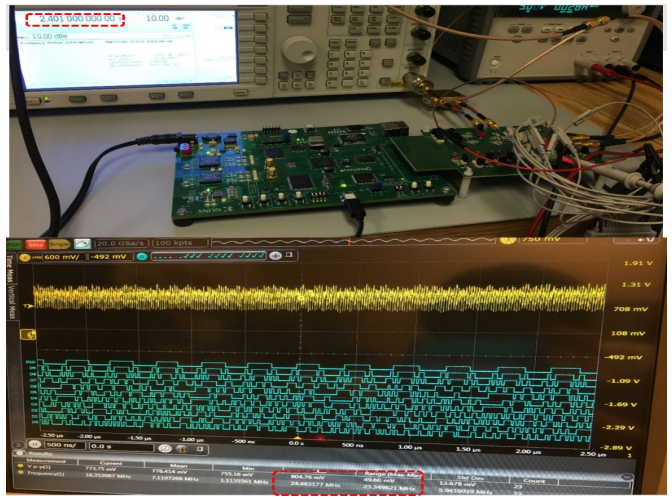
ALPHACORE

Robust High Performance Microelectronics



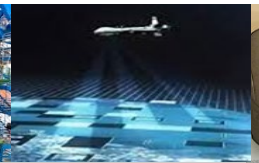



The ADC has a **8-way** interleaved architecture, with combined sampling rate of 2.4GSa/s. The sampling rate is limited by on-chip clock buffers. Optimized buffers would deliver **up to 3.2GS/s with 6mW of additional power.**

We can interleave **16-way**(on-chip) to achieve **6.4GS/s for continuous digitization with no dead time**

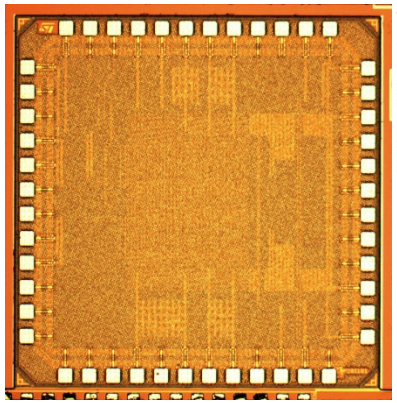
The **developed calibration algorithm** has been shown to be very effective for the calibration of interleaving spurs, in this case yielding SFDR of 60-70 dB and ENOB that varies from 7.9 bits to 8.5 bits in the first Nyquist band.

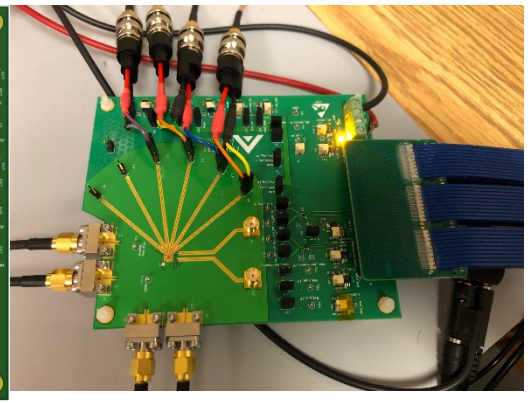
Power < 6 mW (FOM < 6.9fJ/conv)



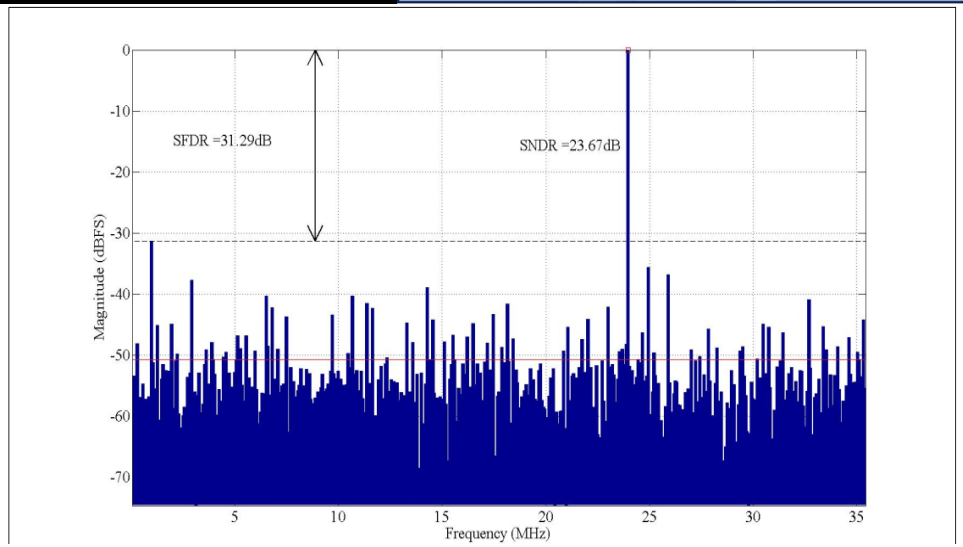
# 20GS/s 20GHz 6bit ADC





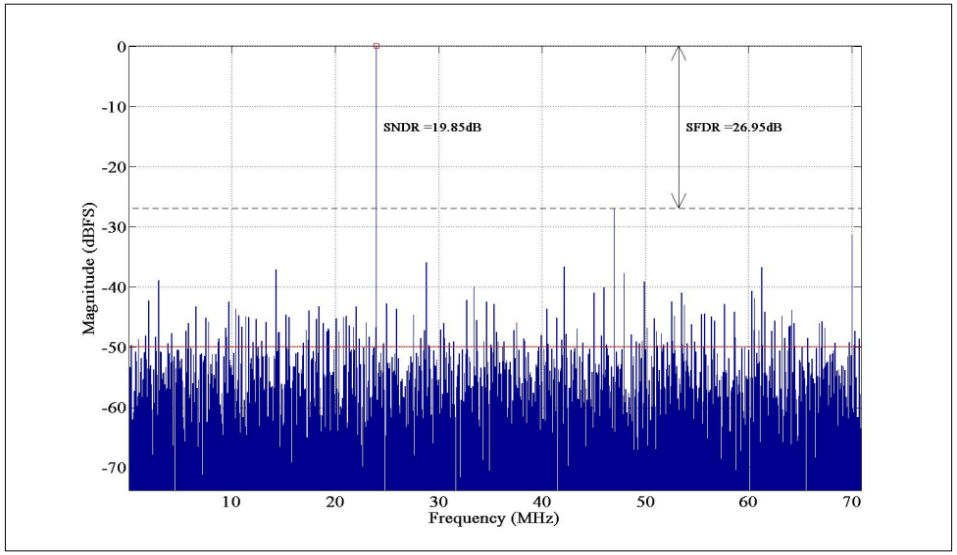


ENOB is 3.7 when tested at 9GSa/s and 8GHz input bandwidth

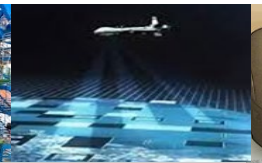



- IP functionality testing completed with a COB package.
- Development of a high-speed custom package with the lowest possible parasitics has been planned. The expected performance with a proper package is >4.5 ENOB, >20GSa/s, >20GHz and <300mW.
- The COB package and our current test setup allows testing the ADC at 16GSa/s and 8GHz.
- The goal is to be able to test beyond 20GSa/s sample rate and 20GHz input bandwidth

Measurements achieved for sampling frequencies up to 17.2GS/s with ENOB up to 3.3 bits

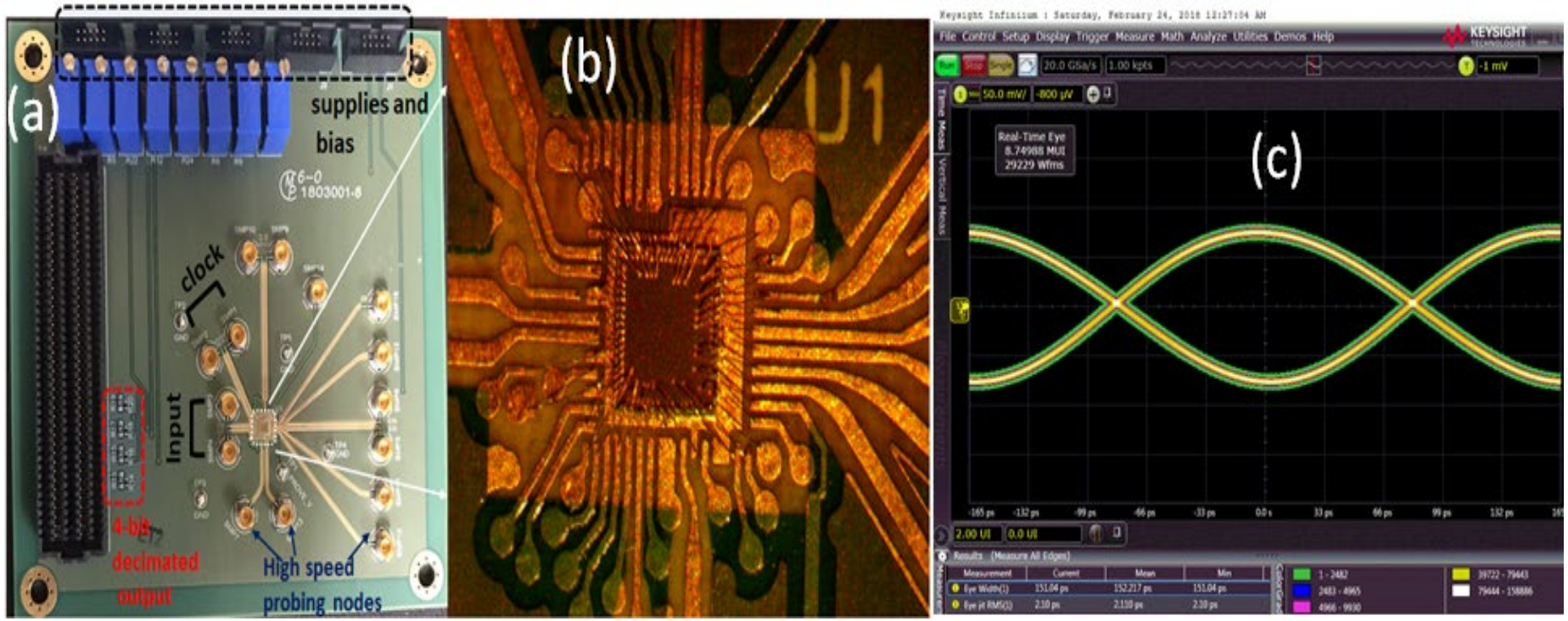



Output decimated by a factor of 126 in this testing setup

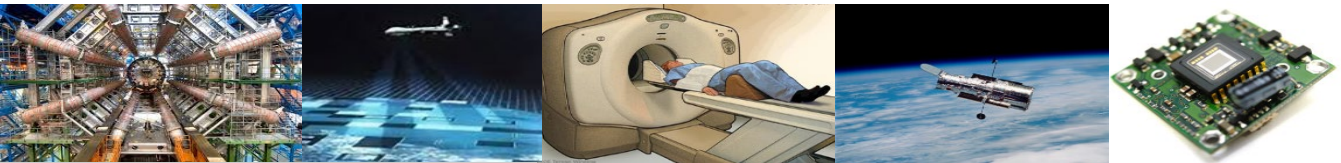




# High Speed Interface (CML drivers)

Robust High Performance Microelectronics



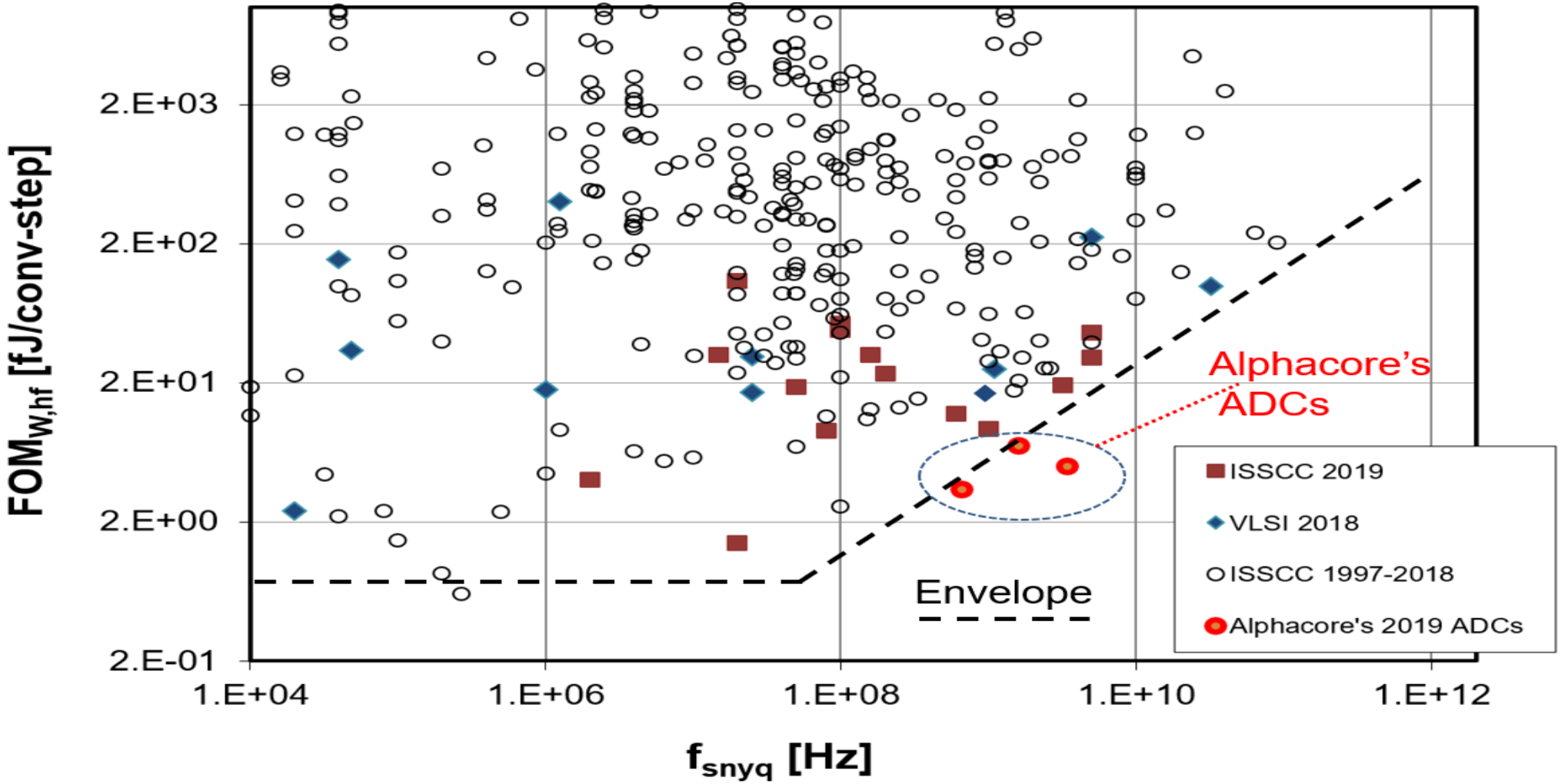

a) Alphacore's high speed digitizer evaluation board with high speed CML drivers (data rate up to 12GB/s) b) micrograph of the die c) oscilloscope measurement of the CML drivers at 6GB/s (limited by our low data rate board design) with RMS jitter of 2ps.



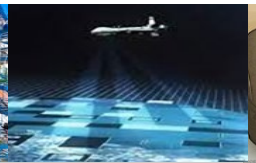
# Alphacore's Ultra Low Power ADCs Walden Chart comparison: FOM vs Speed

ALPHACORE

Robust High Performance Microelectronics








# Alphacore's Other Solutions for Nuclear Physics Experiments

# Radiation Hard High Speed Camera System for Accelerator Beam Diagnostics

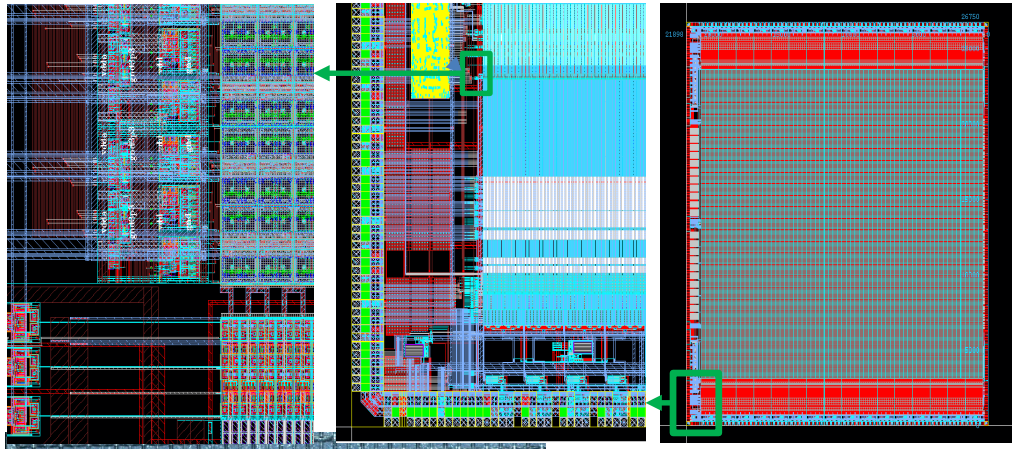
ALPHACORE

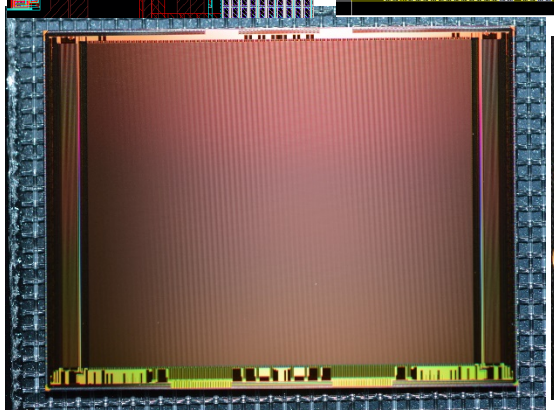
Robust High Performance Microelectronics

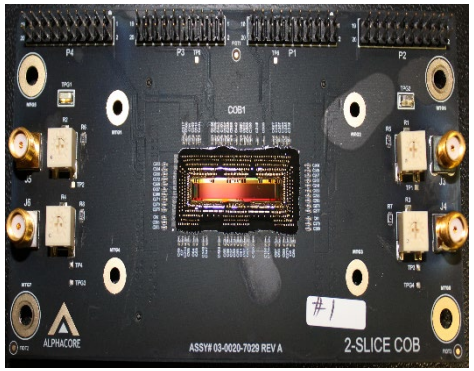
*Zoom: Px array, column bias, row decoders*

*Pixels, column ADCs, PLL*

*Full 1 Mpx chip 27mm x 22mm*

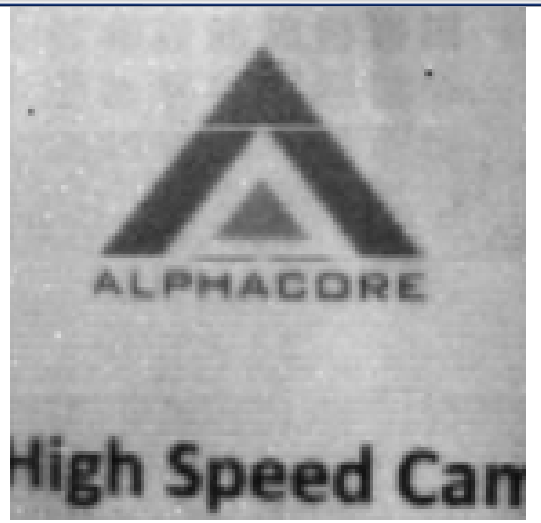






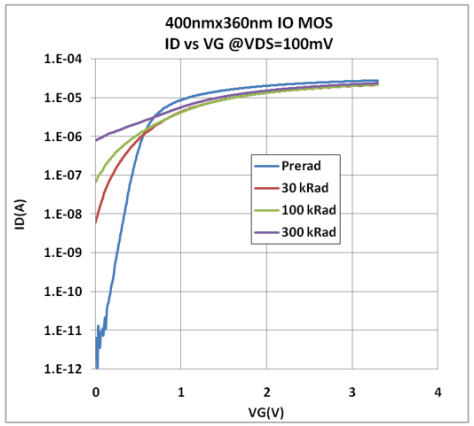

1024 x 768 10,000fps image sensor has been designed, fabricated, packaged and is currently under test.

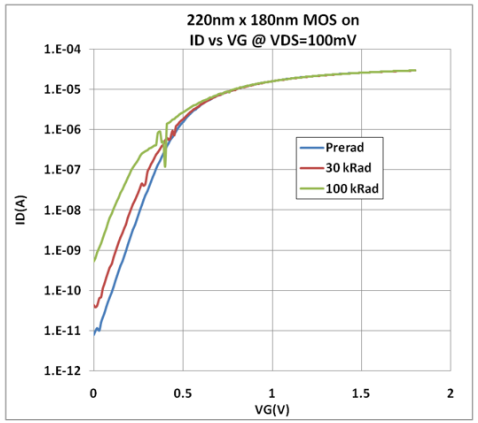
10,000-pixel image sensor and camera has been designed, built and evaluated. It operates up to 20,000 fps

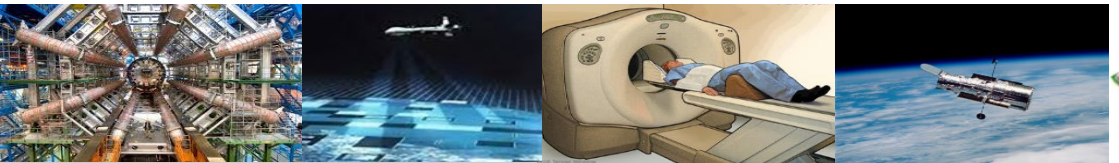



## TID Effects in CMOS Transistors and Pixels

Based on Co-60 tests, thick oxide NMOS has 100x higher leakage than core NMOS. The Alphacore image sensor uses core transistors for all supporting circuits outside the pixel array.



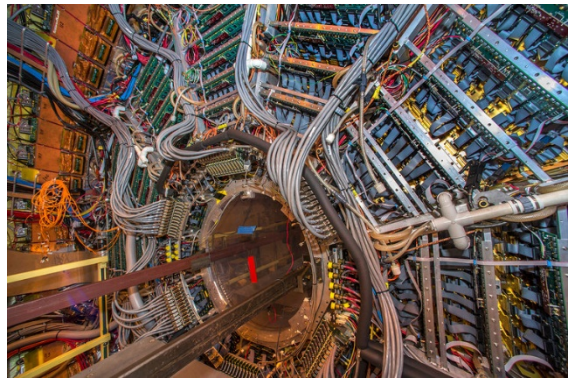



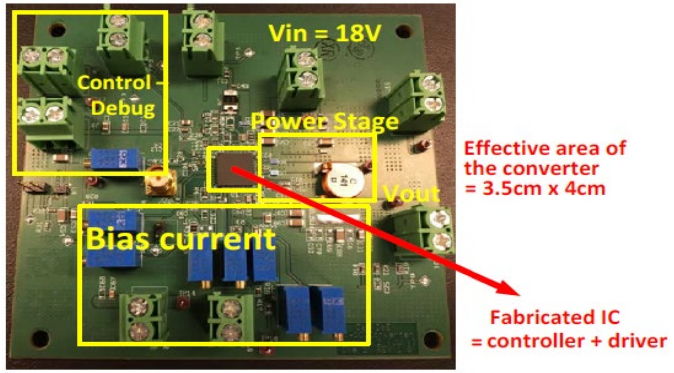
# Radiation Hard Point of Load (POL) DC-DC Converter for Large Detector Systems

ALPHACORE

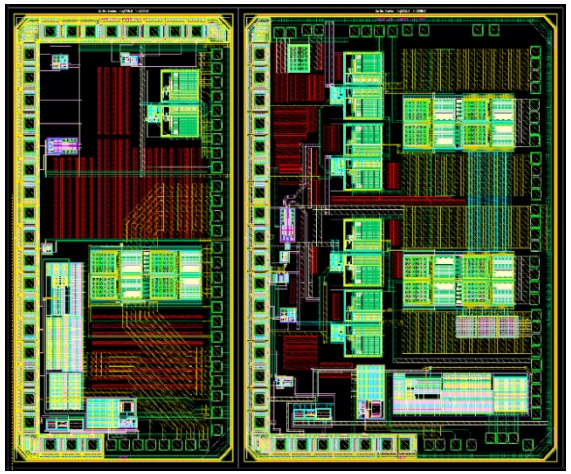
Robust High Performance Microelectronics



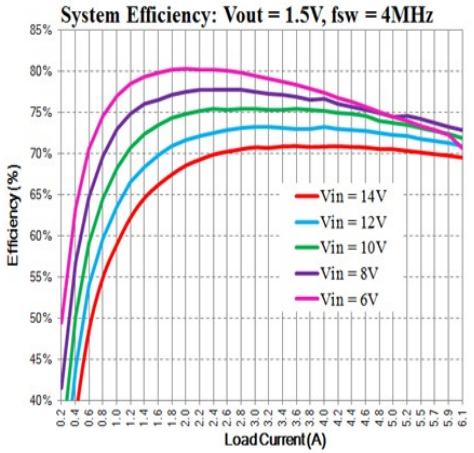
*Large Detector Experiment*



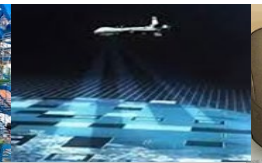

*Alphacore's rad-hard POL converter evaluation board*



*Alphacore's rad-hard POL converter controller ASIC*




*Alphacore's rad-hard POL converter test results*



POL DC-DC converter specs:
18V in, 1.2V – 5V out, 10A load current
Efficiency > 70%
Rad-hard to TID = 150Mrad
High magnetic field tolerance (no ferrite core inductors used)

Large detector experiments can significantly benefit from high input voltage POL converters which enable bringing the power to the core chips in the form of "high voltage - low current". Cooling needs will be much lower.

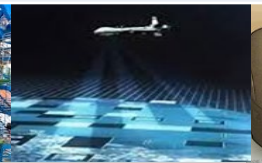
These DC-DC Pol converters need to be very rad-hard and magnetic field tolerant. Alphacore has designed and demonstrated such a device in a DOE SBIR program. Dense medical imaging scanners is another application.

# Other Relevant IP

ALPHACORE

Robust High Performance Microelectronics

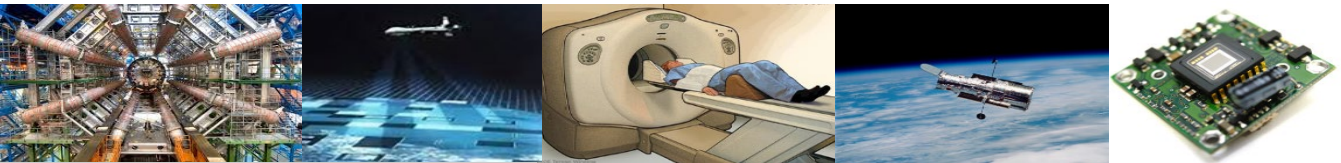
| | IP type | Status |
|---|---|---|
| 1 | 10b, 500MSPS, 2GHz, 1.2mW ADC core (radiation tolerant, 100krad) | Evaluated |
| 2 | 9b, 1GSPS, 2GHz, 2.7mW ADC core (radiation tolerant, 100krad) | Evaluated |
| 3 | 10b, 3GSPS, 3GHz, 18mW ADC core (radiation tolerant, 100krad) | Evaluated |
| 4 | 6b, 20GSPS, 20GHz, 220mW ADC core (radiation tolerant, 100krad) | Evaluated |
| 5 | Rad-hard multi-channel, 10-bit, 50MSPS, 7mW ADC ASIC (300krad) | Under evaluation |
| 6 | Rad-hard multi-channel 12bit 100MS/s, 90mW ADC ASIC (300krad) | Under evaluation |
| | Rad-hard multi-channel 50-200 ns rise time, 1GHz CSA ASIC with (300krad) | Under evaluation |
| 6 | Rad-hard, 12-bit, 50MSPS, 9mW ADC (300krad) | Under evaluation |
| 7 | 6b, 5GSPS, 16GHz, 25mW ADC core (radiation tolerant, 100krad) | Taped out |
| 8 | 10b, 5GSPS, 36mW, 3GHz ADC core (radiation tolerant, 100krad) | Tapeout Oct 2019 |
| 9 | 8b, 100GSPS, 40GHz, 80mW ADC core | Under design |
| 10 | 12b, 500MSPS DAC (radiation tolerant, 100krad) | Evaluated |
| 11 | 6GHz – 13GHz tunable, 360fs jitter PLL (radiation tolerant, 100krad) | Evaluated |
| 12 | 12Gb/s transceiver I/Os (radiation tolerant, 100krad) | Evaluated |
| 13 | Rad-hard 56Gb/s PAM4 Transceiver (1Mrad) | Tapeout in 2020 |
| 14 | Rad-hard 27b dynamic range 256 X 256 IR DROIC (300krad) | Tapeout Sep 2019 |
| 15 | Rad-hard 20b dynamic range 32 X 32 flash LIDAR receiver (300krad) | Tapeout ready as of June 2019 |
| 16 | Rad-hard 1Mpix, 10,000fps videocamera, 300krad | Under evaluation |
| 17 | Rad-hard DC-DC converter, 14V-to-1.5V, 7A, 1Mrad | Prototype tested (product chip under testing) |
| 18 | Rad-hard Li-Ion Battery monitor, 300krad | Tapeout completed in June 2019 |
| 19 | In-package chip use time monitor | Under evaluation |
| 20 | On-chip identification and authentication monitor | Evaluated (First prototype demoed) |
| 21 | Rad-hard reconfigurable satellite power distribution ASIC, 300krad | Tapeout August 2019 |
| 22 | 12b, 6GSPS DAC | Tapeout Fall 2019 |
| 23 | 12b, 1TSPS Waveform Digitizer ASIC | Tapeout Fall 2019 |
| 24 | Sensor self-calibration monitor/controller | Taped out July 2019 |


# Summary



- The DOE Nuclear Physics STTR Phase II program reviewed in this presentation strengthens Alphacore's digitizer and readout ASIC family offered to Nuclear Physics, Scientific, Space and Defense customers.
- The program is advancing at a fast phase: Complete ASICs are currently being evaluated at the end of the Year 1.
- This presentation also summarized Alphacore's silicon evaluated ADCs and other IP relevant to Nuclear Physics researchers

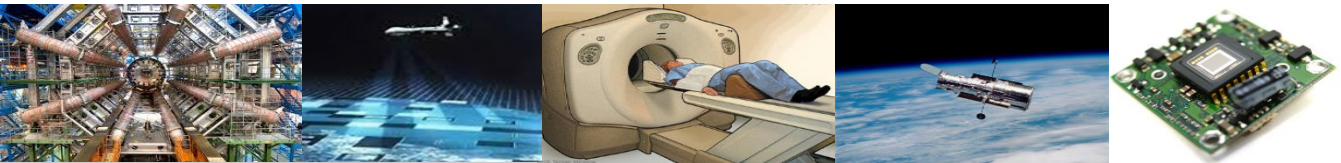


# Acknowledgement



Work on this program was funded by Department of Energy / Nuclear Physics, Grant #DE-SC00017074.

We especially appreciate the guidance by Dr. Manouchehr Farkhondeh and Dr. Michelle Shinn.



# Questions?