12-bit 32 Channel 500MSps Low Latency ADC

Award Number: DE-SC0017213
Summary of year 1 progress, Ph II project
Presentation Outline

• The Company, its Specialization/Expertise
• A List of Successful Projects
• Used IC Fabrication Technologies
• Current Project - 12-bit 32 Channel 500MSps Low Latency ADC:
  • Relevance to the NP Program
  • Project Goals
  • Chip Description
  • Project Schedules and Milestones
• Plans for the Future
The Company

- Pacific MicroCHIP Corp. was incorporated in 2006.
- It is headquartered in Culver City, California.
- Main focus of the company – providing IC/ASIC design services and turnkey solutions.

Office in Culver City, CA
Our Offerings

IC/ASIC Design Services:

• Circuit Design (analog, RF/mixed, digital)
• Simulation
• Physical Design
• Chip Assembly

Turnkey Solutions:

• IC Design
• Chip Fabrication Logistics
• Package Development (involving a 3rd party)
• Chip Packaging (involving a 3rd party)
• PCB Development for Testing/Eval. (involving a 3rd party)
• Testing/Characterization (an in-house lab)
• Delivery of Chips, Parts and Board Level Solutions
Core Expertise

- Analog (ADC/DAC, CTF, VGA, BG, LDO)
- Mixed Signal (PLL, CDR, SerDes, MDrv, TIA)
- RF (LNA, Mixer/Modulator, PA)
- Digital (Verilog, RTL, P&R, Timing Closure, DFT, Verifications)
- Layout (SiGe/CMOS) down to 7nm
A List of Successful Projects

- 12-bit 32 Channel 500MSps Low Latency ADC ➜ Being presented.
- A spectrometer ASIC 4GHz BW, 6-bit@8GSps, 8K frequency bins.
- A correlation radiometer ASIC 2xI/Q inputs, 2-bit@20GSps, cross-correlation within 16 bands.
- 20GS/s 6-bit ADC ASIC.
- An 8-bit up to 56GS/s ADC.
- A fiber-optic TRx ASIC for 200Gbps. Includes 4xADC/DAC (8-bit@56GSps).
- An 8-bit up to 64GS/s DAC for fiber optic >400Gb/s Tx.
- A laser controller ASIC for 100-400Gbps fiber optic modules. Includes 12-14-bit DACs, ADCs, TIAs, PIDs, PWM, etc.
- A low power RF TRx ASIC for medical pill endoscopes. Tx 433.8MHz (1mA), Rx 13.56MHz (2mA).
- A low Power Rx front end (TIA) for up to 4x28Gb/s NRZ realized in 130nm SiGe.
- A low power up to 4x32Gb/s NRZ MZ modulator driver realized in 180nm SiGe.
- A low power up to 2x56Gb/s PAM4 MZ modulator driver realized? in 180nm SiGe.
- A cross-correlator ASIC including 128 2-bit 1GSps ADCs and a 64x64 cross-correlator matrix.
- A dual transceiver ASIC with eFEC/FEC (5M gates) for 8.5Gb/s to 11.3Gb/s fiber optic networks.
- An EDC receiver with an analog Viterbi for fiber optic networks from 8Gb/s up to 11.3Gb/s.
- A UWB transceiver in 180nm SiGe.
IC Technologies Used – down to 7nm node

- indicates previously used node
Relevance to the NP Program

NP detectors require thousands of signal processing channels => need for digitizers to:

• Shrink in size - our ASIC combines independent 32 ADCs per chip.
• Reduce power consumption - we offer 25mW per ADC.

Upgrades in these systems demand for:

• Digitizing accuracy - our ADC features 12-bit resolution.
• Adequate sampling speed - our ADC features 0.5GS/s.
• Low conversion latency - we offer 8ns.

Targeted specific applications:

• Low latency particle beams control systems.
• Imaging and spectroscopy systems for gamma-ray detectors.
• Multichannel detectors based on tube and silicon photo multipliers.
Project Goals for Phase II

Within this project we will:

• Design circuits and layout for the ADC ASIC.
• Fabricate the chip.
• Develop a special chip carrier.
• Package the chips.
• Develop a test PCB and a DUT socket.
• Develop a GUI and a test bench.
• Test and characterize the ADC ASIC.
• Prepare a datasheet for marketing.
• Submit deliverables to the DoE.
Specifications Include:

- 32 independently operated ADC channels
- 500 MS/s sampling rate
- 0.6Vpp differential input swing
- 10-bit ENOB
- 250MHz Input signal bandwidth
- -40C..+125C temperature range
- 25mW/channel power consumption (with interface)

- JESD204B output data interface
- 8ns latency (direct ADC data output mode)
- 32x8Gb/s output data rate
- I2C interface for ASIC control
- 8.7mm² estimated ASIC layout footprint
- Solder bumped die in a BGA package
- 28nm CMOS technology
12-bit 32 Channel 500MSps
Low Latency ADC

ASIC Block Diagram
12-bit 500MSps ADC Core Block Diagram

- Two-times time-interleaved ADC core
- Sampling clock skew adjustment
- Two-stage pipelined SAR architecture
- Programmable residue Amp gain
- Programmable ADC FS range
- Bootstrapped input switches
- 1-bit redundancy between ADC stages
ASIC Top-level Layout

Chip’s periphery:
32 independent ADC channels located in 2 circles

Central part:
• PLL with a clock tree
• Temperature sensor
• CPU for calibration
• I2C control interface

Single ADC channel

Pacific MicroCHIP Corp.
ASIC Bump Map

Clock distribution network

Clock arrival time to ADC channels is matched to support data alignment
12-bit 32 Channel 500MSps
Low Latency ADC Power Budget

ADC channel power budget, 25mW

- OUTPUT DATA INTERFACE: 11.4
- SUB-ADC1 [12bit 250MS/s]: 6.2
- SUB-ADC2 [12bit 250MS/s]: 6.2
- CLOCK GENERATOR: 0.36
- DATA SYNC: 0.17
- OFFSET CANCELLATION: 1.05

Sub-ADC power budget, 6.2mW

- ADC STAGE1 [5bit 250MS/s]: 1.1
- ADC STAGE2 [8bit 250MS/s]: 0.9
- RESIDUE AMPLIFIER: 4.2
**Expected Part Appearance**

BGA 18 x 18 balls, 0.8mm ball pitch

Bypass capacitors on the chip carrier

Lid

Final part, top view

Bottom view

Note: Images are based on a previously developed similar BGA package.
### Comparison to ADCs Available on the Market

<table>
<thead>
<tr>
<th>#</th>
<th>Vendor</th>
<th># of Channels</th>
<th>Sample Rate, MS/s</th>
<th>Power Cons. per Channel</th>
<th>Architecture/Latency</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>TI 12-bit ADS52J90</td>
<td>32</td>
<td>40</td>
<td>41mW</td>
<td>Pipeline/2.5us</td>
</tr>
<tr>
<td>2.</td>
<td>TI 12-bit ADS5403IZAYR</td>
<td>1</td>
<td>500</td>
<td>1W</td>
<td>Pipeline/240ns</td>
</tr>
<tr>
<td>3.</td>
<td>TI 12-bit ADS54T04IZAYR</td>
<td>2</td>
<td>500</td>
<td>1.15W</td>
<td>Pipeline/240ns</td>
</tr>
<tr>
<td>4.</td>
<td>ADI 12-bit AD9234BCPZRL7</td>
<td>2</td>
<td>500</td>
<td>1.5W</td>
<td>Pipeline/240ns</td>
</tr>
<tr>
<td>5.</td>
<td>Pacific Microchip Corp. 12-bit*</td>
<td>32</td>
<td>500</td>
<td>25mW</td>
<td>SAR/Pipeline/8ns</td>
</tr>
</tbody>
</table>

* Expected performance
**Project Milestones and Deliverables**

### Milestones for Year 1

1. Digital blocks are designed - RTL, synthesis, timing closure, P&R are finished
2. Analog circuits are designed and simulated
3. Circuits are integrated, ASIC's top level schematics are completed
4. Layout of cells and blocks is designed and verified
5. Parasitics are extracted, circuits are resimulated and optimized
6. ASIC's top level functionality simulated/verified
7. Layout is integrated and verified
8. Design is organized and submitted for chip's fabrication

### Milestones for Year 2

9. Chip is fabricated
10. Chip carrier is developed and fabricated
11. Chip is packaged
12. Test PCB is designed, fabricated and assembled
13. GUI is developed
14. ASIC is assembled on the test board
15. ASIC is characterized
16. Testing data is collected, conclusion is made on achieving the required parameters
17. Specifications/description of the ASIC's IP block are ready
18. Project is completed, final report is prepared and submitted to the DoE
Plans for the Future
What is Beyond Phase II?

• End of Ph II - the chip’s prototype is ready.
• Redesign chip based on testing results and the feedback from the customers.
• Fabricate the final chip.
• Test/evaluate it.
• Prepare chip description and datasheets.
• Organize the ADC ASIC design as an IP block and advertise it.
• Provide the chip to the DoE community and commercial customers.
We would appreciate any application ideas and customer leads for the presented ADC ASIC!

THANK YOU