Low Cost, High-Density Digital Electronics for Nuclear Physics

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SkuTek Instrumentation
SkuTek.com

Outline

- The company and its capabilities.
- Customers.
- Products.
- Description of the Phase II project.
- Relevance to the NP program.
  - Our products are used at Fermilab, Oak Ridge, Los Alamos, MSU-NSCL, LZ Dark Matter Search. All these were funded by the DOE.
  - Recently we are focusing on working together with the ANL Physics Division.
- Deliverables.
- Plans.
- Questions for the NP community.

The company and its capabilities

- The team has grown over the last year. We hired two physicists and two software engineers (one of them part time).
- We also worked with several interns listed on the Acknowledgement page.

Our focus:

Data acquisition (DAQ) for nuclear physics, high energy physics, and particle astrophysics.

We use digital techniques to acquire and process signals from nuclear radiation detectors.

Our capabilities:

- Electronic design.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors, especially Embedded Linux.
- Algorithms for pulse processing.
- Algorithm implementation in the FPGA (VHDL, Verilog) and in embedded processors (python, C).
- Processing data from nuclear detectors of any kind.
- Development of detector assemblies using scintillators, PMTs, or SiPMs.

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Our customers

University of Rochester

Houghton College

The University of Tennessee Knoxville

SFU Simon Fraser University Engaging the World

Université Laval

Augustana University

Los Alamos National Laboratory

Fermilab

Wiener Plein & Baus, Corp. — Worldwide Industrial-electronic Nuclear-electronic Ressources

Albert Einstein Center for Fundamental Physics

Universität Bern

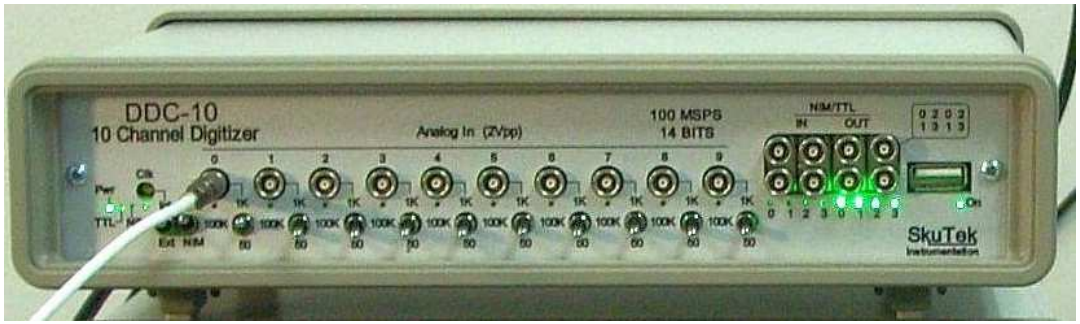
Shanghai Jiao Tong University

NSCL

National Superconducting Cyclotron Laboratory

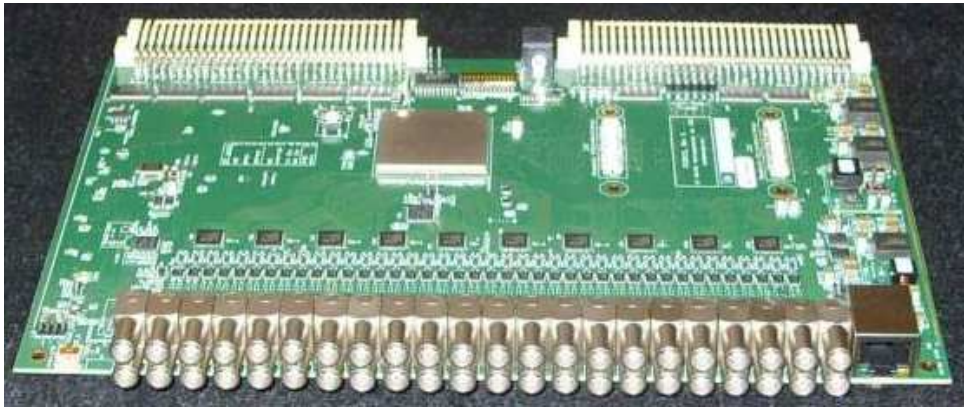
Data Acquisition Products

Standalone networked digitizer (10 channels)



Low cost networked digitizer (2 channels)

VME digitizer: 40 channels



Trigger / Logic module

Description of Phase II project

Problem or situation that is being addressed.

In Nuclear Physics there is need for cost effective, high density data acquisition (DAQ) systems with hundreds or even thousands of channels capable of signal monitoring and analysis.

How this problem or situation is being addressed.

We are developing digital DAQ modules with dozens of channels of waveform digitization, on-board FPGA, Ethernet, USB, and VME interfaces, and running Linux on-board.

The deliverables.

- The products will range from simple table-top units to systems with thousands of channels.
- The table top units will serve small NP experiments, radiation detector development, or student labs teaching Nuclear Physics.
- Large systems will serve experiments conducted at DOE facilities, e.g., Facility for Rare Isotope Beams (FRIB), which is a new national user facility for Nuclear Physics.

SkuTek DAQ Electronics for Dark Matter Search

SkuTek collaboration with UofR Physics and Astronomy

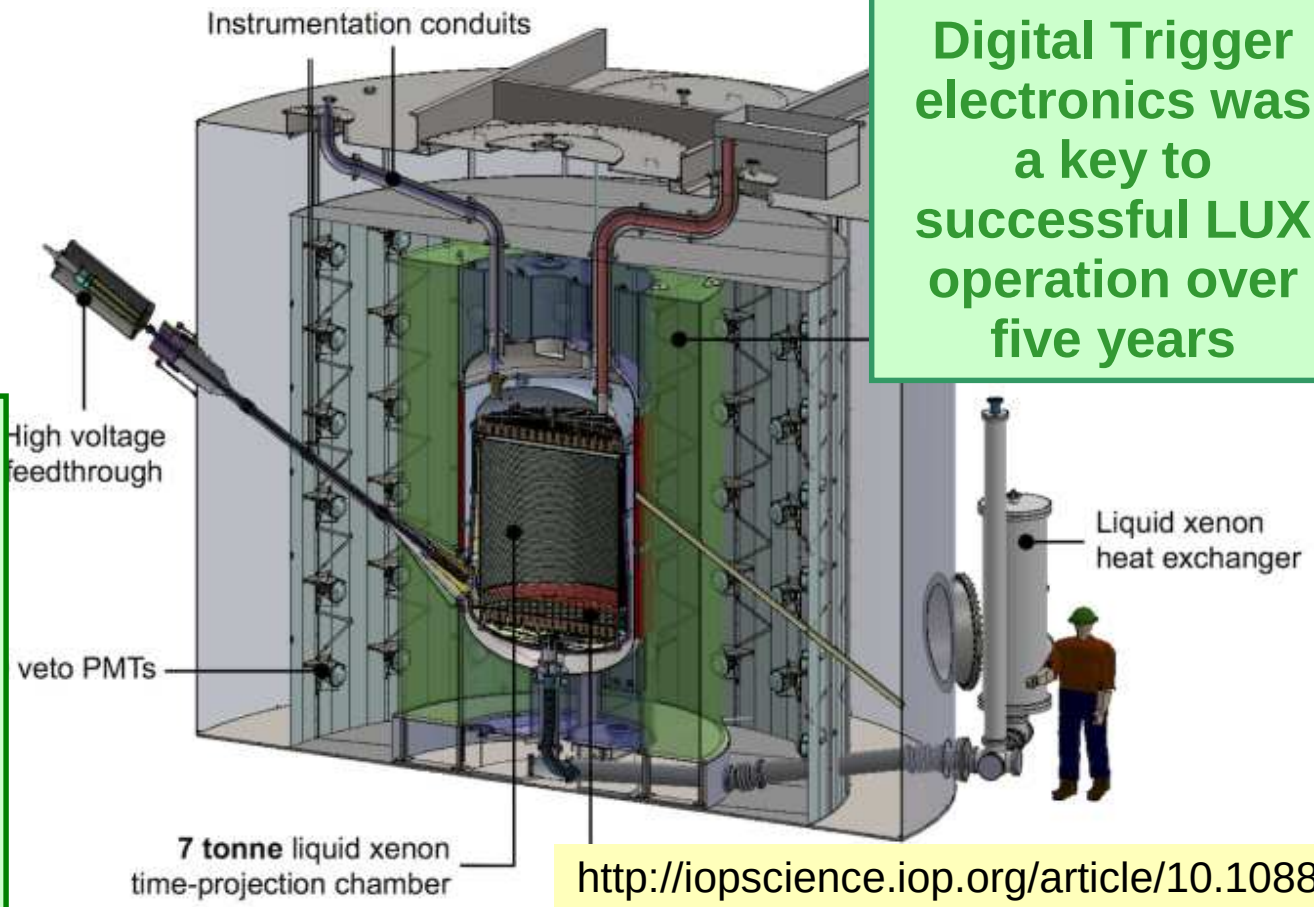
LUX-Zepplin is the “ultimate Dark Matter Search Detector”. Together with UofR we are building the digital DAQ for LZ with **1,359** channels. (Non-SBIR funding!)

This Fall we will deliver all the electronics to the LZ Collaboration (87 boards).

- Amount of Xenon: 5.6 tons fiducial
  - Drift time in Xenon: 700 µs.
- Number of PMTs: **745**
  - 614 with dual gain
  - 131 single gain
- Electronic channels:

  2*614 + 131 = **1,359**.

- **SkuTek DAQ electronics**
  - **Low noise**
  - **Flexible connection topology**
    - **GbE TCP/IP 40 MB/s**
    - **GbE UDP 109 MB/s**
    - **Fast Serial Links 400 MB/s**
  - **Powerful on board processing**
    - **FPGA**
    - **Embedded Linux**



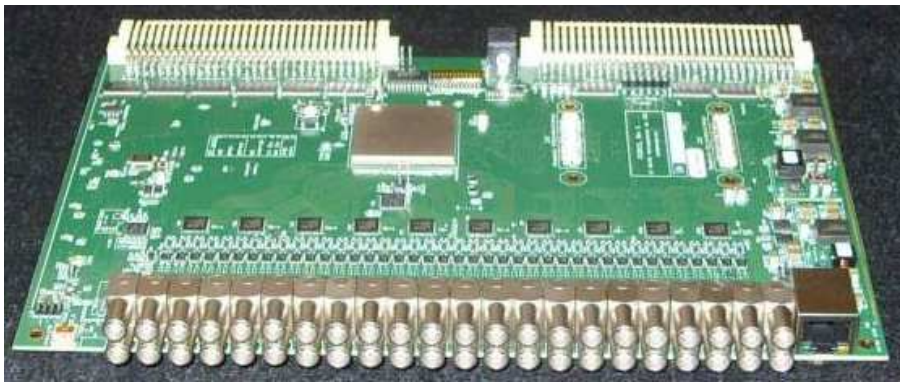
SkuTek Digital Trigger electronics was a key to successful LUX operation over five years

http://iopscience.iop.org/article/10.1088/1748-0221/11/02/C02072

Electronics for the NP Data Acquisition Systems

A modern digital DAQ is composed of digitizers and the Trigger / Logic modules. The previous SkuTek designs employed Blackfin processors and Spartan-6 FPGAs. We have upgraded both the the digitizers and the Trigger/Logic with **ARM processors** and **Kintex-7**. The low density 10-channel digitizer is still using Spartan-6 (cost!).

High density digitizer: **40 channels**



Kintex-7

Low density standalone digitizer: **10 channels**

Spartan-6

Trigger / Logic module has been upgraded with ARM and Kintex-7

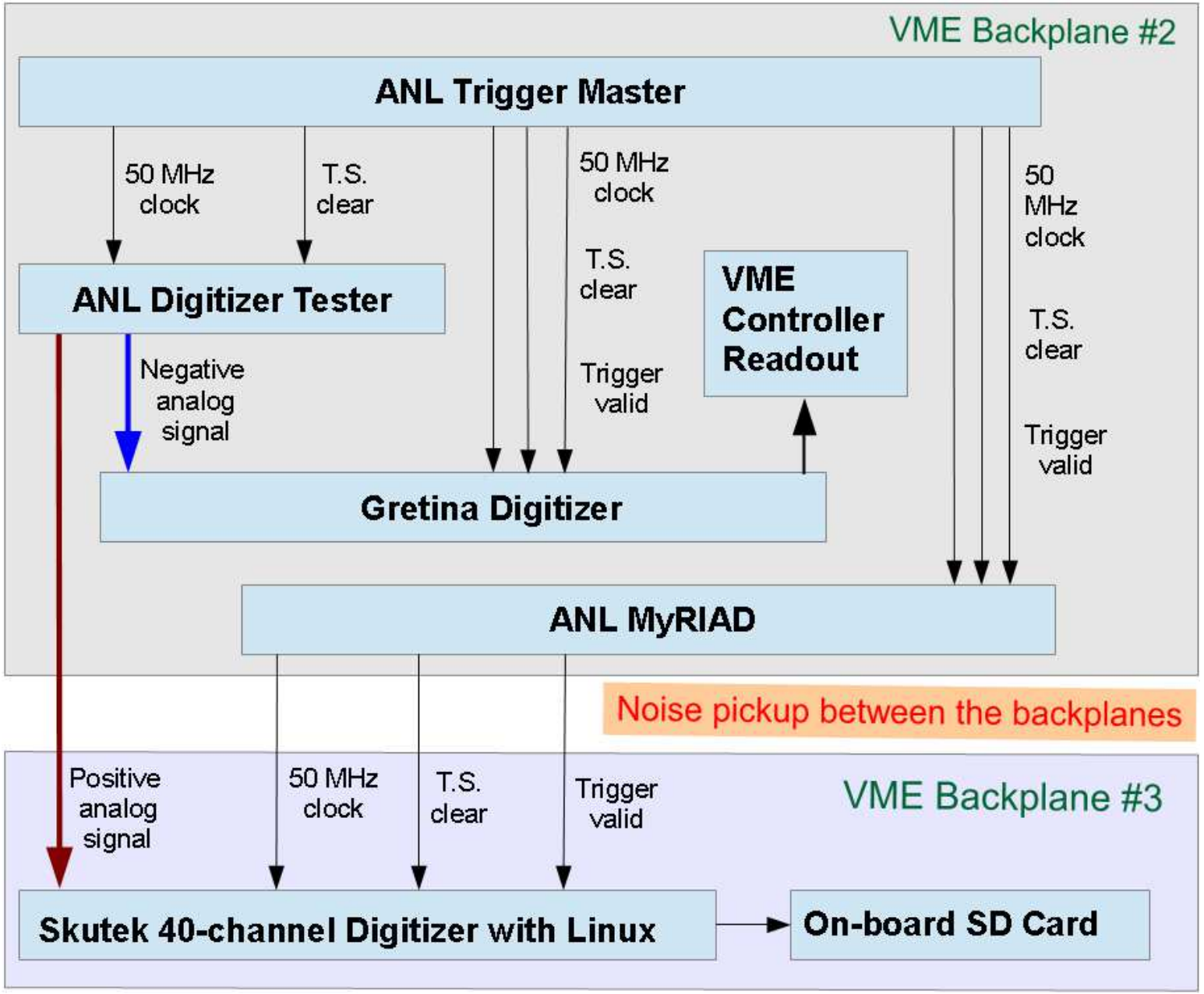
Kintex-7

The DDC-40 Digitizer

- Recently it has been demonstrated and evaluated at Argonne National Laboratory.

- 40 ADC channels:
  - 100 MHz sampling rate
  - ADC chip resolution: 12, 14, or 16 bits
  - 2V input range
  - +/-1V adjustable baseline
- Kintex-7 Xilinx FPGA, two options:
  - XC7K325T: BRAM=1,780 kB (**228 µs/chan**)
  - XC7K410T: BRAM=3,180 kB (**407 µs/chan**)
- Fast serial link over HDMI -> Trigger / Logic
- Temperature, voltage, current monitoring
- Embedded Linux Module with Ethernet, USB-2, and RS-232
- Remotely programmable:
  - Both the FPGA and the Linux Module
  - FPGA can be reprogrammed over Internet
  - Internal FPGA signals can be remotely accessed over Internet.

DDC-40 Was Tested in the ANL Physics Lab



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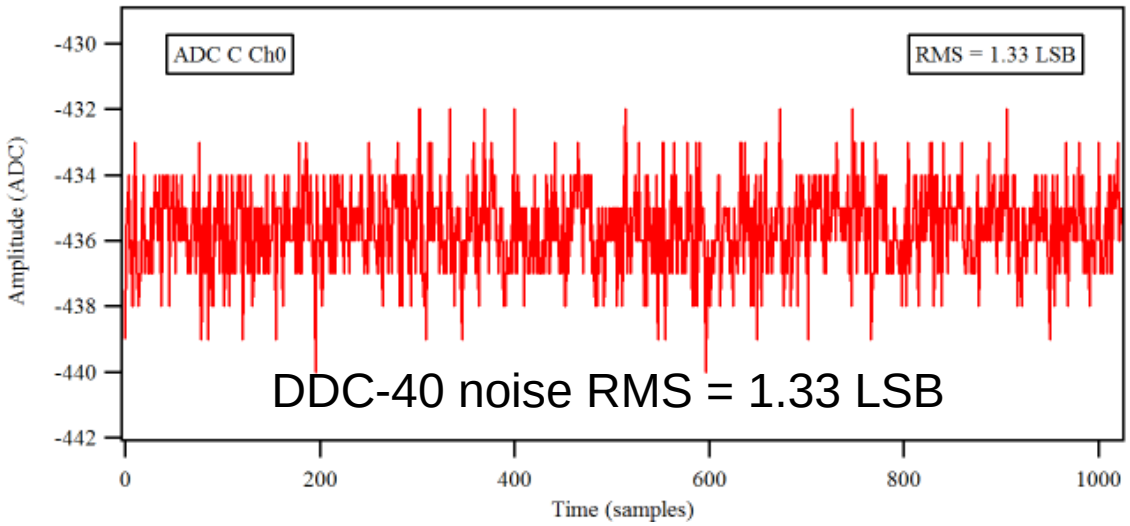
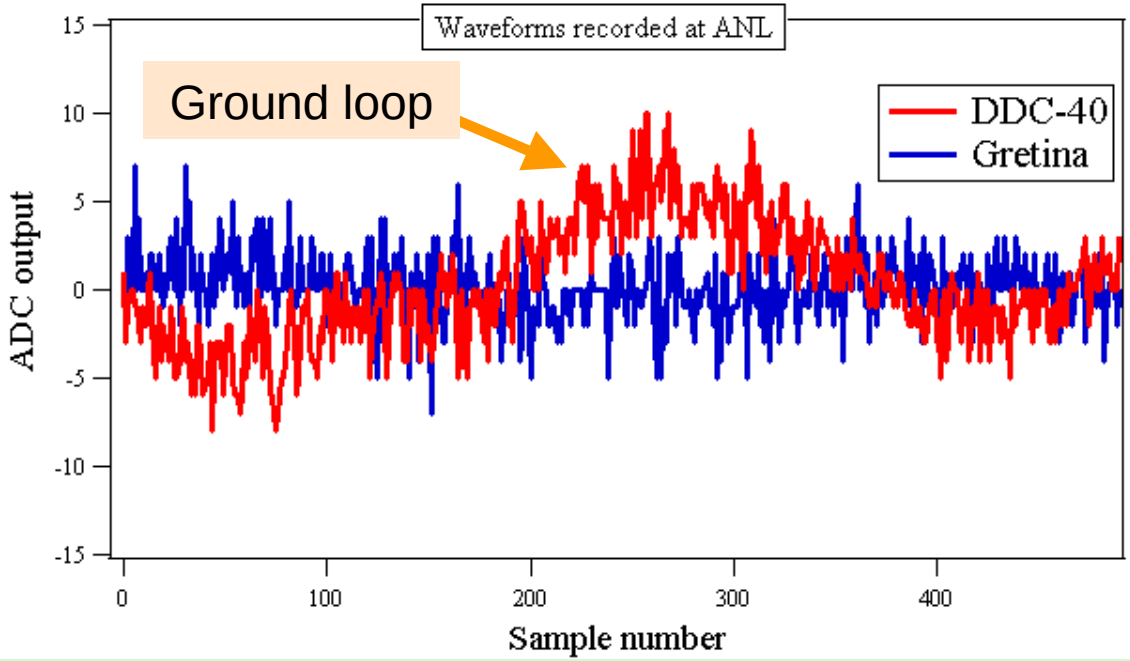
Noise in Rochester and at ANL

DDC-40 free run waveform in Rochester





DDC-40 in Rochester
Noise RMS = 1.33 LSB

The DDC-40 and the Gretina digitizer in the ANL Test Setup.

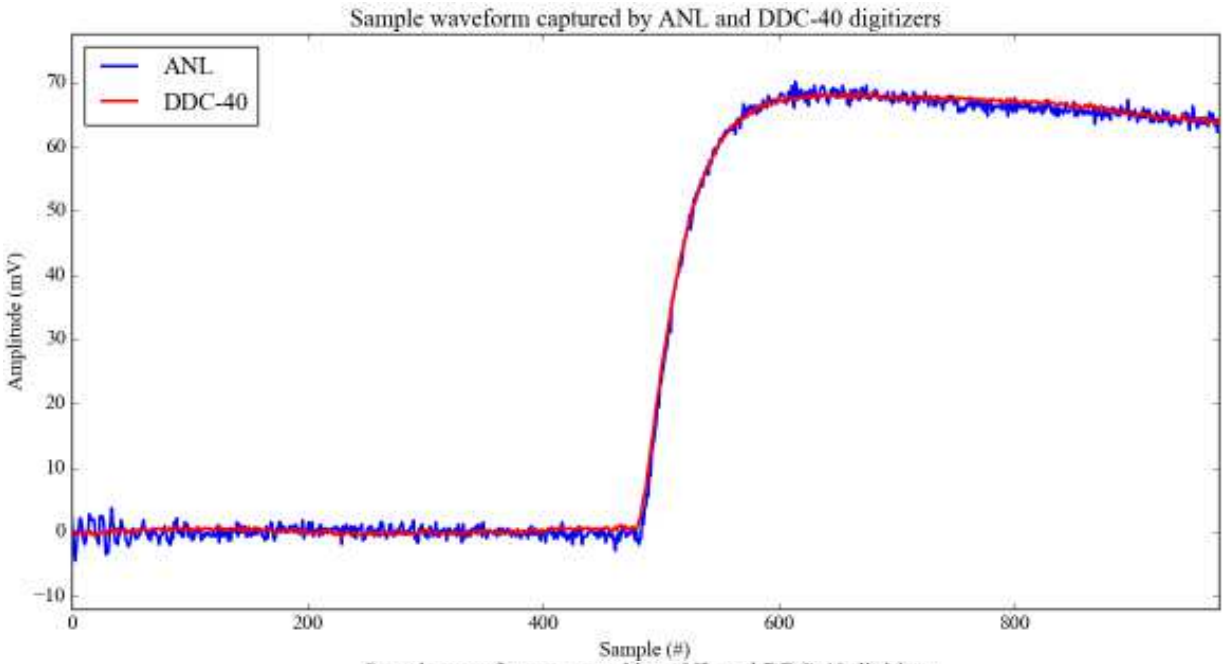
Blue: Signal source and reception in the same backplane.

Red: Signal source and reception in two separate backplanes.

The periodic noise was due to a ground loop.

We were able to suppress the pickup noise using a digital filter.

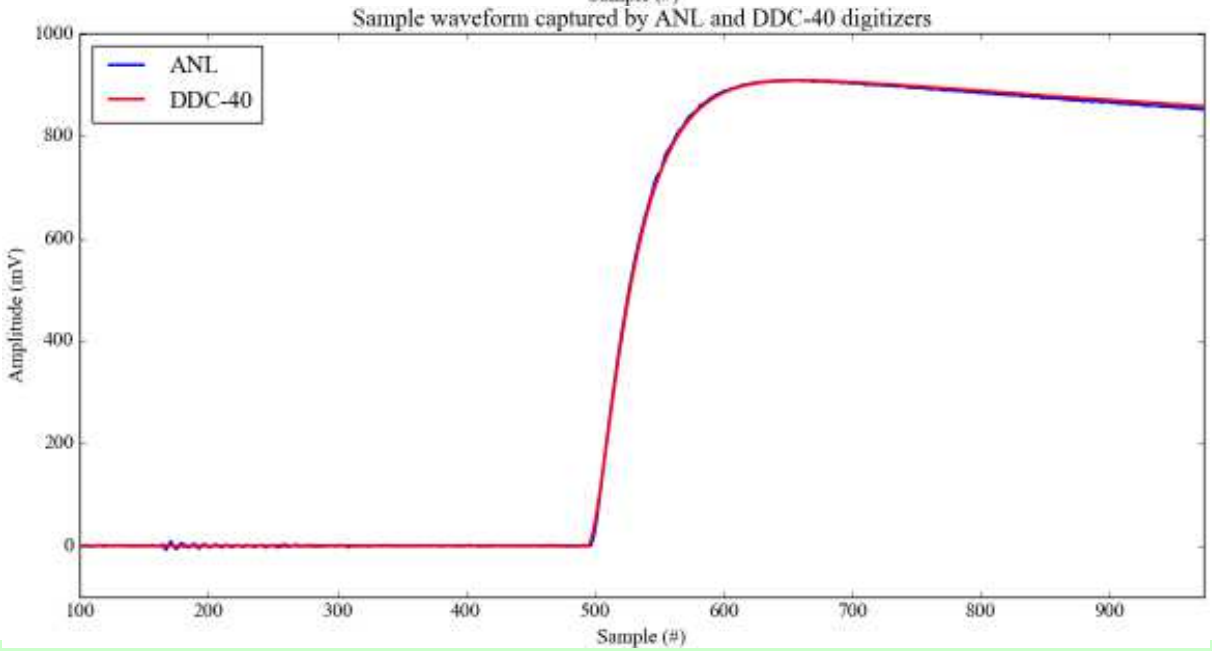
Pulse Responses of the DDC-40 and Gretina Digitizer



The pulses from the Digitizer Tester had nominal 300 ns rise and 50 μs fall.

Small pulse responses normalized to the same pulse height

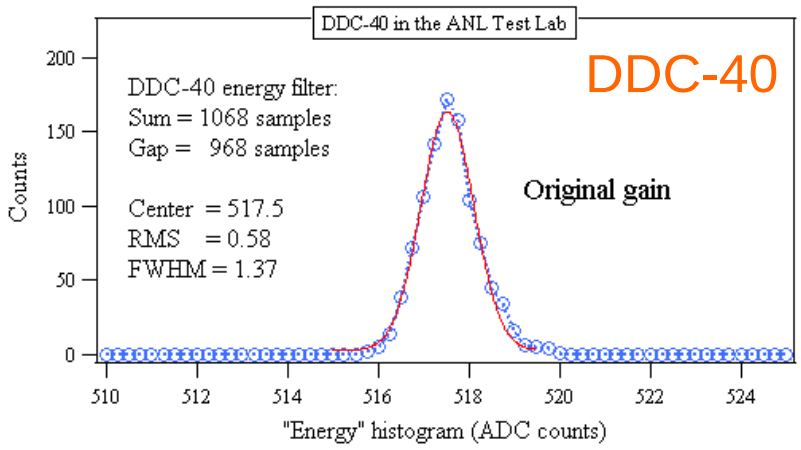
The nominal input ranges of the DDC-40 and the Gretina digitizer differ 2x, so we normalized the pulse heights to make them match in this figure.

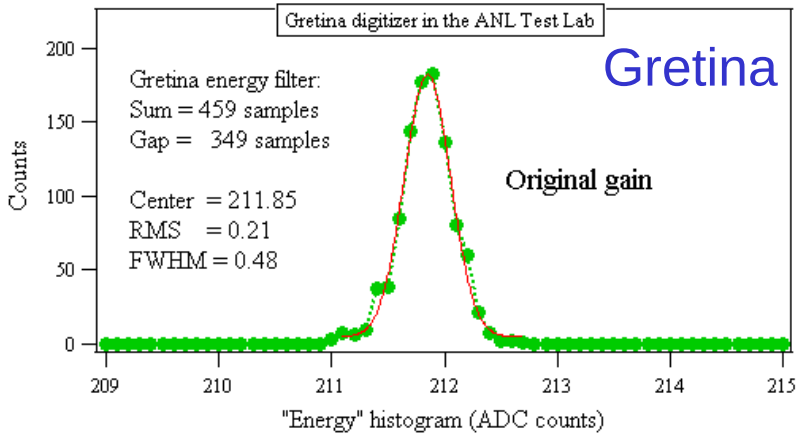


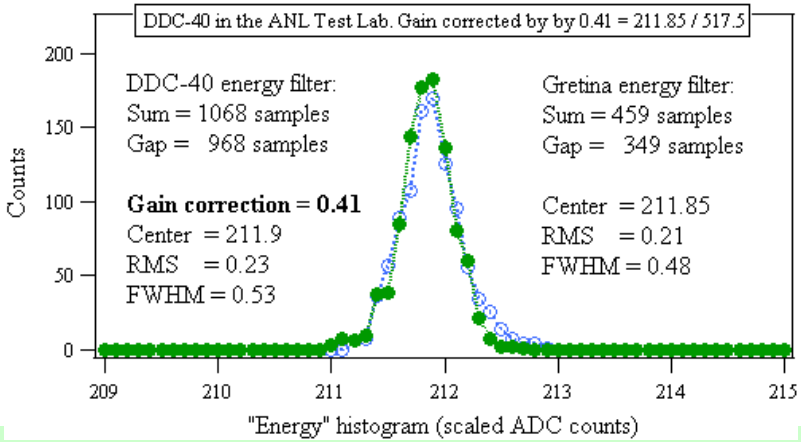
Large pulse responses normalized to the same pulse height

Noise pickup did not affect the DDC-40 pulse response

DDC-40 Matched the Gretina Digitizer Resolution







DDC-40 after digital suppression of the periodic pickup noise.

DDC-40 gain was higher by 2.44 than the Gretina digitizer gain (nominally two times higher). The periodic pickup noise was minimized with a digital filter tuned to the frequency of the periodic noise.

Gretina digitizer in the ANL Test Setup.

Gretina digitizer gain was lower by 2.44 than the DDC-40 gain (nominally two times). The coefficient was determined from fitting the centroids, shown on the left.

Comparing the Gretina and the DDC-40 digitizers in the ANL Test Setup: **THEY MATCH!**

DDC-40 gain was corrected down by 0.41 to match the Gretina digitizer gain (nominally 0.5). The periodic pickup noise was minimized with a digital filter.

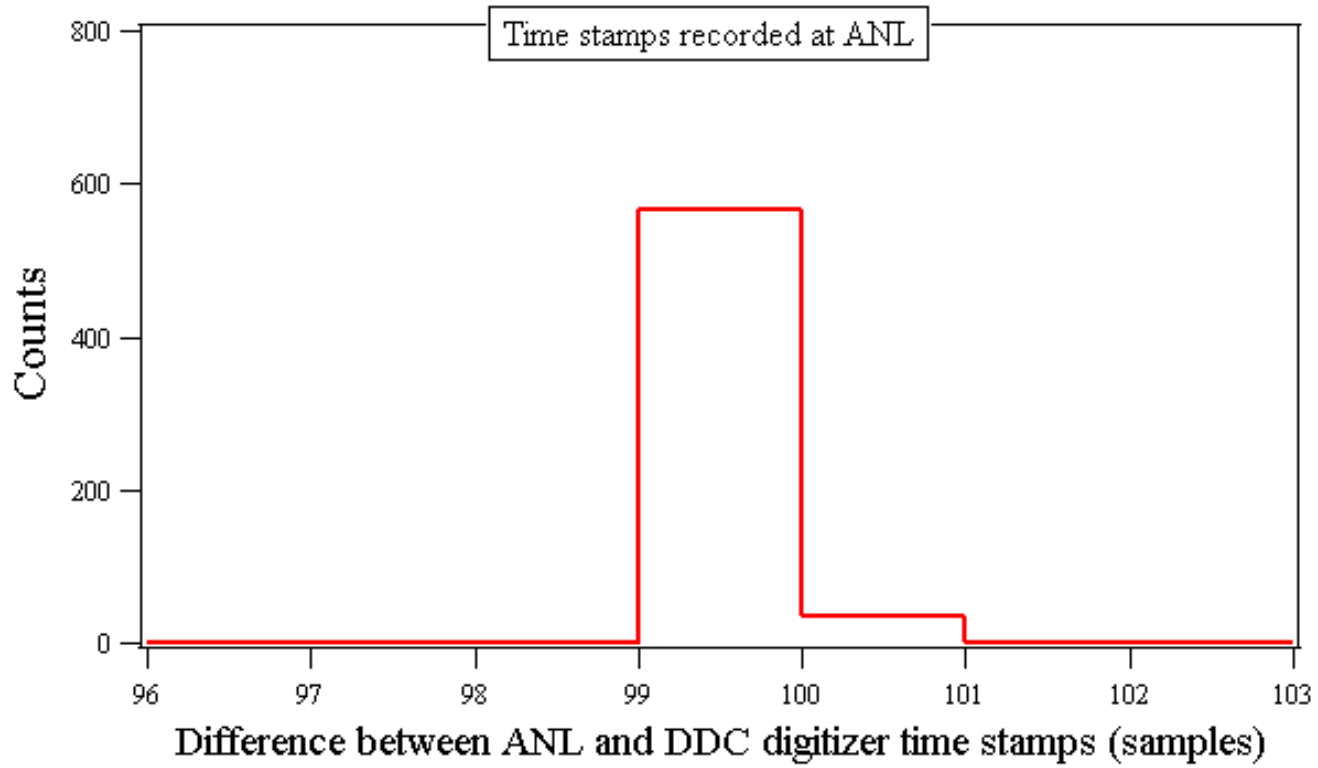
Both digitizers achieved equivalent energy resolutions!

Time Stamping @ ANL

Both digitizers recorded the Time Stamps within ~one clock jitter from each other.

Waveforms could be precisely correlated between the digitizers, using the TS.

Time Stamp difference between the DDC-40 and the Gretina digitizers



Summary of Technical Achievements

- Five 10-channel units were built and tested. Two units were already shipped to a customer.
- We continue the firmware and software development using the remaining three units.
- We upgraded the Trigger/Logic Module to ARM and Kintex-7.
- 40-channel digitizer has been developed. Two units (80 channels) were built and tested.
- We tested one of the 40-channel units in parallel with the Gretina digitizer at ANL.
  - DDC-40 was operated using an embedded Jupyter interface. (I.e., iPython.)
  - ADC clock distribution, time stamping, and triggering were shared between the DDC-40 and Gretina digitizers.
  - Both digitizers wrote separate, but coordinated binary data files.
  - Event time stamping was accurate to 10 ns between the DDC-40 and Gretina digitizers.
  - We achieved equivalent pulse height resolutions of the DDC-40 and Gretina digitizers, after a digital suppression of the periodic noise pickup.
- We used the DDC-40 know-how to design an LZ digitizer with 32 channels (separate funding).
- The LZ DAQ electronics will be delivered to LZ this Fall (87 boards).

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Future Plans

- Continue development of firmware and software for both digitizers (10 and 40 channel).
- Develop complete systems of many digitizers managed by Trigger Modules.
- A complete small system will be tested at ANL: two digitizers + Trigger / Logic Module. (Planned for this Fall.)
  - This multi-digitizer DAQ system will be interfaced with the ANL DAQ framework (triggering, clock distribution, time stamping).
- **Develop protocols and interfaces compatible with the ANL infrastructure**.
  - We were awarded a Phase I grant for these developments.
  - Successful integration with the ANL infrastructure will pave the way to FRIB.
- SkuTek participates in the FRIB DAQ Working Group spearheaded by Robert Varner (ORNL). The Workgroup is developing guidelines for the community-wide DAQ interfaces and protocols.

  https://www.phy.ornl.gov/fribdaq/
  - SkuTek will eventually use the FRIB DAQ Working Group guidelines in our products.
  - Meanwhile we will follow the de-facto interfaces and protocols developed at ANL.

Questions for the NP Community

- The community needs to provide a set of guidelines and technical standards for the inter-DAQ communication and synchronization.
- Can the community specify how to tie together separate DAQ systems?
- How to exchange trigger, validation, time stamps, and other control signals?
  - This work is ongoing: https://www.phy.ornl.gov/fribdaq/
- Meanwhile we will follow the de-facto interfaces and protocols developed at ANL.

Acknowledgements

Joanna Klima, Sean Fallon, Gregory Kick, David Miller,
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Eryk Druszkiewicz, Frank Wolfs

John Anderson and Michael Carpenter were our hosts @ ANL

Special thanks to Michelle Shinn and Manouchehr Farkhondeh

Backup slides

Kintex-7 improves the performance of our products

Kintex-7: more logic, more memory

- Spartan-6 was the best tradeoff between price and performance circa five years ago.
- The new Series-7 FPGAs now offers more digital resources at a reasonable cost.

Feature	XC3S5000 Spartan-3 a)	XC6SLX150 Spartan-6 b)	XC7K325T Kintex-7 c)	XC7K410T Kintex-7 c)	Relative to XC3S5000
Equivalent logic cells from Data Sheet	74,880	147,443	326,080	406,720	2.0 / 4.4 / **5.4**
Multiply-accumulate units	104 d)	180	840	1540	1.7 / 8.1 / **14.8**
Waveform memory (k samples) e)	104 k	268 k	890 k	1,590 k	2.6 / 8.6 / **15.3**
Balls per package	900	900	900	900	same
I/O pins	633	576	500	500	0.9 / 0.8 / 0.8
Price lowest speed grade (900 balls)	$166	$210	$1,032	$1,496	1.3 / 6.2 / 9.0
Price “our” speed grade (900 balls)	$191	$210	$1,550	$1,796	1.1 / 8.1 / 9.4
$$ per channel for 32+ channels f)	$5	$5	$40	$45	

a) XC3S5000 is used in present GRETINA digitizers. It is the community’s performance yardstick.

b) XC6SLX150 was used in our previous 10-channel and 32-channel digitizers.

c) These pin compatible Kintex-7 chips will be used in our high density digitizers (40 channels).

d) XC3S5000 provides multipliers without the built-in accumulate register.

e) Total number of block RAM bits divided by 18. Parity bits are considered not useful for waveform storage.

f) Approximate FPGA cost per channel for 32+ channels.