

DE-SC0023557

High Channel Density Digital Data Acquisition System

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SBIR Exchange, July 29, 2025 2:40pm



- The company and its capabilities.
 - Customers.
- High channel density DAQ.
- Progress.
- Outreach projects.
- Future plans.
- Acknowledgements.

The company and its capabilities

- The team: four physicists / engineers, a junior research engineer, a senior software engineer, engineering associate, a part time physicist, and a manager. We regularly work with a local Electrical Engineering consultant.
- We worked with interns listed on the Acknowledgements page.

Our focus:

Digital data acquisition (DAQ) for nuclear physics, high energy physics, astrophysics, etc.

Our capabilities: End-to-end development of electronic instruments for Nuclear Physics.

- Electronic design. We can *collaborate* with researchers across the field with board design.
- Firmware development for Field Programmable Gate Arrays (FPGA).
- Software development for embedded processors, either hard silicon or soft cores.
- NP algorithm implementation in FPGAs and in embedded processors.
- Processing data from nuclear detectors of any kind.
- Development of detector assemblies using scintillators, PMTs, PIN diodes, or SiPMs.

Our customers



Los Alamos National Laboratory



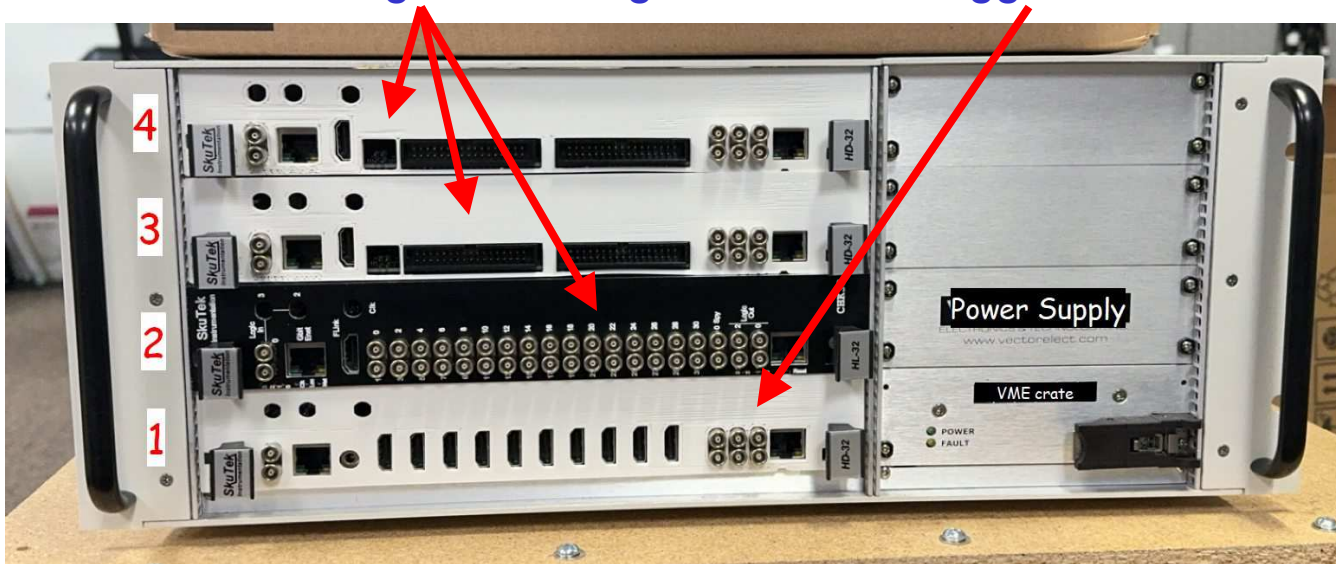
Brown
University



High Channel Density Digital Data Acquisition System

- The solicitation topic C55-22 is calling for development of high channel density (with ≥ 256 channels) digital data acquisition with ≥ 100 MSPS, ≥ 12 bit ADC information per channel.
- We proposed a modular system. Channels can be added in multiple of 32. All boards are controlled with embedded Linux, one Linux per board. The boards are either independent, or connected to Trigger Master.
 1. *Trigger Logic Master* serving up to 10 digitizers (up to 320 channels). Masters can be cascaded.
 2. *32-channel digitizer* with **LEMO** inputs for high resolution detectors.
 3. *32-channel digitizer* with **FERA** inputs. FERA inputs were suggested by ANL for silicon strip detectors.

Multi digitizer configuration with Trigger Master.



Single digitizer configuration.



32-Channel Digitizer With **FERA** Inputs and On-Board Calibration

NIM in 0,1

1G Ethernet

Fast LVDS Link to Master

Channels 0..15

Bias voltage
and +5V for
channels 0..15

Channels 16..31

Bias voltage
and +5V for
channels 16..31

Analog out 0,1

NIM out 0..3

Linux Ethernet

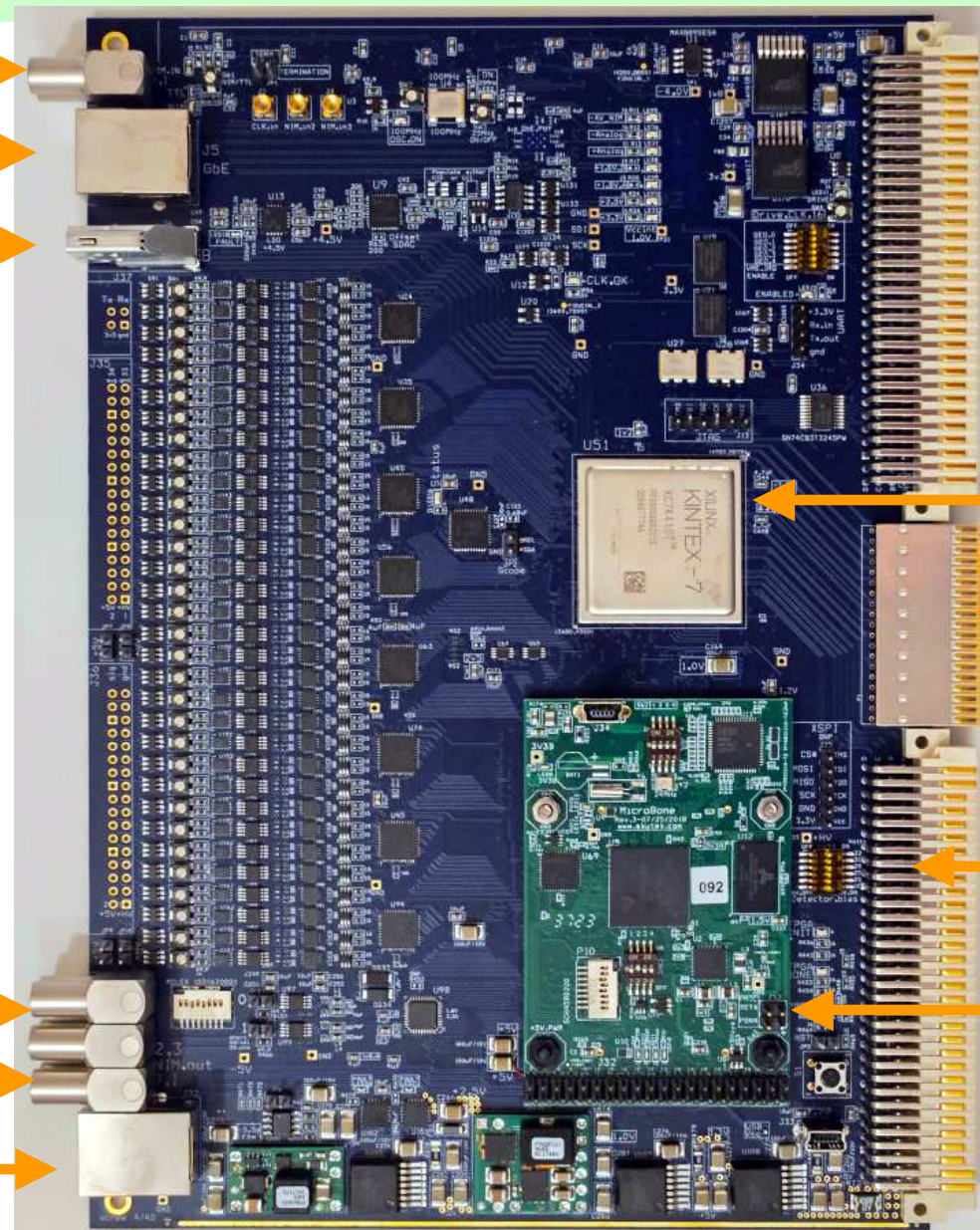
- On - board calibration with 16-bit voltage DAC

FPGA XC7K410T
with 3,180 kilobytes of RAM

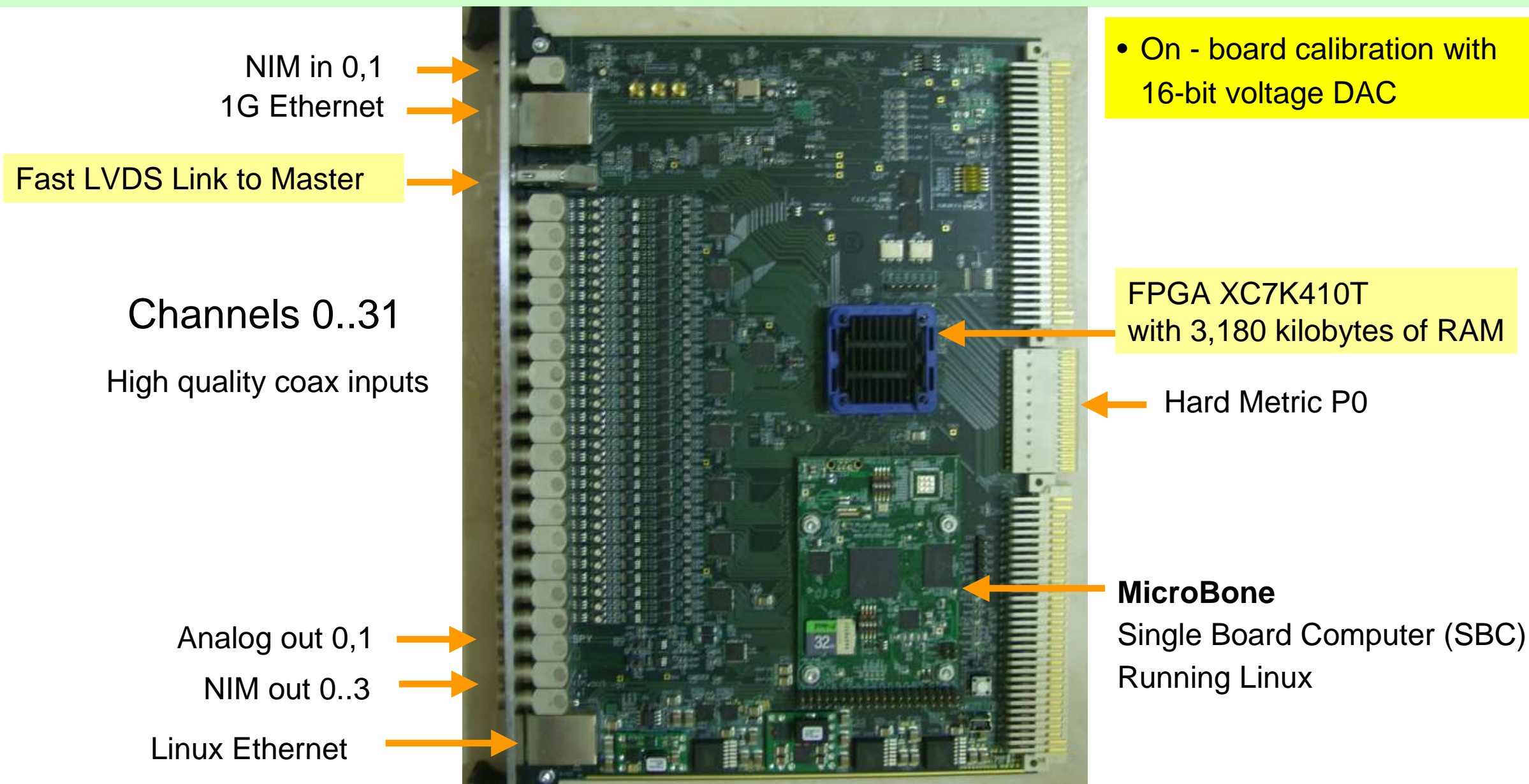
Hard Metric P0

Bias voltage
selection
in 6 steps
10..32 volts

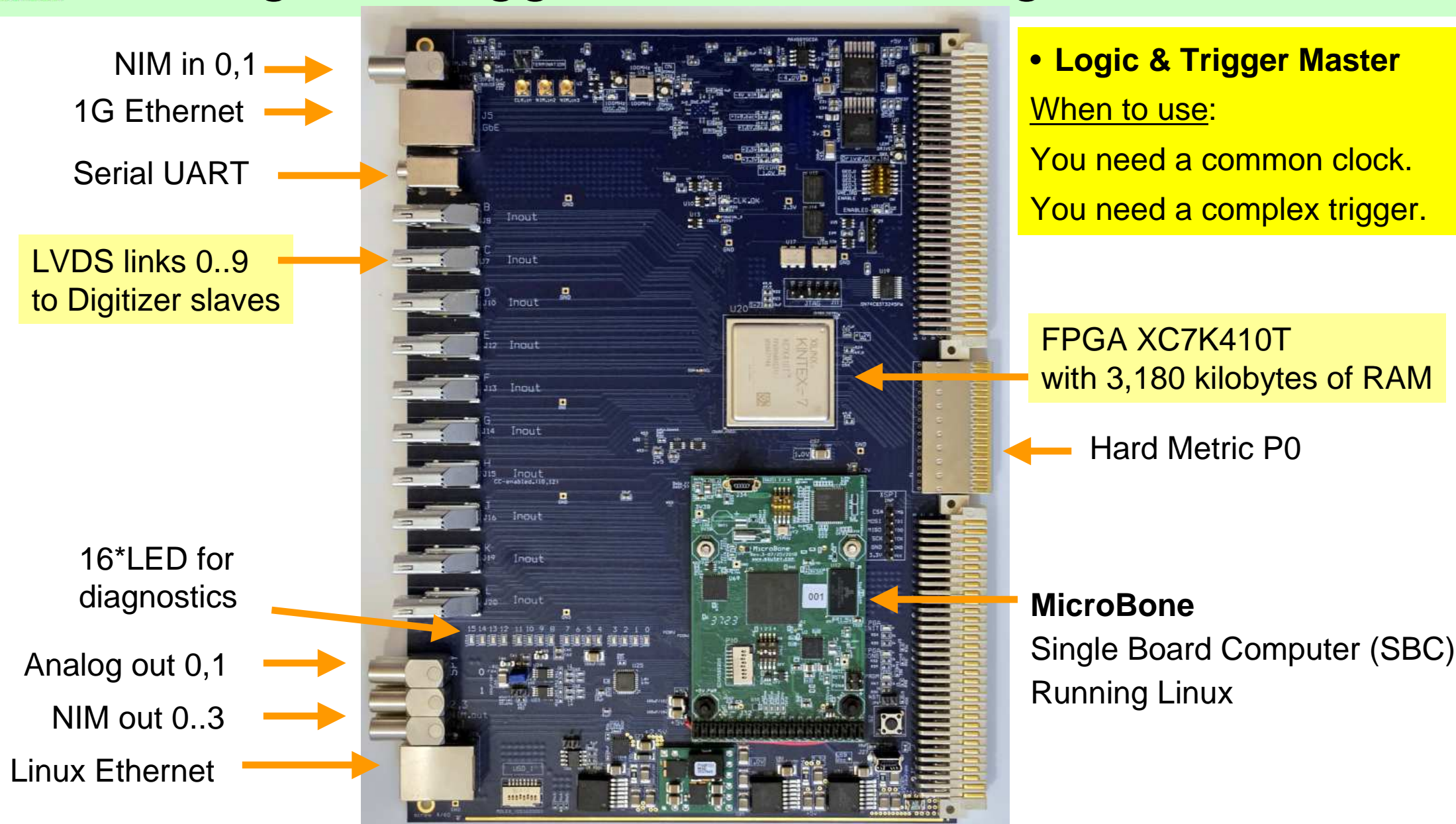
MicroBone
Single Board Computer (SBC)
Running Linux



32-Channel Digitizer With **LEMO** Inputs and On-Board Calibration

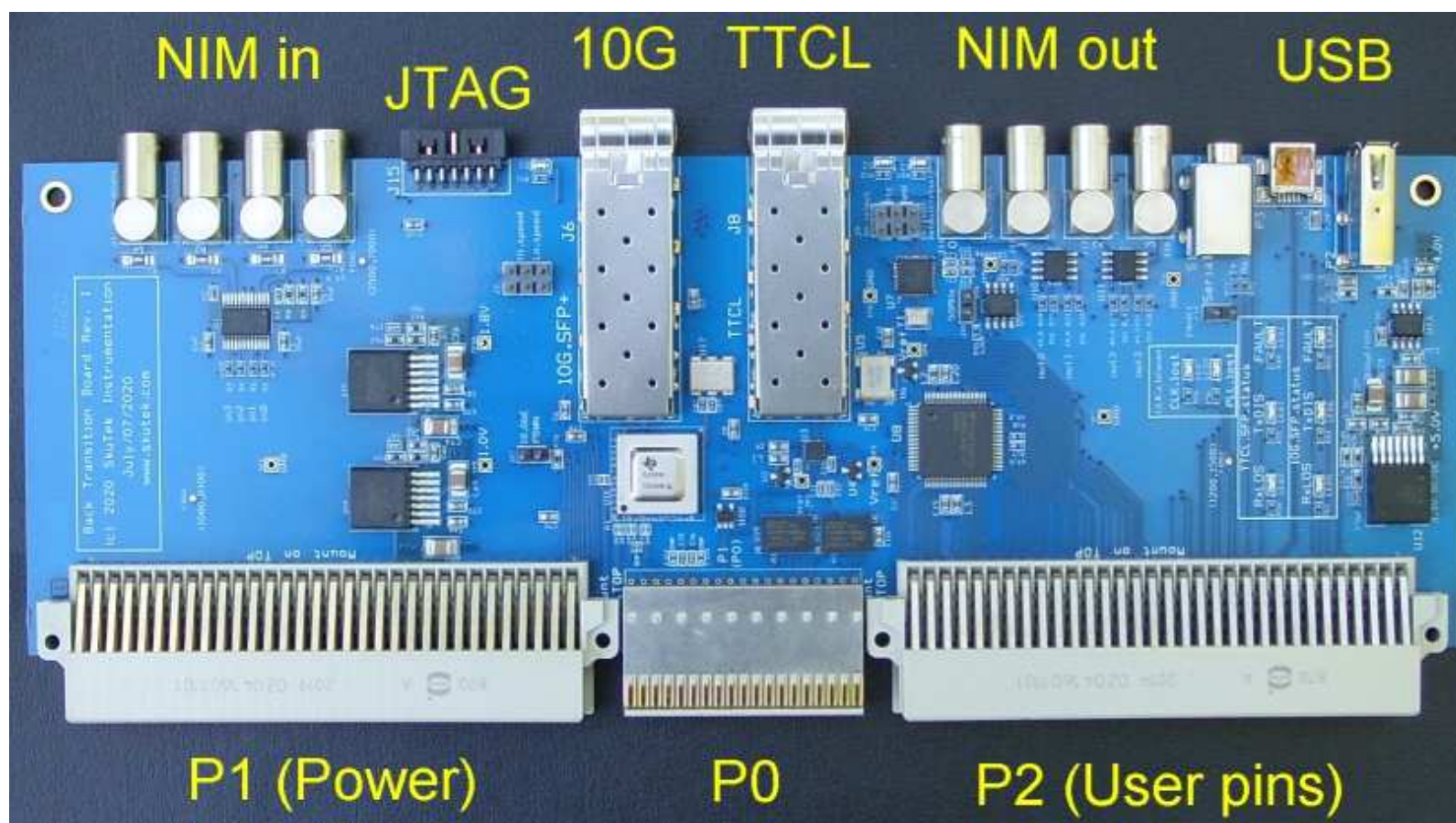


Logic & Trigger Master for Large Scale DAQ



High Speed 10G Streaming Rear Transition Module (RTM)

- RTM will provide system integration with Nuclear Physics framework.
- High speed 10G data streaming with GRETA-compatible binary format.
- White Rabbit (WR) support is under development (being tested at FRIB).



- **Optional Streaming RTM.**
Can be added to any our board.
When to use:
You need 10G streaming output from every board.

Digitizer Ecosystem: Data Streaming and Management

Developed under DE-SC0021502

Each Digitizer can stream data at up to 10G, using the Rear Transition Module

1 Digitizer = 10 G = 1.2 GB/s ~ **140K** waveforms per second

4 Digitizers = 40 G = 5 GB/s ~ **700K** waveforms per second

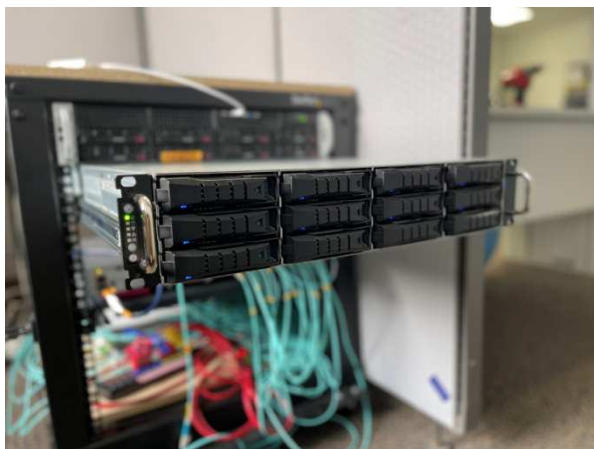
10 Digitizers = 100 G = 12 GB/s ~ **1.4M** waveforms per second

**Assuming 4096 Samples per waveform*

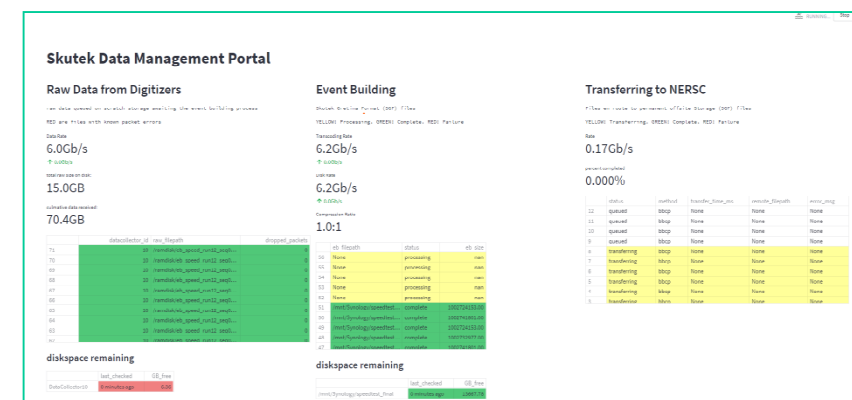
When to use:

You need 10G streaming outputs
generating **lots of** data.

Our Data Management Solutions will receive the streams and
transfer your data to NERSC or another supercomputing center



Data Collector servers receive event streams and convert them to files



A Web-based Interface will let you monitor
your data as it's collected, processed, and
transferred to NERSC

Very Low Noise and Excellent Pulse Response

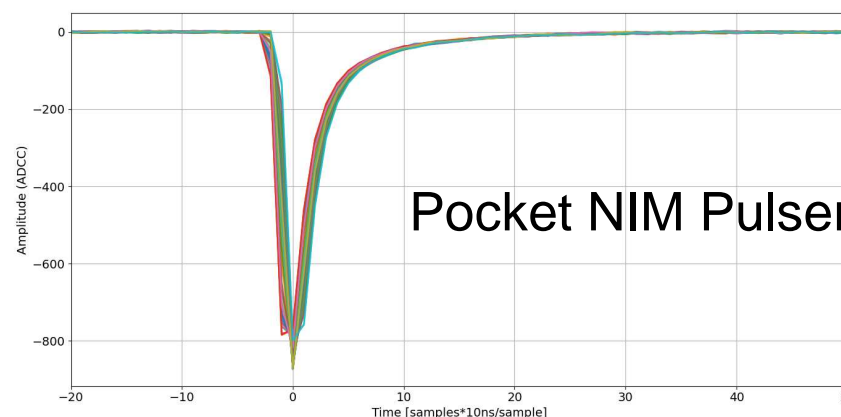
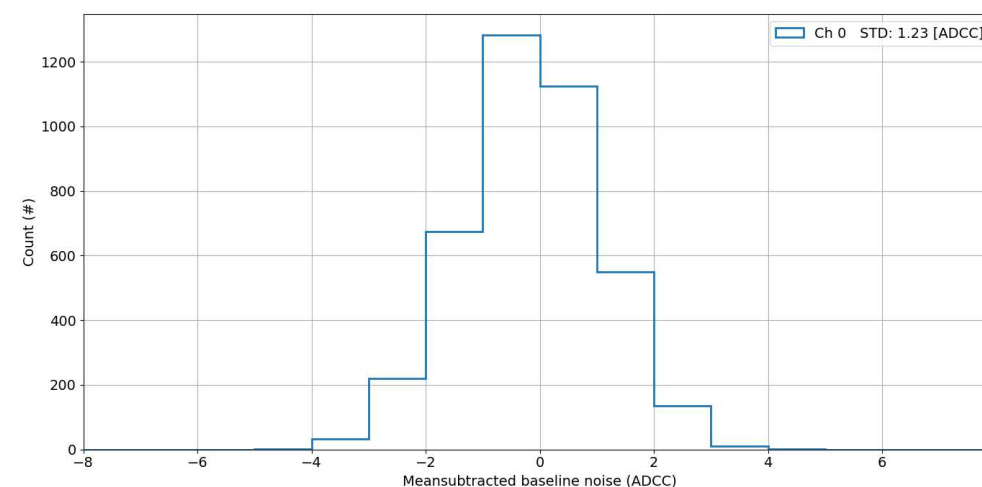
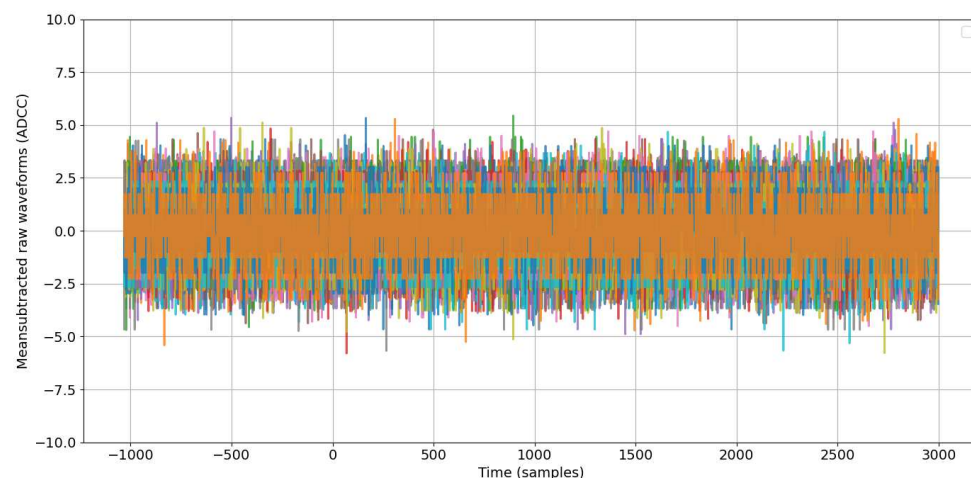
- Signal range = 2 volts, digitized with 14 bits @ 100 MSPS.

ADC noise RMS = 1 LSB from the datasheet

Noise RMS = **1.23** LSB = 150 μV

1 LSB = 2 V / 16k = 122 μV

Noise waveforms from all 32 channels



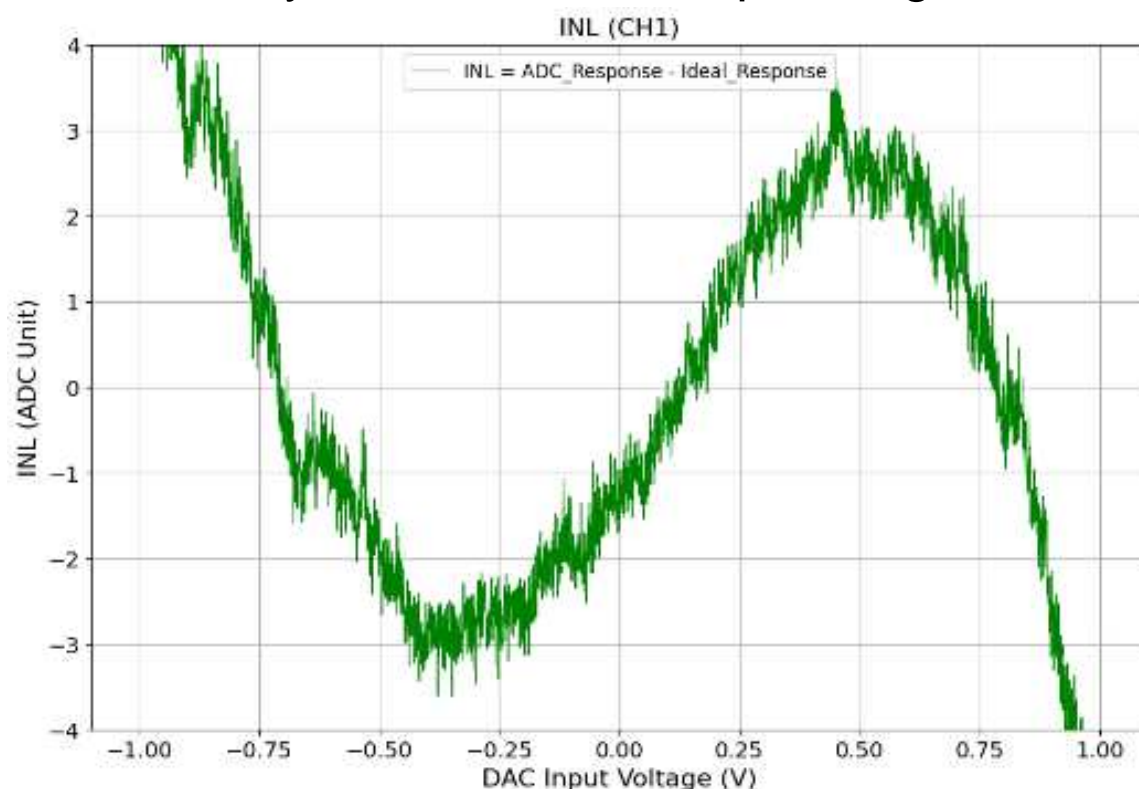
Pocket NIM Pulser (~10 ns pulse, similar to PMT)

On-board Nonlinearity Measurement With 16-bit DAC

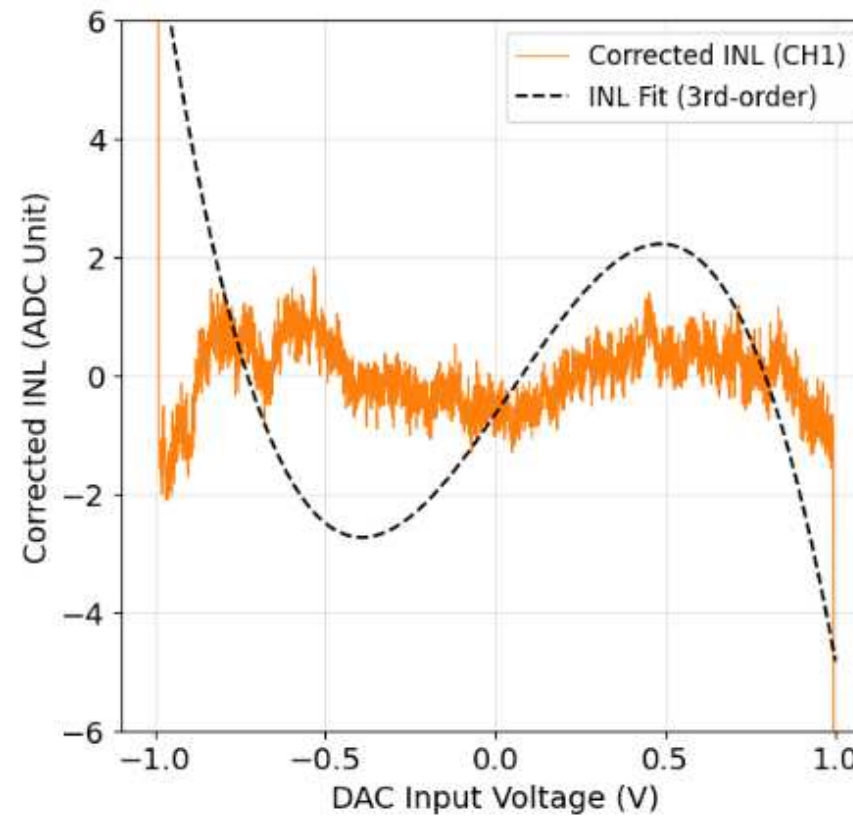
Originally developed under DE-SC0020500 and adopted to the current project.

Sampling ADCs are quite nonlinear. We need to measure the INL, and correct if necessary.

Nonlinearity measured over input range = 2 volts.



Offline nonlinearity correction.



Status of the Digitizer Firmware

- In collaboration with ANL, we ported the DSP core from the 10-channel GRETINA / DGS digitizer.
- The core was geared towards high resolution HPGe and their BGO Compton shields.
 - We worked with John Anderson and Michael Oberling, DE-SC0018467.
- We then redesigned the core to serve a wider variety of detectors. We added a few subsystems:
 1. *General Purpose Memory Controller* (GPMC) interfaced to our MicroBone Single Board Computer (SBC) which is used for setting up and monitoring the digitizer operation.
 2. *Data Streaming Engine*: The Parallel Channel Packer (PCP) between the DSP stage and the UDP Streamer. PCP cycles through all channels sequentially (0→31→0) during UDP transfer.
 3. *UDP Streamer* accepts data buffers from the PCP and funnels them to the UDP endpoint.

Subsystem #1 is interfaced and controlled via Linux. Subsystems #2 and #3 are independent of Linux.

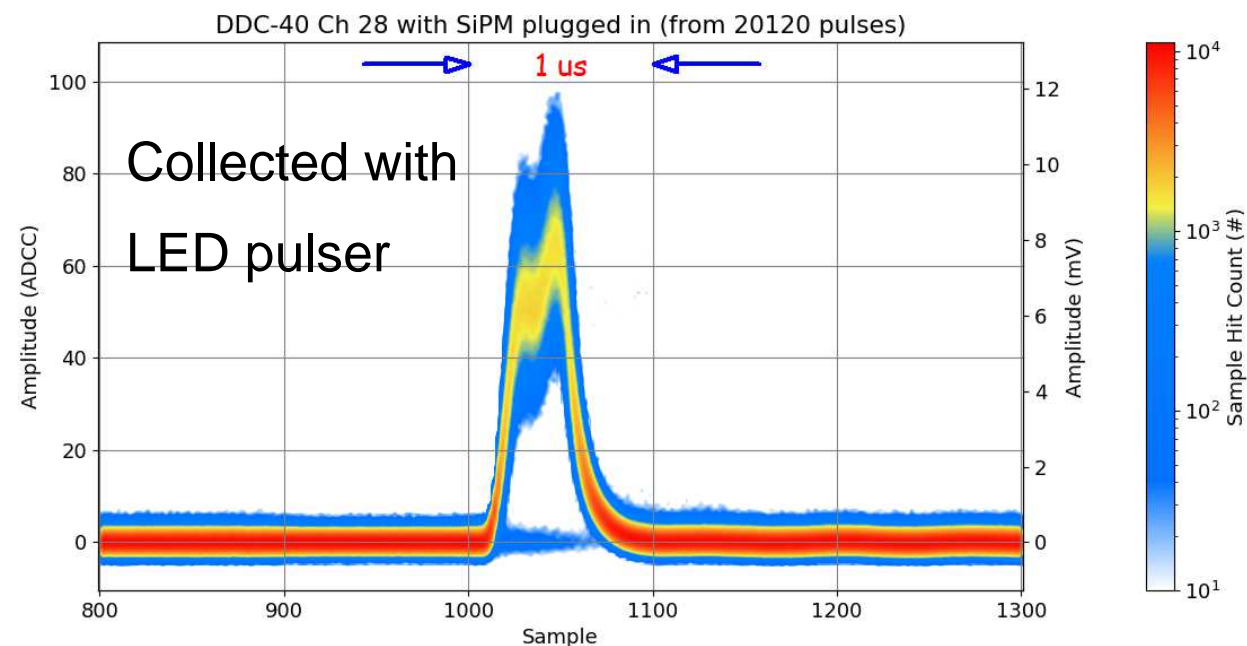
Status: We wrote the VHDL code. We are now working on integration.

- We developed the *software control framework* based on the REST interface.
 - Representational State Transfer (REST) is a method for sending commands using HTTP.
 - REST is popular in the research community. E.g. both NERSC and GRETA adopted REST.
- Hardware Abstraction Layer (HAL) translates between REST commands and FPGA registers.
 - HAL is a library of low level utility functions.
- We are developing programmatic control of the firmware (not through a graphical interface).
 - Requested by FRIB.
 - C utilities, Python scripts, Jupyter.
 - We released our C utility library to the public.
- **Status**: We wrote the code. We are now using it to control the digitizers.

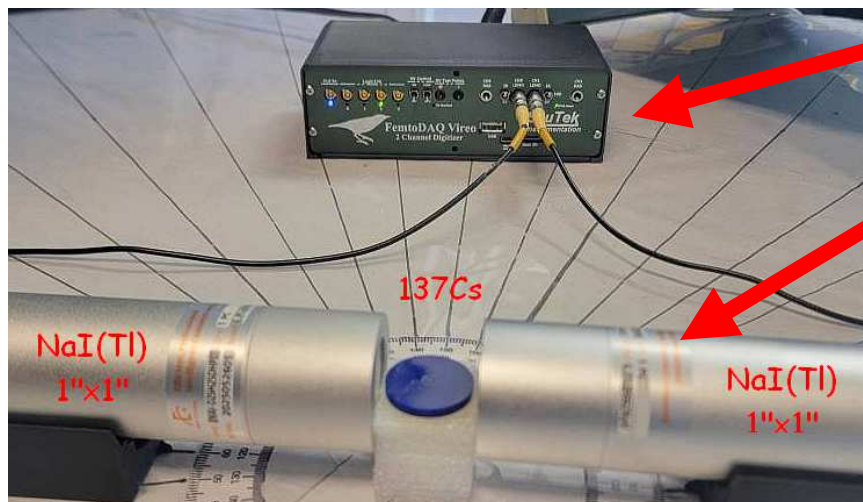
- **What we have done.**
 - We have advanced the digitizer firmware.
 - The DSP core and the Parallel Channel Packer are brand new.
 - We advanced the software drivers for these cores.
- **Remaining work.**
 - Finalize and test the digitizer firmware.
 - Firmware for the *Trigger Logic Master*: multiplicity trigger, bit pattern trigger, other triggers.
 - Integration and testing of the Digitizers with the Trigger Logic Master.
 - Integrate with our own ecosystem: data collection, data storage, and data management.
- **Make the community aware.**
 - We need to make the NP community aware of our products and solutions.
 - Outreach and support. It is actually a lot of fun.

- Real-time DAQ trigger on the neutrino signal from galactic core-collapse supernovae (SN).
 - Waiting for the Betelgeuse to become a supernova...
 - M. Elise McCarthy, Dept. of Physics and Astronomy, University of Rochester
- Muon capture and decay experiment in Advanced Nuclear Science Education Laboratory (ANSEL).
 - Frank Wolfs and Eryk Druszkiewicz, Dept. of Physics and Astronomy, University of Rochester
- Precise timing with White Rabbit and GPS at FRIB.
 - Giordano Cerizza and Aaron Chester, FRIB.
- R&D on an ASIC for the LEGEND experiment and R&D of a graphene field effect amplifier.
 - Alan Poon and Lisa Schlueter, LBNL.
- SiPM detector project at LBNL with 40-channel Firebird.
 - Aaron Manalaysay, LBNL.
- Using EjFAT for fast data transfer.
 - Ilya Baldin, Yatish Kumar, Stacey Sheldon, and Derek Howard, Jefferson Lab.

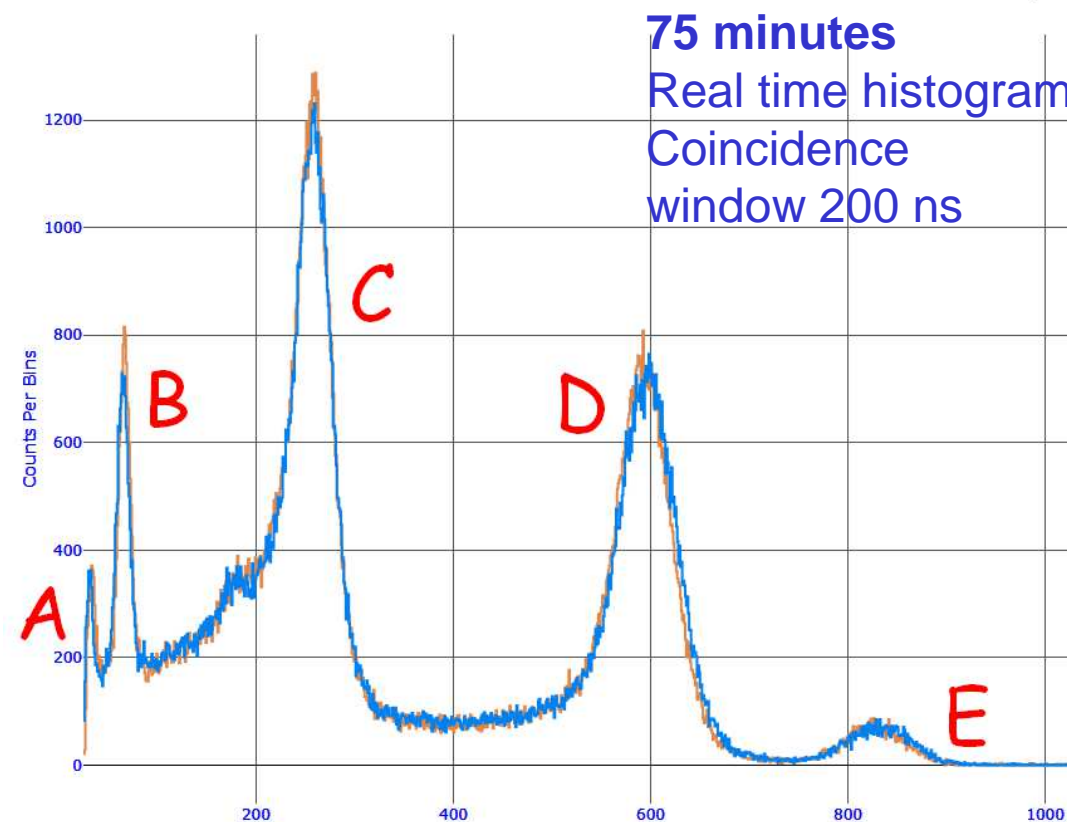
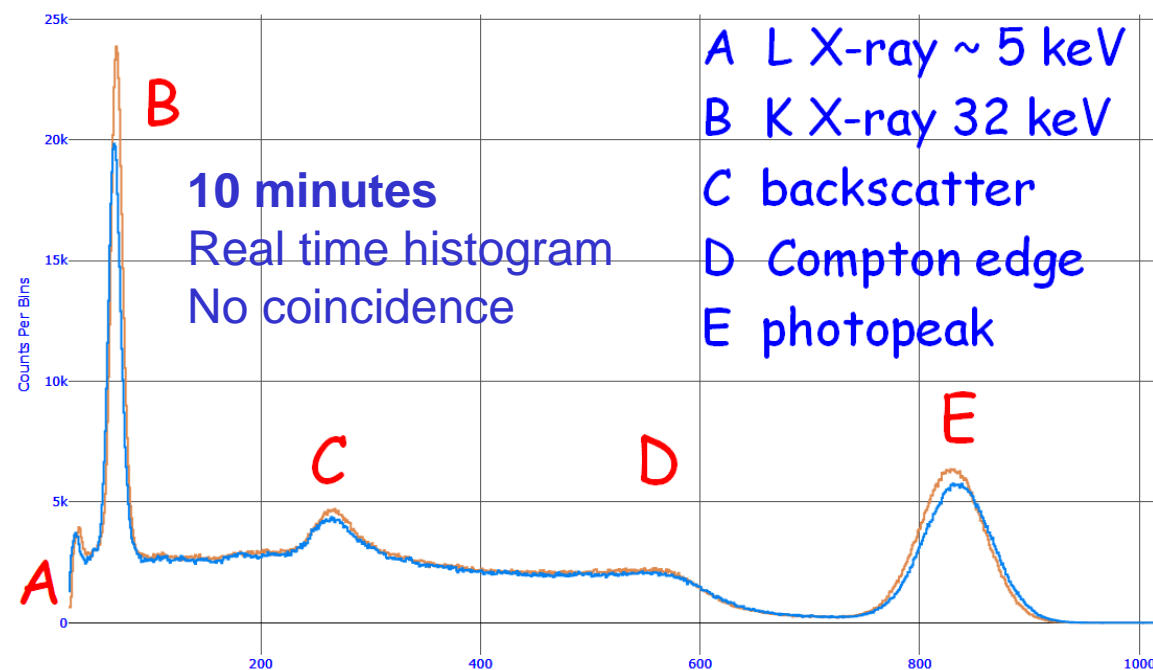
Aaron Manalaysay, Principal Investigator, LBNL. Working with Eryk Druszkiewicz.



Example: Real Time Coincidence Measurement With Digital Instrument



- 2-channel Vireo, 14 bits @ 100 MHz, on-board Linux
- On-board coincidence firmware. NIM not needed!
- Two detectors, NaI(Tl) 1"x1" with built in HV and preamps
- Real time histograms with ^{137}Cs , 5 μCi , single γ photon.
- Coincidence with a single photon??



Future Plans

- Implement user - friendly and developer - friendly control interfaces for the DAQ.
- Add features requested by the community.
 - E.g., support for the White Rabbit clock was requested by FRIB. We have implemented it.
- Work out integration of multiple Digitizers and Trigger Logic Masters into a coherent DAQ.
- Gain visibility and brand recognition in Nuclear Physics, HEP, and other branches of physics.
 - Optimize the digitizer hardware, firmware, and software for best user experience.
 - Support valuable research and educational projects with our devices.
 - Advertise the entry-level 2-channel units for education.
 - Develop exciting demonstrations and applications like the one we have shown.
 - Enjoy what we are doing.
- Keep developing expertise within the team.
- Keep working with interns.

Joanna Klima, Jackson Hebel, Jeffrey Maggio, JianCong Zeng,
Hugh Gallo, Edmond Tan, David Miller, James Vitkus, WS



Consultant: Eryk Druszkiewicz

Interns and coop students:

Ujval Madhu, Solomon Shulman

Special thanks to Manouchehr Farkhondeh and Michelle Shinn

This work was supported by the DOE Office of Science, Office of Nuclear Physics under the SBIR grant DE-SC0023557