VERTICALLY INTEGRATED TIMING READOUT CHIP (VTROC):
An Advanced, Small Pitch, Low Power Solution For Nuclear Physics Applications

Contract # DE-SC0022479 | 2024 SBIR/STTR Exchange Meeting
Period of performance: 04/03/2023 - 04/02/2025
TPOC: Dr. Michelle Shinn

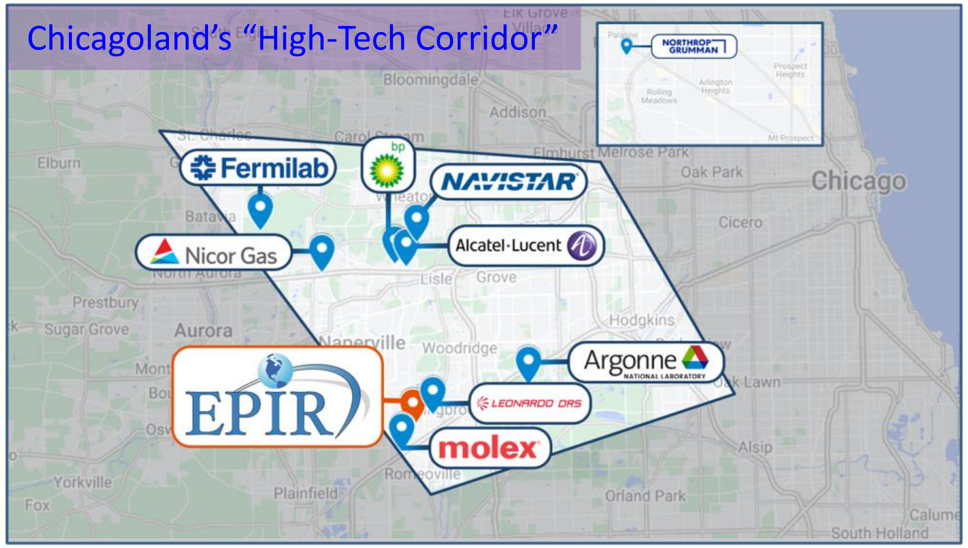
- **EPIR, Inc. Team:** Dr. Sushant Sonde (PI), Dr. Silviu Velicu (PM), Dr. Yong Chang
- **Fermilab Team:** Dr. Tiehui Ted Liu

July 29, 2025

OUTLINE

- Introduction
  - Company overview
- Background
  - DOE's requirements
  - EPIR Inc.'s proposed approach
- Programmatic
  - Program Objectives
  - Updates on technical tasks
    - ASIC design effort
    - Multi-tier integration effort
    - Testing and validation results
- Summary & Outlook

COMPANY OVERVIEW



Headquartered in Bolingbrook, IL

- Commercial supplier of MBE materials and devices to a broad customer base
- Provider of material, focal plane arrays, and sensors solutions

II-VI Material Manufacturing

- Grow II-VI materials to enable standard and custom imaging products
- HgCdTe on CdZnTe and Si-based substrates

Focal Plane Arrays (FPAs) Development & Production

- Standard and specialty array detectors, FPAs, and sensors
- Modeling, optimization, fabrication and testing

R&D Solutions using II-VI Technology

- Full process development to meet customer specifications
- Advanced interconnect solutions for pixel detectors

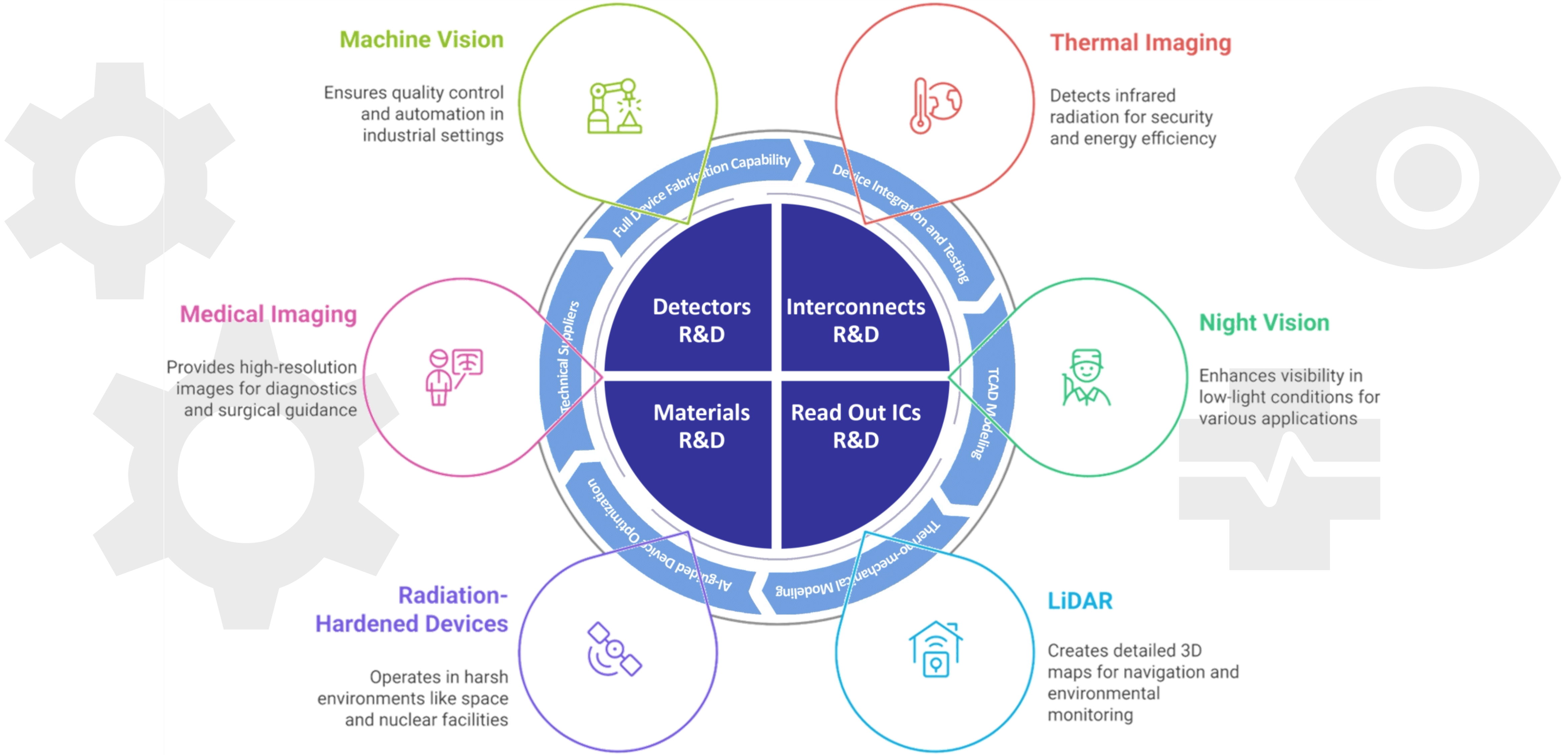
Contact US

- 586 Territorial Drive Ste A, Bolingbrook, IL 60440
- ssonde@epirinc.com
- 512-905-9885

- Cutting-edge sensor technology development with leading US imaging companies and federal agencies.

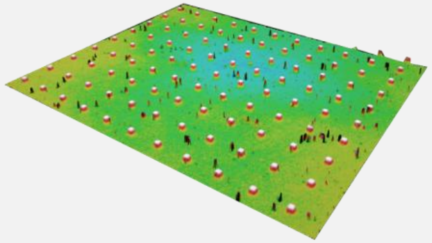
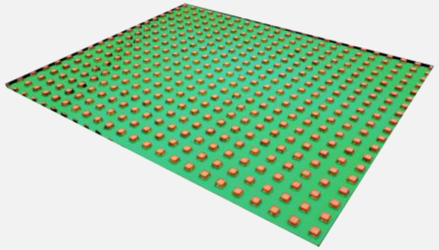
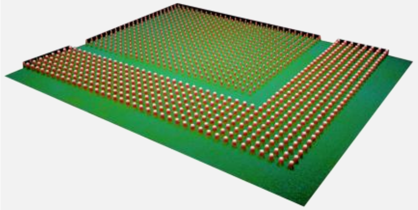
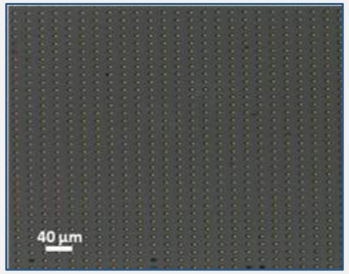
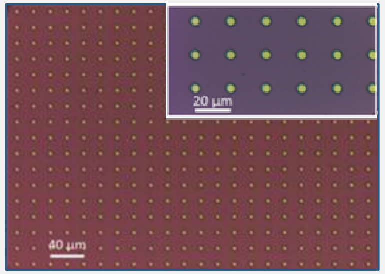
COMPANY OVERVIEW

EPIR'S TECHNICAL INFRASTRUCTURE & TARGET APPLICATIONS

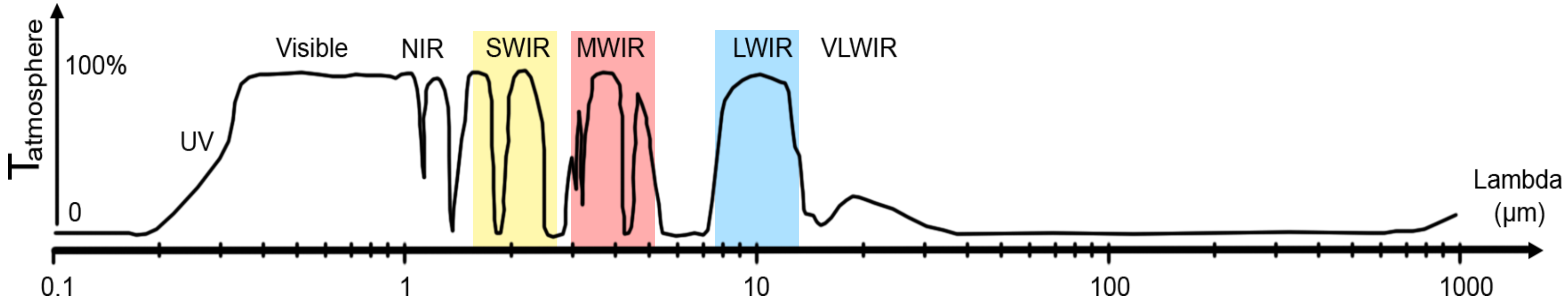


EPIR's technical infrastructure drives innovation in multiple different application spaces

PRODUCT PORTFOLIO

EPIR, Inc.	Commercial-grade Solutions			Custom Solutions	
Format	320×256 30 µm pitch	640×512 15 µm pitch	1280×720 8 µm pitch	640×512 20 µm pitch	1280×512 20 µm pitch
Relative Die Size	20×11mm	20×11mm	21×10mm	23×14mm	30×18mm
Layout					

- EPIR manufactures both standard and custom devices in the NIR to LWIR range



NIR on Si, 298K

MWIR on CZT, 140K

LWIR on CZT, 85K

eSWIR on Si, 195K

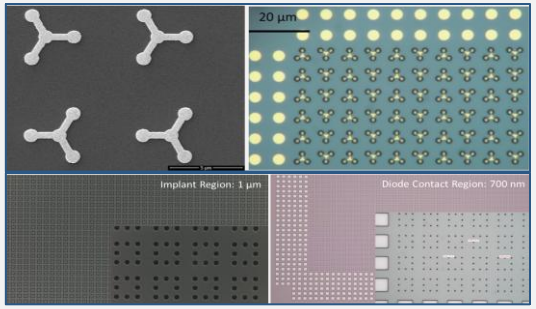
MWIR on Si, 110K

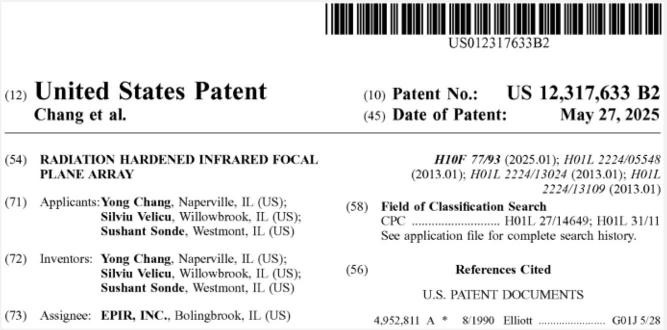
LWIR on CZT, 85K

PRODUCT PORTFOLIO

Distributed Junction FPA I & II

- Rad-hard applications
- Minimum Feature: 500nm
- US Patent 12,317,633




US012317633B2

(12) **United States Patent**
Chang et al.

(10) **Patent No.:** US 12,317,633 B2
(45) **Date of Patent:** May 27, 2025

(54) RADIATION HARDENED INFRARED FOCAL PLANE ARRAY

(71) Applicants: Yong Chang, Naperville, IL (US); Silviu Velicu, Willowbrook, IL (US); Sushant Sonde, Westmont, IL (US)

(72) Inventors: Yong Chang, Naperville, IL (US); Silviu Velicu, Willowbrook, IL (US); Sushant Sonde, Westmont, IL (US)

(73) Assignee: EPIR, INC., Bolingbrook, IL (US)

H10F 77/93 (2025.01); *H01L 2224/05548* (2013.01); *H01L 2224/13024* (2013.01); *H01L 2224/13109* (2013.01)

(58) Field of Classification Search
CPC H01L 27/14649; H01L 31/11
See application file for complete search history.

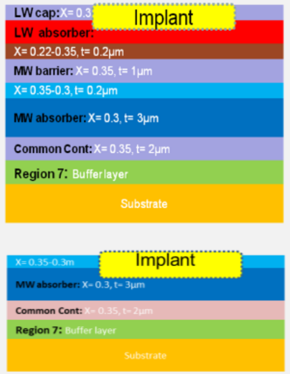
(56) References Cited

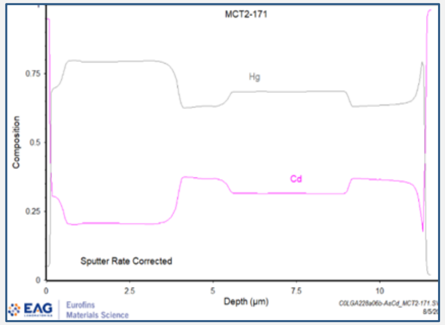
U.S. PATENT DOCUMENTS

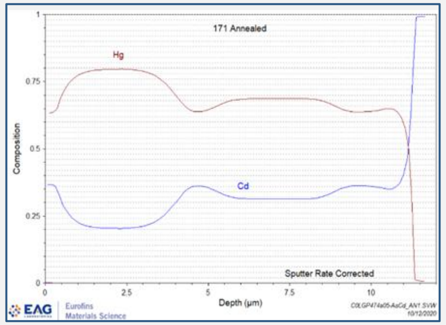
4,952,811 A * 8/1990 Elliott G01J 5/28

Highly Non-planar FPA Geometries

- Simultaneous two-color detection

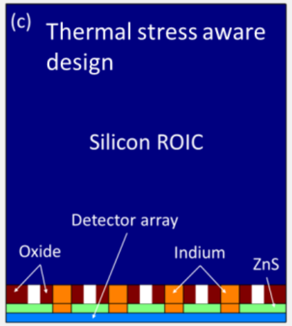


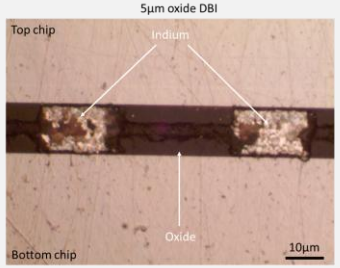


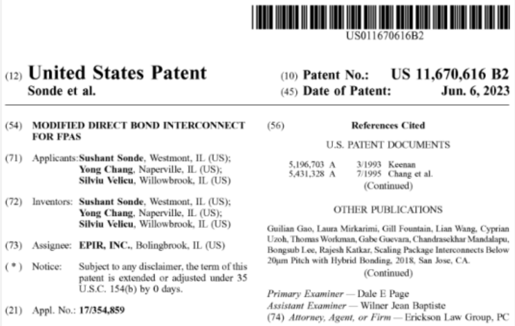


Advanced Interconnect Development

- Thermal stress aware technology for 3D hetero-integration
- Broadly applicable to various focal plane genre
- US Patent 11,670,616






US011670616B2

(12) **United States Patent**
Sonde et al.

(10) **Patent No.:** US 11,670,616 B2
(45) **Date of Patent:** Jun. 6, 2023

(54) MODIFIED DIRECT BOND INTERCONNECT FOR FPAS

(71) Applicants: Sushant Sonde, Westmont, IL (US); Yong Chang, Naperville, IL (US); Silviu Velicu, Willowbrook, IL (US)

(72) Inventors: Sushant Sonde, Westmont, IL (US); Yong Chang, Naperville, IL (US); Silviu Velicu, Willowbrook, IL (US)

(73) Assignee: EPIR, INC., Bolingbrook, IL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: 17/354,859

(56) References Cited

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(Continued)

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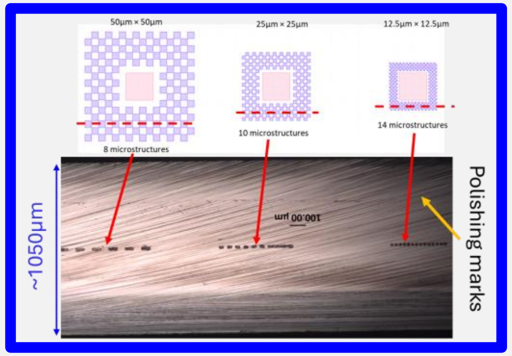
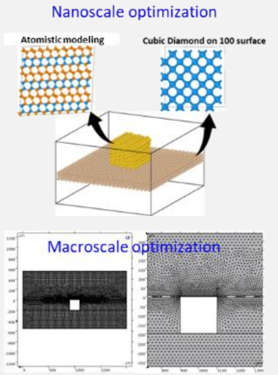
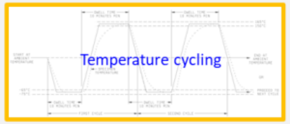
Guilian Gao, Laura Mirkarimi, Gill Fountain, Lian Wang, Cyprian Uzoh, Thomas Workman, Gabe Guevara, Chandrasekhar Mandalapu, Bongsub Lee, Rajesh Katkar, Scaling Package Interconnects Below 20µm Pitch with Hybrid Bonding, 2018, San Jose, CA.
(Continued)

Primary Examiner — Dale E Page
Assistant Examiner — Wilner Jean Baptiste
(74) *Attorney, Agent, or Firm* — Erickson Law Group, PC

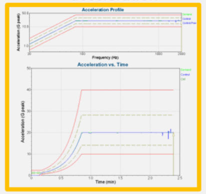
- Low temperature silicon bonding technology (Patent pending)
- Validated to military specs







Vibration, shock, constant acceleration

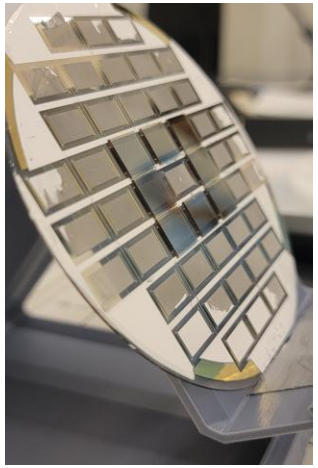


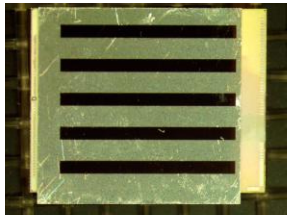
SYNERGISTIC ACTIVITIES WITH DOE

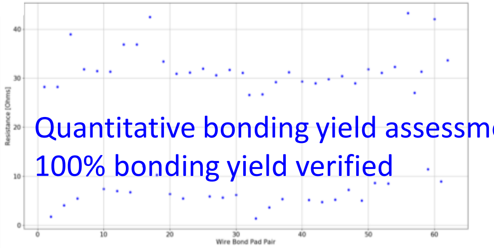
ADVANCED R&D SOLUTIONS FOR NP & HEP APPLICATIONS

Advanced Integration Technology

- Integration of ETROC1/ETROC2 with LGAD
  - Die-die/Die-to-wafer integration
  - Alignment accuracy of 500nm verified on chips down to 8µm-pitch pixel sensors
  - Conventional and thermal stress aware DBI technology
  - Improved jitter behavior > 20%



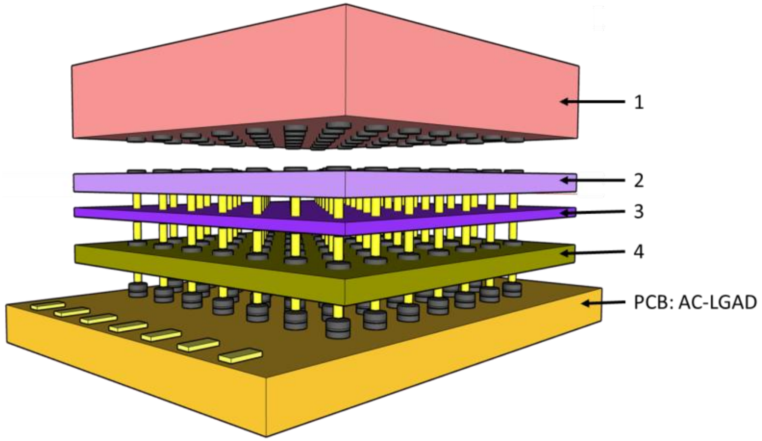




Quantitative bonding yield assessment
100% bonding yield verified

Multi-tier, Small-pixel ASIC

- VTROC: Vertically-Integrated Timing Read Out Chip

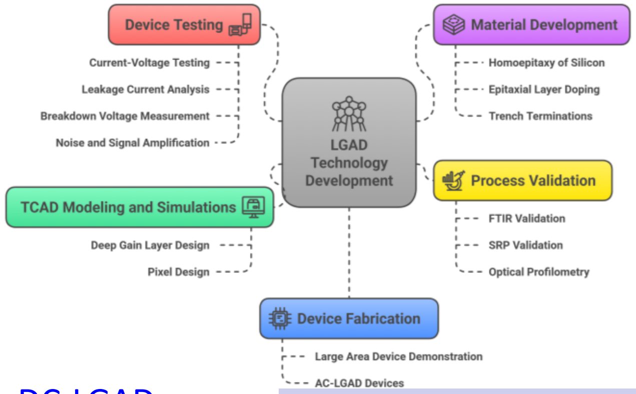


1. Detector: Small-pixel AC-LGAD
2. Front end preamp + discriminator + charge injector
3. Circular buffer memory array + readout logic
4. PCB: AC-LGAD

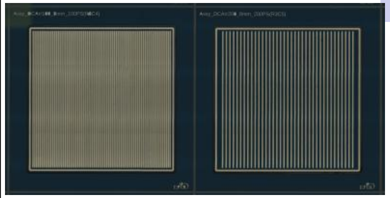
- 250µm pixel pitch
- 8×8 pixels
- Multi-tier ASICs
- 4-tier integration scheme

Radiation Tolerant Silicon Sensors

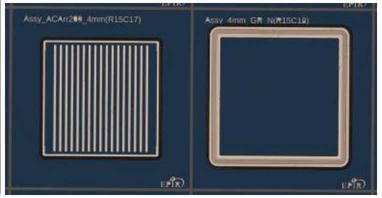
- Advanced LGAD and AC-LGAD designs
  - Multi-layer epitaxial growth
  - In-situ doping allows design flexibility
  - Large area device fabrication



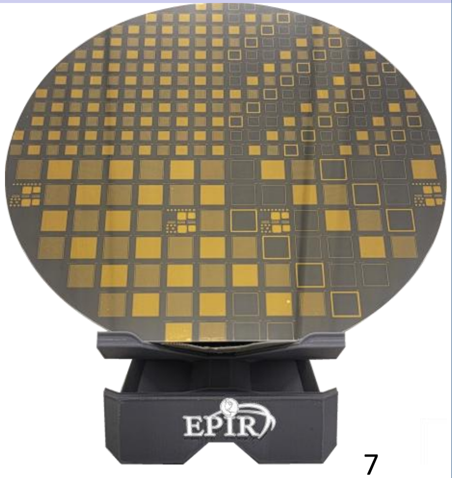
DC-LGADs



AC-LGADs



Patent App. # US63/547,881

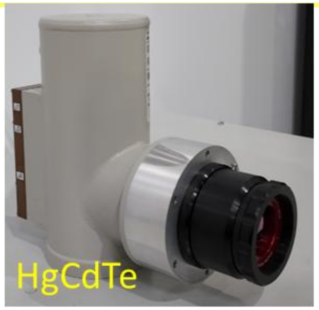


Patented technologies for advanced integration and advanced sensors

SYNERGISTIC ACTIVITIES WITH DOE

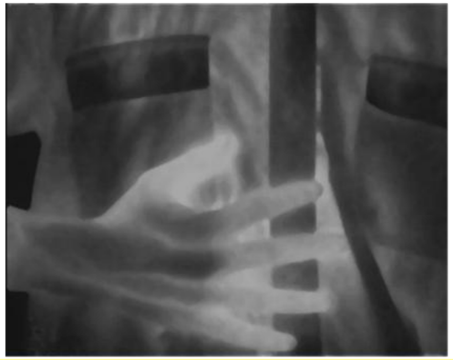
ADVANCED R&D SOLUTIONS FOR NP & HEP APPLICATIONS

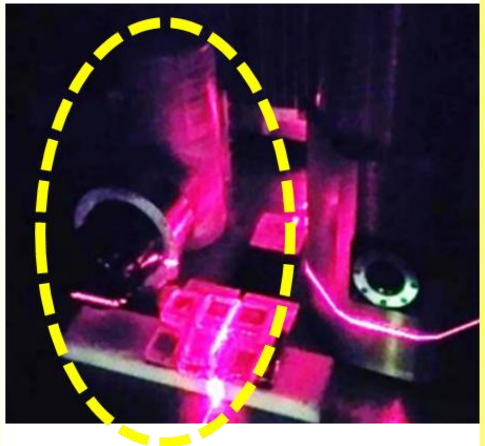
Radiation Hardened Camera



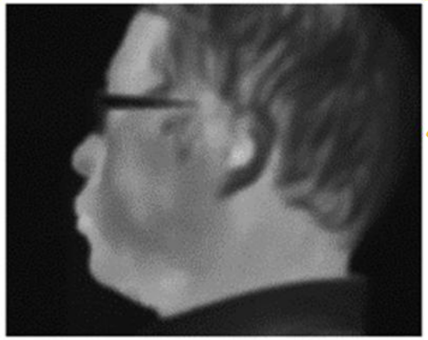
LN2 cooled Camera head

Stirling cooler camera and MWIR imager



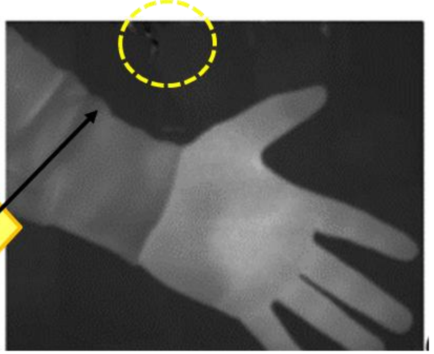


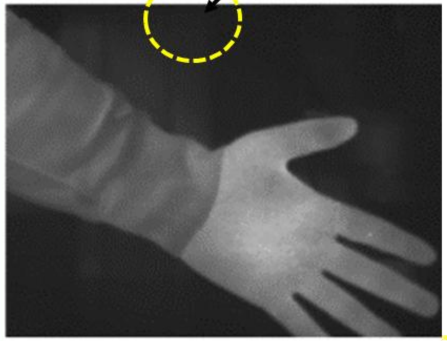
Tested under neutron irradiation 1.5×10^{13} n·cm^{-2} neutron exposure under an instant flux of 2×10^{9} n ·cm^{-2} ·s^{-1}



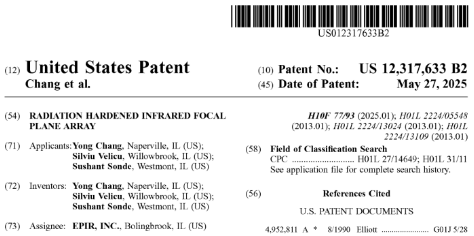
After 10^{12} n ·cm^{-2} fluence neutron exposure

After 1.5×10^{13} n·cm^{-2} fluence neutron exposure under an instant flux of 2×10^{9} n ·cm^{-2} ·s^{-1}





After an extra temperature cycling from 100K to room temperature. The circled area shows the defective pixels recovered after temperature circling.



US012317633B2

(12) **United States Patent**
Chang et al.

(10) **Patent No.:** **US 12,317,633 B2**
(45) **Date of Patent:** **May 27, 2025**

(54) **RADIATION HARDENED INFRARED FOCAL PLANE ARRAY**

(71) Applicants: **Yong Chang**, Naperville, IL (US); **Silviu Velicu**, Willowbrook, IL (US); **Sushant Sonde**, Westmont, IL (US)

(72) Inventors: **Yong Chang**, Naperville, IL (US); **Silviu Velicu**, Willowbrook, IL (US); **Sushant Sonde**, Westmont, IL (US)

(73) Assignee: **EPIR, INC.**, Bolingbrook, IL (US)

H10F 77/93 (2025.01); *H01L 2224/05548* (2013.01); *H01L 2224/13024* (2013.01); *H01L 2224/13109* (2013.01)

(58) **Field of Classification Search**
CPC H01L 27/14649; H01L 31/11
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,952,811 A * 8/1990 Elliott G01J 5/28

Patented technology for radiation hard sensor

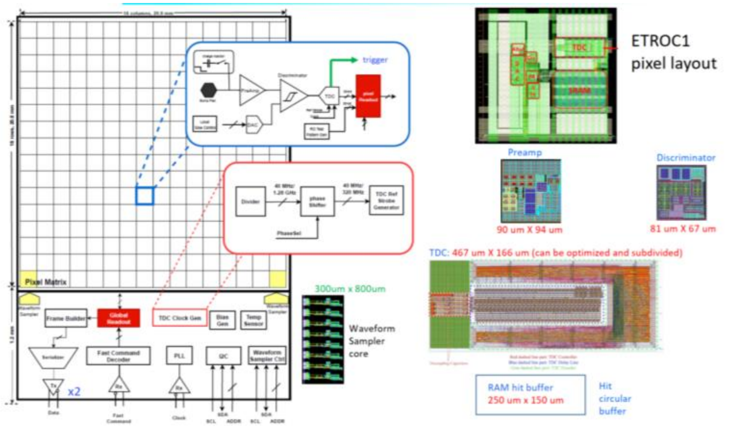
DOE's REQUIREMENTS

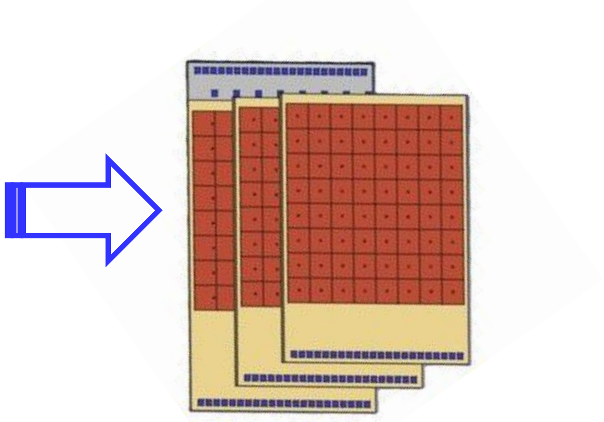
- NUCLEAR PHYSICS ELECTRONICS DESIGN AND FABRICATION
  - Front-End Application-Specific Integrated Circuits (ASICs)
  - Solicitation requirements:
    - Very low power and very low noise charge amplifiers and filters, very high-rate photon-counting circuits, high-precision charge and timing measurement circuits, low-power and small-area ADCs and TDCs, efficient sparsifying and multiplexing circuits.
    - Two-dimensional high-channel-count circuits for small pixels combined with high-density, high-yield, and low-capacitance interconnection techniques. Layering these 2D ASICS via interconnects to increase functionality is also of interest.
    - Microelectronics for extreme environments such as high-radiation (both neutron and ionizing) and low temperature, depending on the application. Specifications for the former are: high channel count (64 channels) ASIC with fast timing (< 10 ps), high radiation hardness (10 Mrad with 10^{15} n/cm^2), fast waveform sampling (> 4GHz) and bandwidth (> 2GHz)
  - Participating teams:
    - Fermilab:
    - EPIR, Inc.

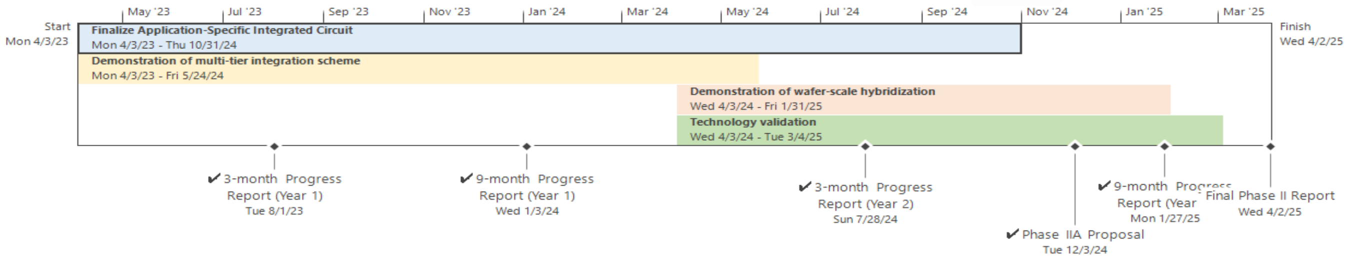
PROPOSED SOLUTION

VERTICALLY INTEGRATED TIMING READOUT CHIP (VTROC)

1300µm× 1300µm pixel footprint 250µm× 250µm pixel footprint







- Multi-tier ASIC
  - Small pixel ASIC: 250µm pixel pitch, 8×8-pixel array
  - Tier 1: Charge injection + Preamplifier + Discriminator, analog front-end
  - Tier 2: Low power Time-to-Digital Converter (TDC)
  - Tier 3: Read out circuit
- Modified Direct Bond Interconnect based multi-tier integration
  - Thermo-mechanical model considering effect of:
    - Bonding geometry
    - Bonding material
    - Detector/Read-out thickness
    - Interconnect metal
    - AI guided optimization
- Prototype demonstration on LGAD-VTROC integration

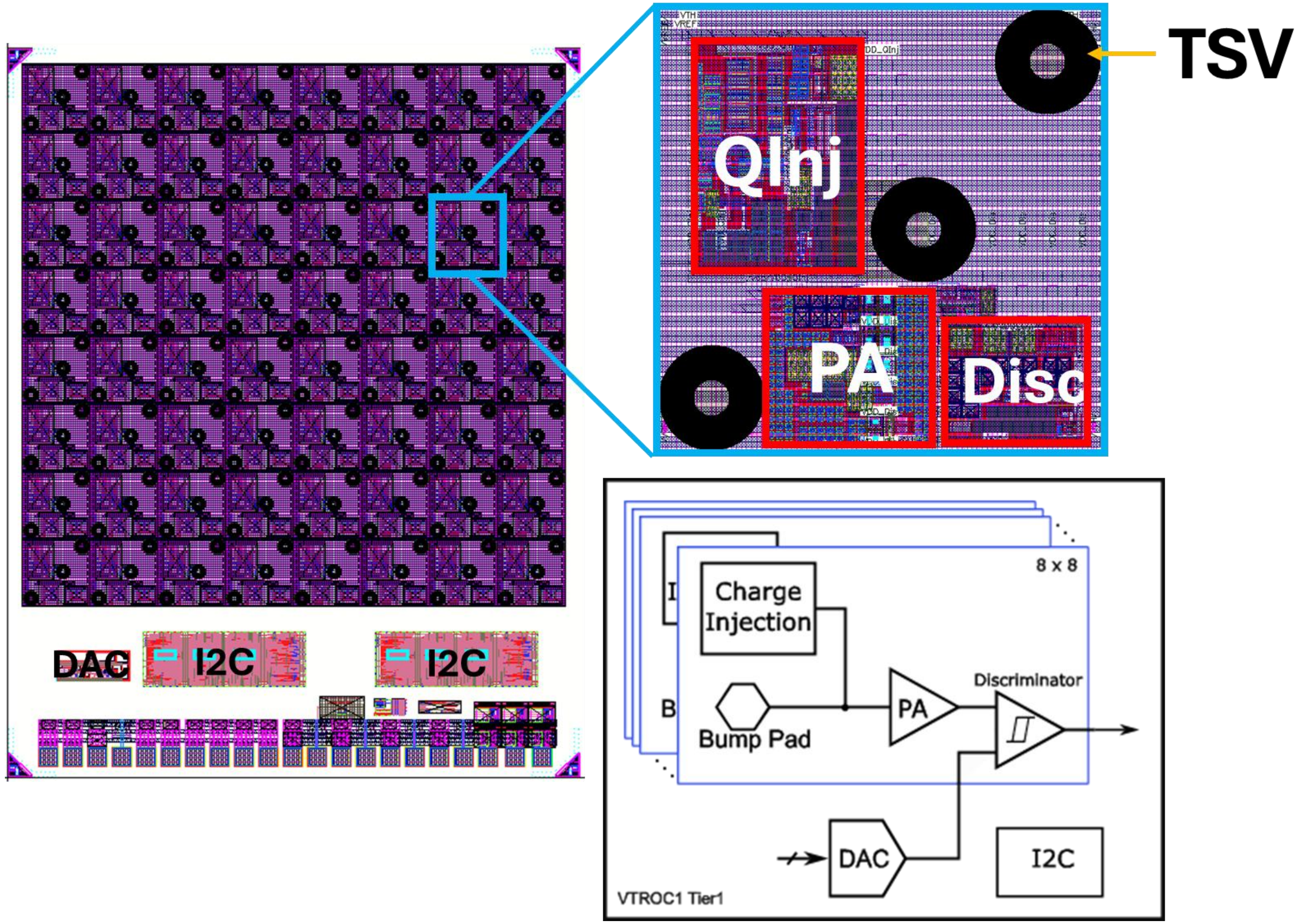
Challenges

- Optimizing circuit blocks to fit reduced footprint (80% of the state-of-the-art)
- Manage power density with reduced pixel footprint
- High-yield multi-tier integration

Expected improvements

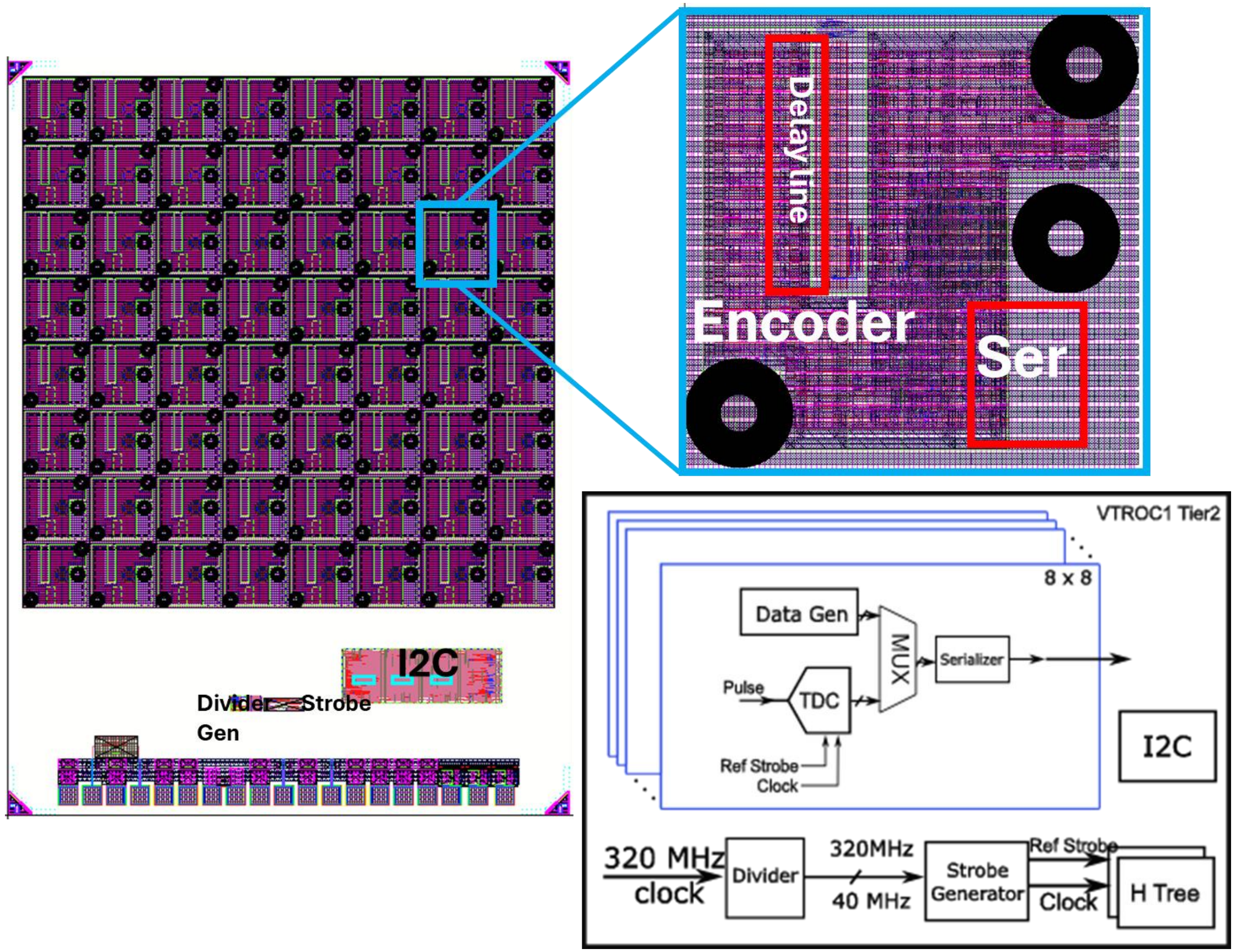
- Separation of low noise analog circuitry from digital blocks
- Improved spatial resolution (260%)
- Improved timing resolution (100%)
- Towards 4D detectors

ASIC DESIGN: TIER 1 – FRONT END PREAMP + DISCRIMINATOR + CHARGE INJECTOR



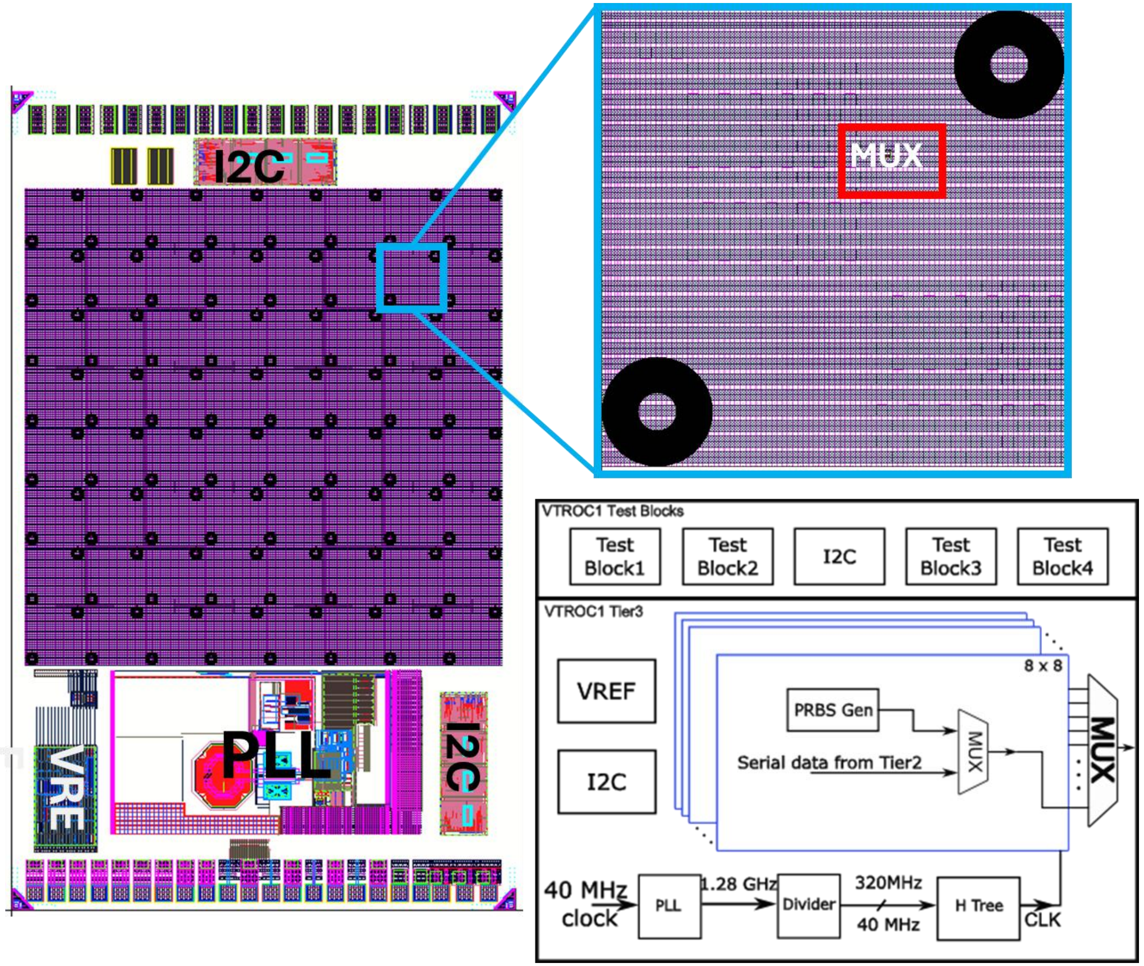
- Tier 1 has an 8×8 pixel array (2mm×2mm), a DAC and two I2C modules with different device addresses. Each pixel has a Qinj, a preamp (PA) including bias, a discriminator, and TSVs. The center TSV is used to deliver Disc output (Tier 1) to TDC pulse input (Tier 2).
- Charge injection signal comes from the external generator through differential-to-single ended eRx. The charge injection signal is delivered by H tree.
- The matrix is split into two sections. The left half has the PA from ETROC project. The right half includes the PA with higher current.
- The outputs of three pixels at the bottom row (0, 24, 32, 56) will be exported to pads for Tier1 testing purposes.
- All the blocks in Tier 1 are in place. Final integration is ongoing.

ASIC DESIGN: TIER 2 – LOW POWER TDC



- Tier 2 has an 8×8 pixel array, a divider, a strobe generator, and a I2C. This TSV is used to transmit the serial data from Tier 2 to Tier 3.
- Tier 2 receives external differential 320 MHz clock. The 320 MHz clock is divided into 40 MHz. The strobe generator produces a strobe signal.
- The strobe signal and 40 MHz clock are delivered to each pixel via two paralleled H tree.
- The delay line, divider, strobe generator, H trees and I2C are in place.
- The encoder and the serializer need to be verified and optimized.

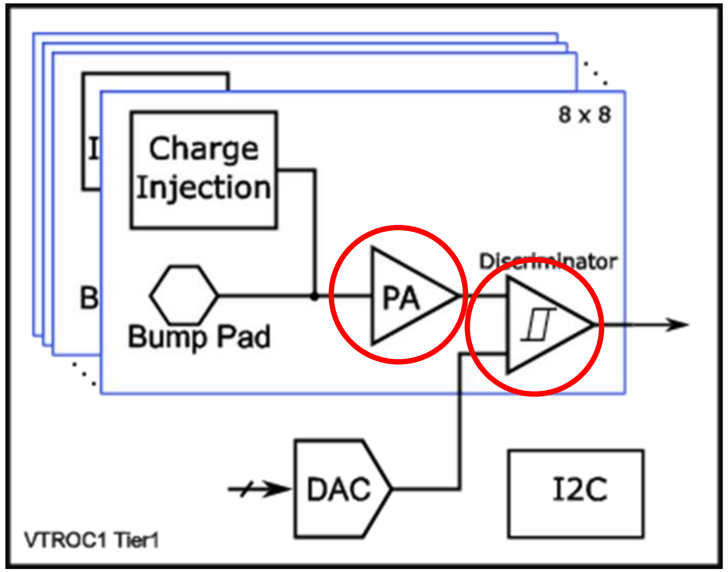
ASIC DESIGN: TIER 3 – READOUT CIRCUITRY + TEST BLOCKS



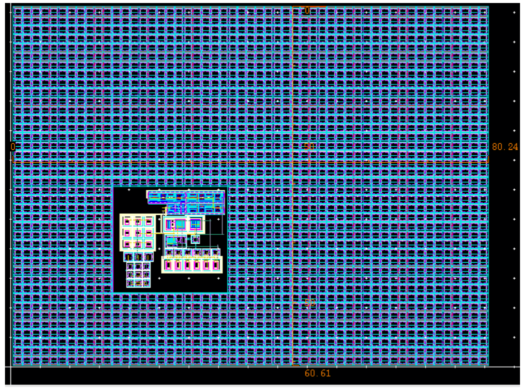
- Tier 3 has an 8×8 pixel matrix, a clock generator (PLL + phase shifter) a I2C module, TSVs and 20 wire bonding pads for analog /digital powers, I2C controls, clock input and data output.
- The data is scrambled before output.
- A Fast command decoder receives the fast commands via eRx and decodes into the control signal to broadcast.
- The MUX, reference generator, PLL, phase shifter, I2C are in place.
- 2000µm×350µm area at the top of Tier 3 is reserved for 4 test blocks.
- The 4 test blocks are being optimized.

ASIC DESIGN: POWER CONSUMPTION

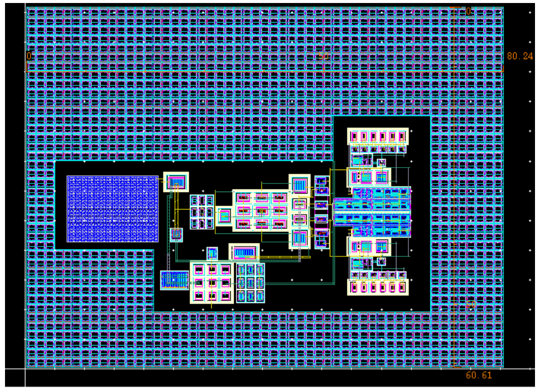
- In pixelized detectors, power consumptions of the front-end preamplifiers and discriminators become a concern. As the number of detector elements or pixels continues to increase, front-end circuits of much lower power consumption are required.
- A new circuit, pseudo thyristor is designed as a discriminator with power consumption 10-20 times lower than existing discriminator (below 100µW per channel).



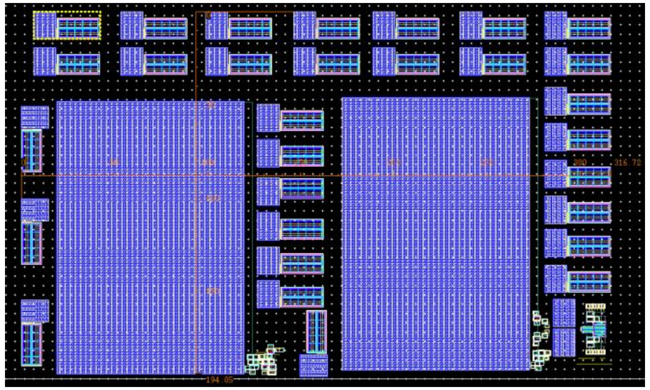
Test Block #1



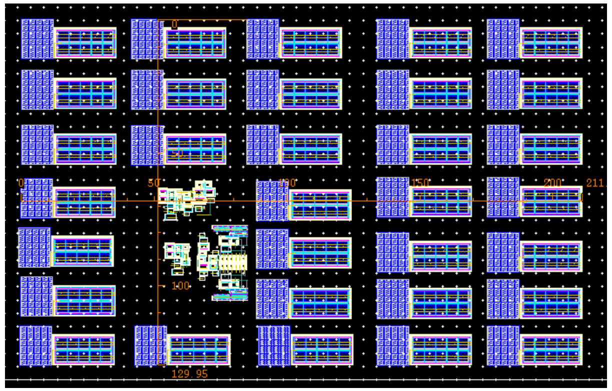
Test Block #2



Test Block #3



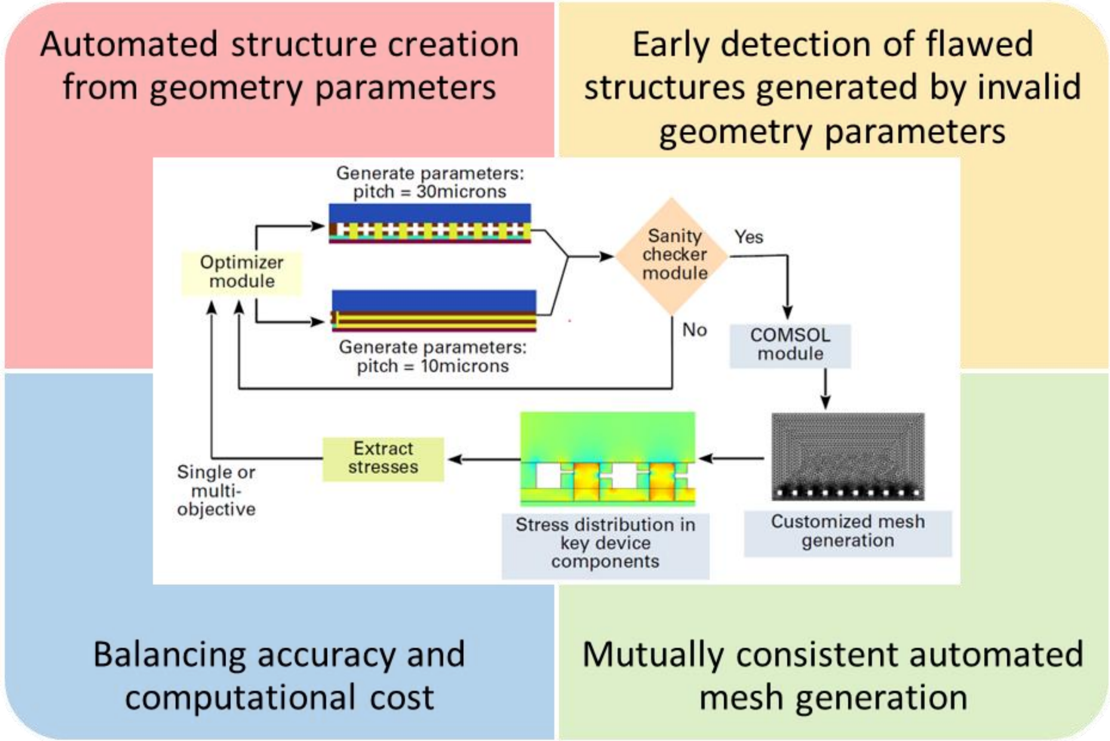
Test Block #4

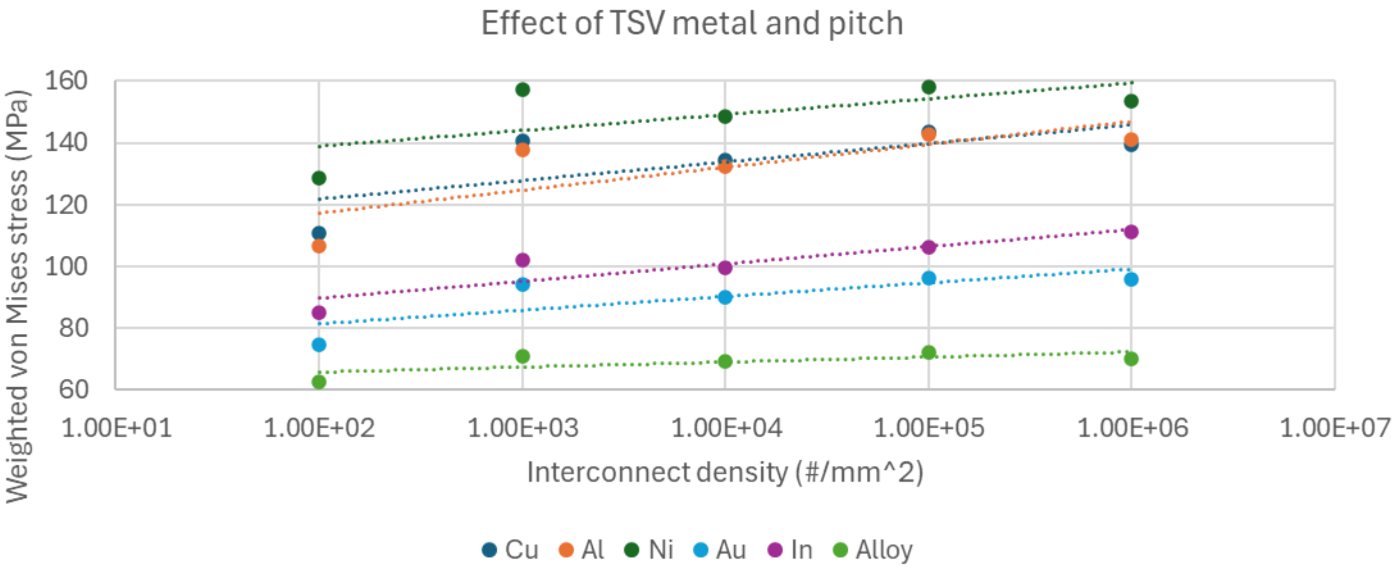


TASK 2: DEMONSTRATION OF MULTI-TIER INTEGRATION SCHEME

TSV DESIGN: KEEP OUT ZONE

- Thermo-mechanical modeling
  - Automated thermal stress evaluation and geometry optimization workflow





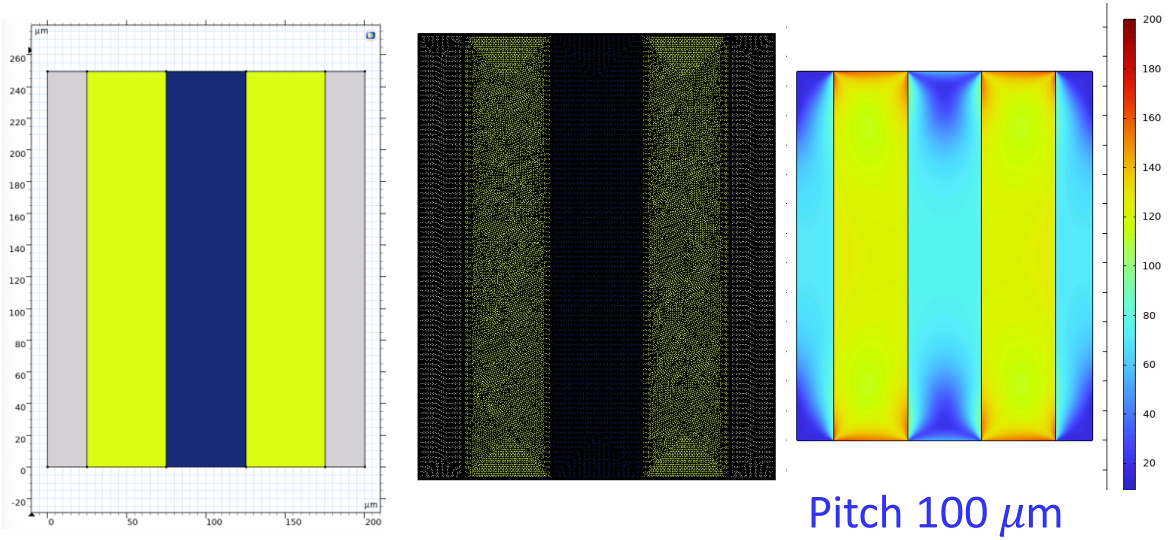
- Higher TSV/interconnect density increases the average thermo-mechanical stress
- This will affect ‘Keep Out Zone’ considerations
- Use of alternate interconnect metal(s) can be considered

TASK 2: DEMONSTRATION OF MULTI-TIER INTEGRATION SCHEME

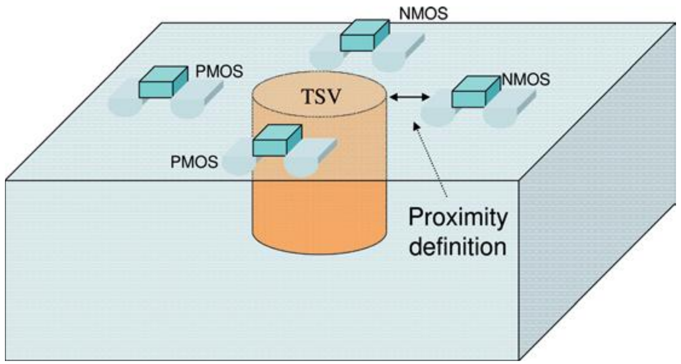
Fermilab EPIR

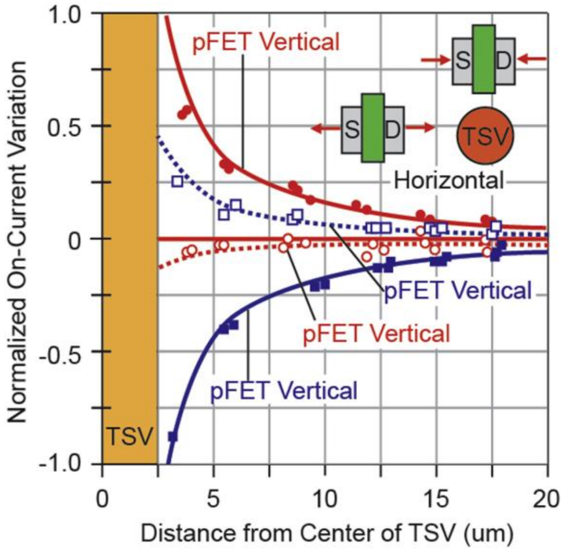
TSV DESIGN: KEEP OUT ZONE

- Mechanical stress can affect MOSFET devices.
- Compressive stress enhances the mobility of pFETs whereas tensile stress enhances the mobility of nFETs.
- TSVs create stress in Si that can extend up to 20µm away from the edge of the TSV.
- Most of the thermomechanical stress is concentrated at the surface.
- This affects positioning of the TSVs.



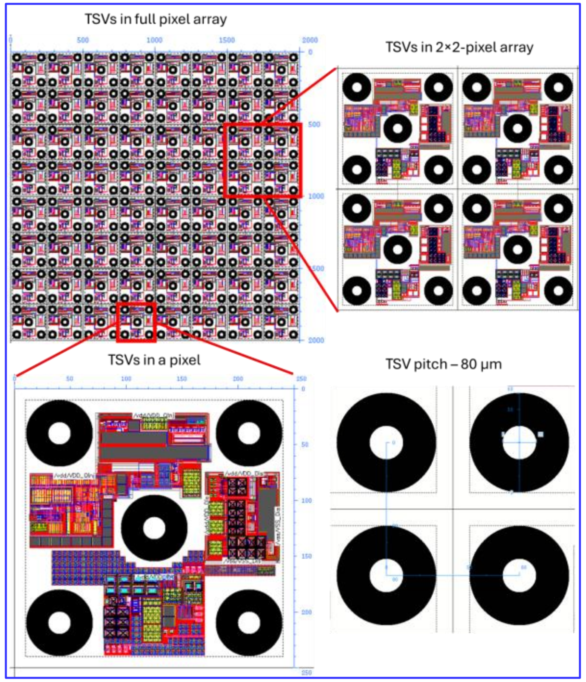
Pitch 100 μm



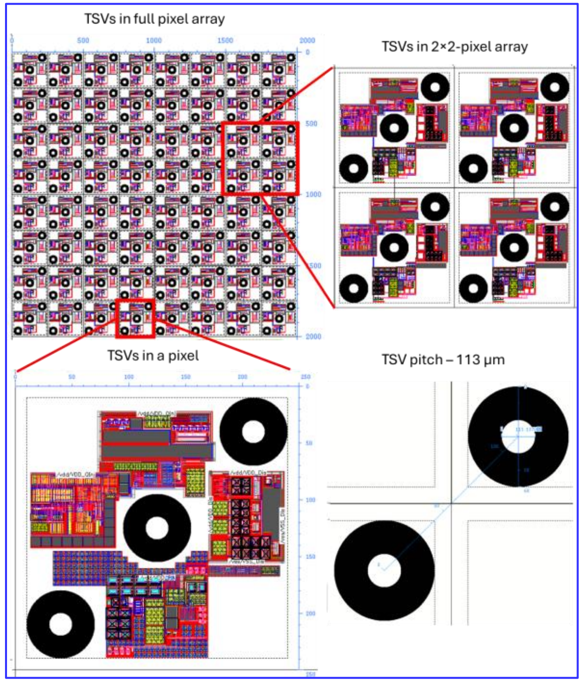


TASK 2: DEMONSTRATION OF MULTI-TIER INTEGRATION SCHEME

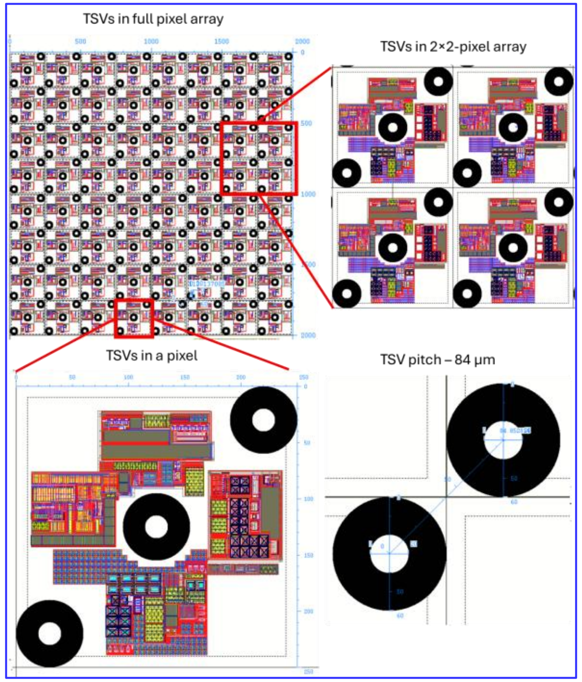
TSV DESIGN: OPTIMIZED NUMBER & LOCATIONS



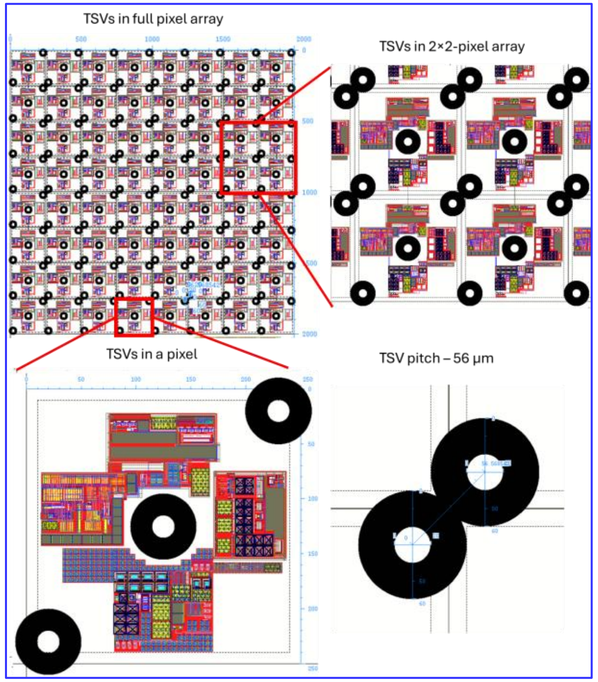
TSV Scheme 1



TSV Scheme 2



TSV Scheme 3



TSV Scheme 4

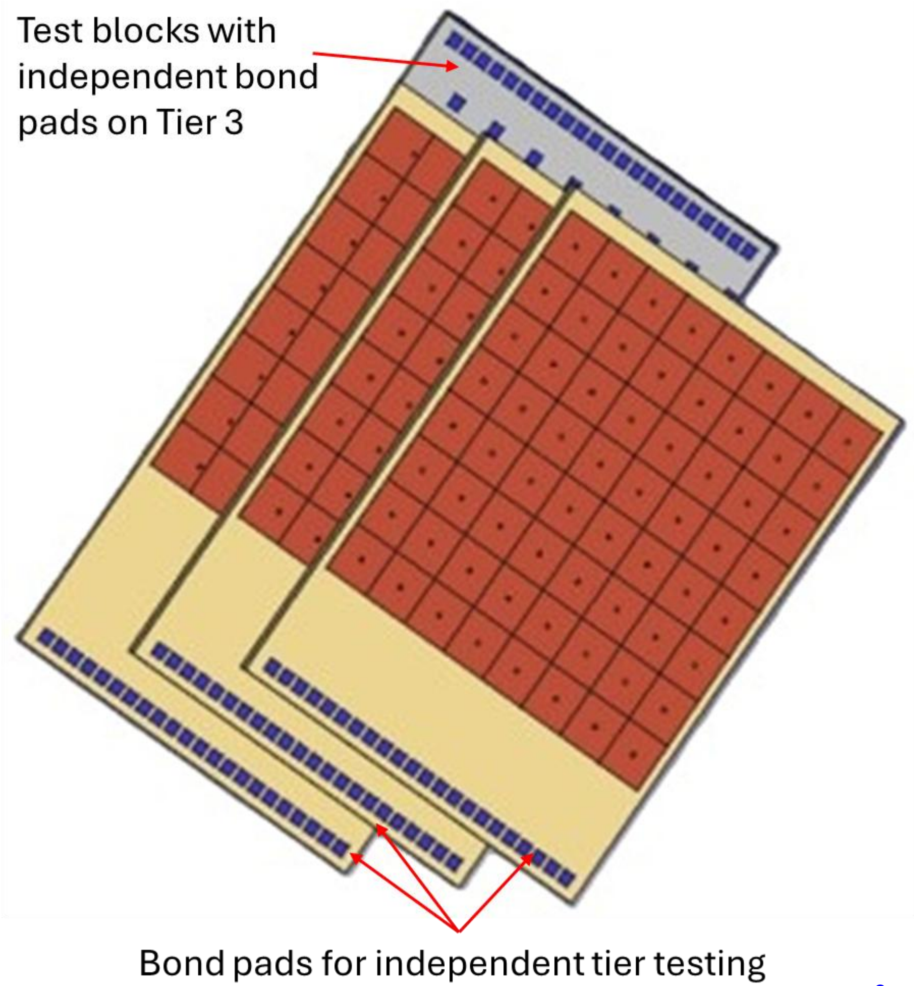
Optimized # of TSVs to minimum required

Optimized TSVs locations
TSV pitch: 84µm

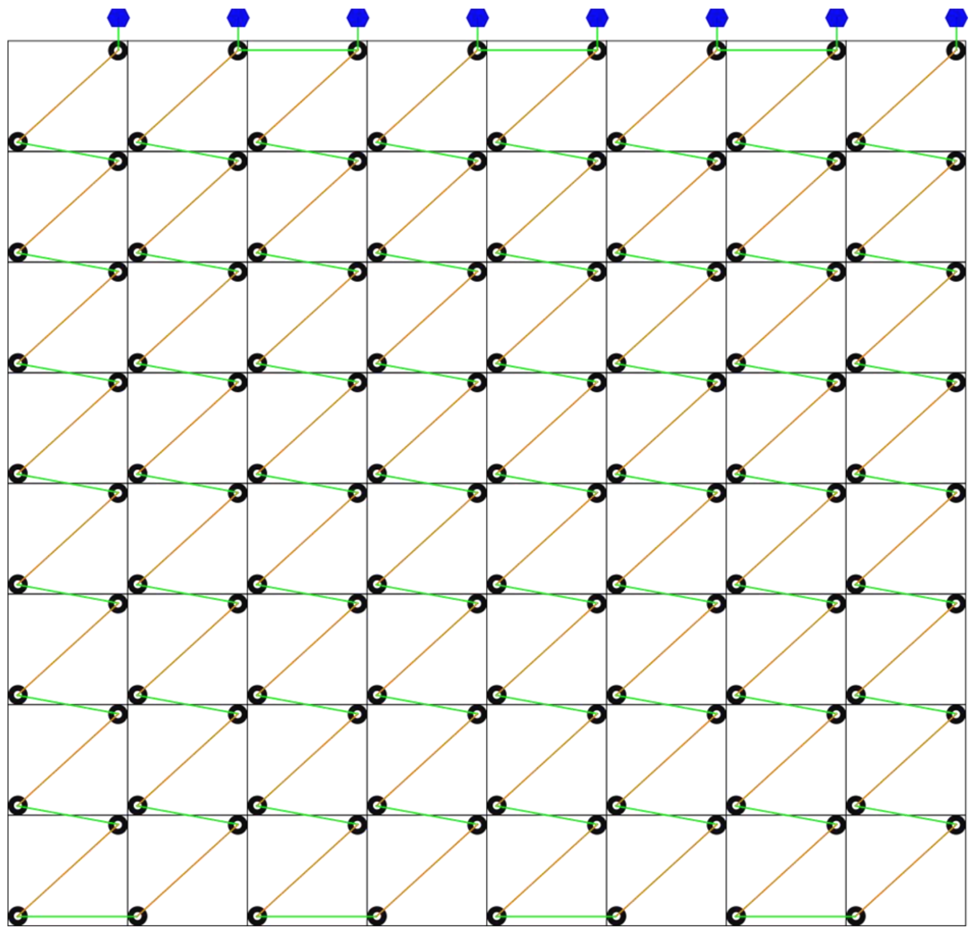
Optimized TSVs locations
TSV pitch: 56µm

TASK 2: DEMONSTRATION OF MULTI-TIER INTEGRATION SCHEME

MILTI-TIER DESIGN & TSV TEST SCHEME



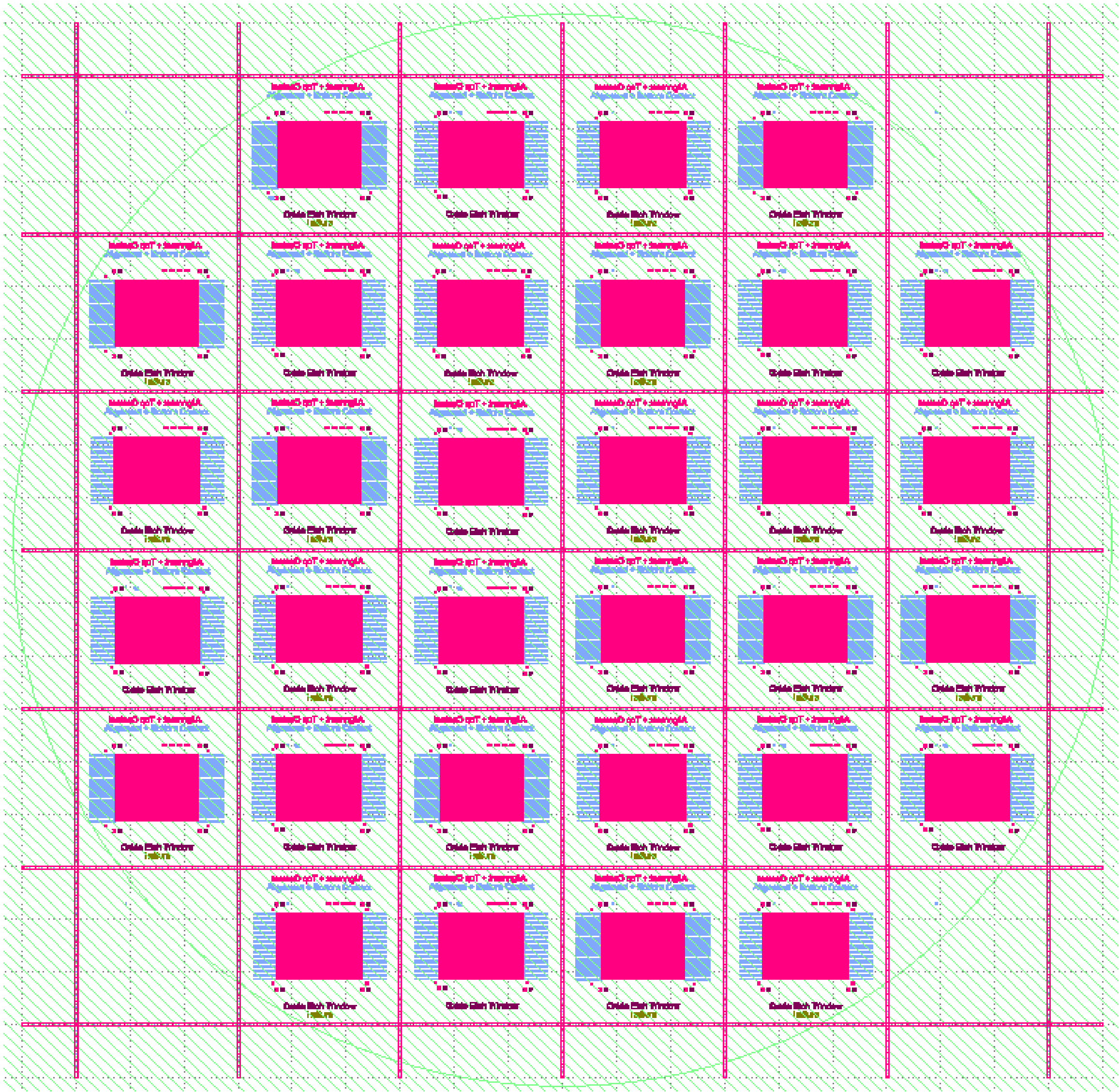
TSV test scheme



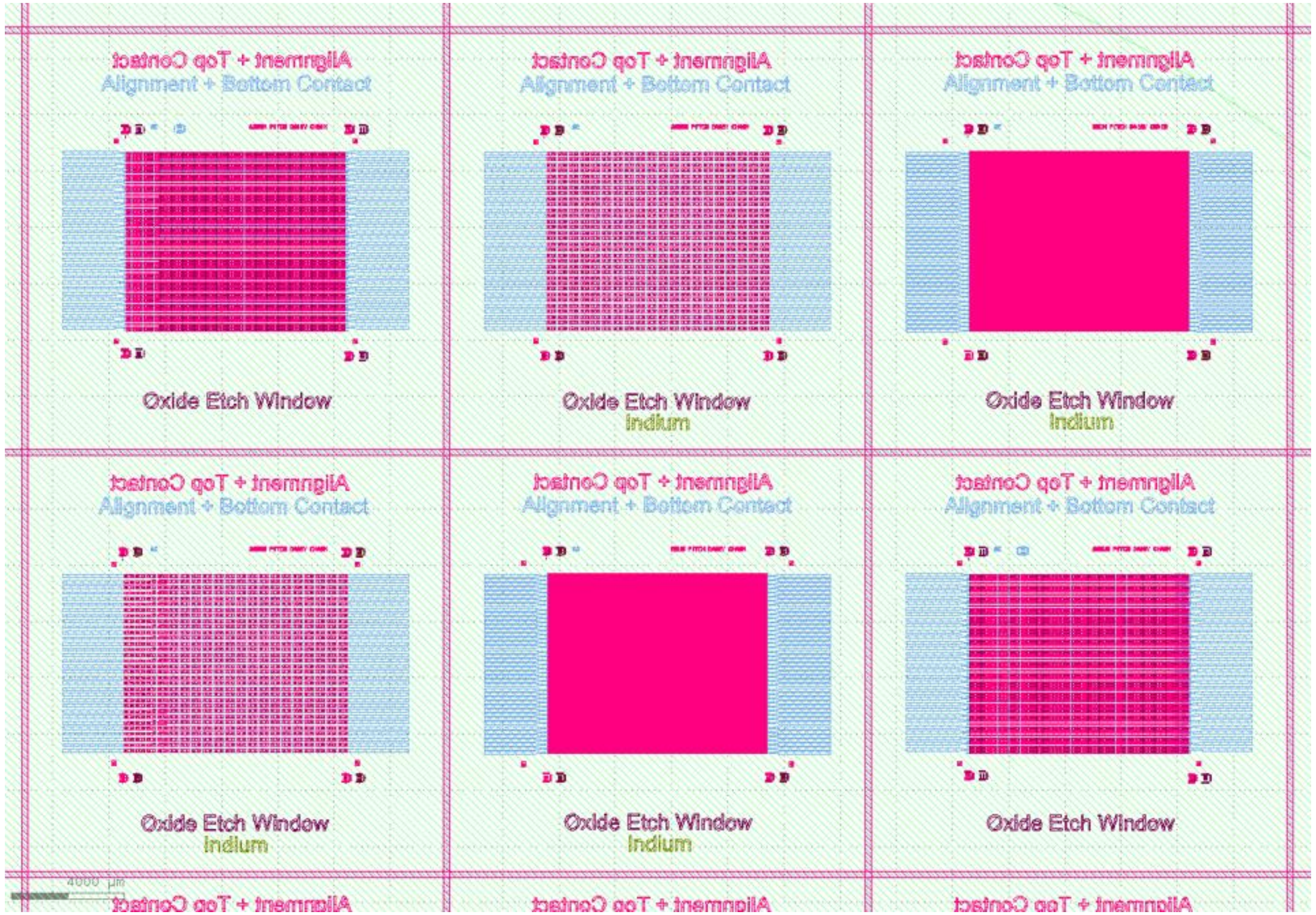
- Daisy-chain structures to validate multi-tier integration

TASK 2: DEMONSTRATION OF MULTI-TIER INTEGRATION SCHEME

MULTI-TIER INTEGRATION PROCESS DEVELOPMENT



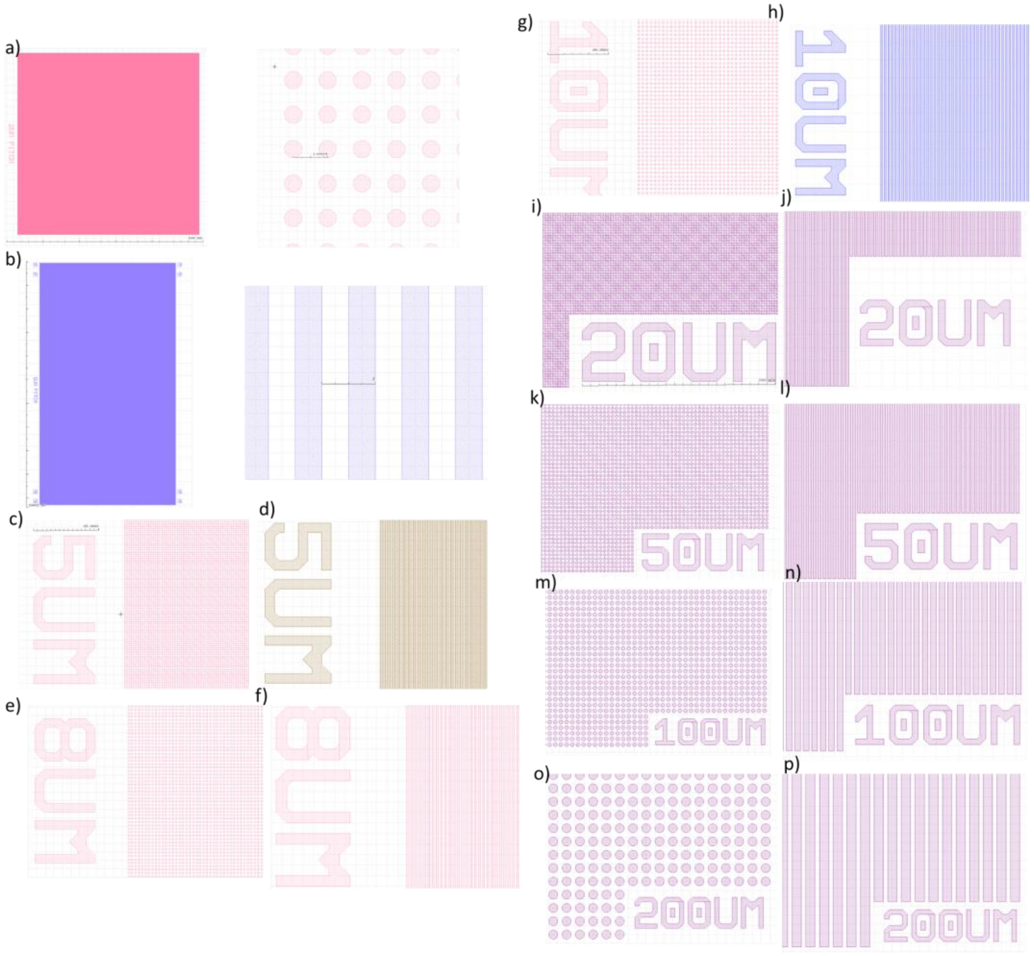
- Includes TSVs with following pitches
  - 50µm
  - 100µm
  - 200µm

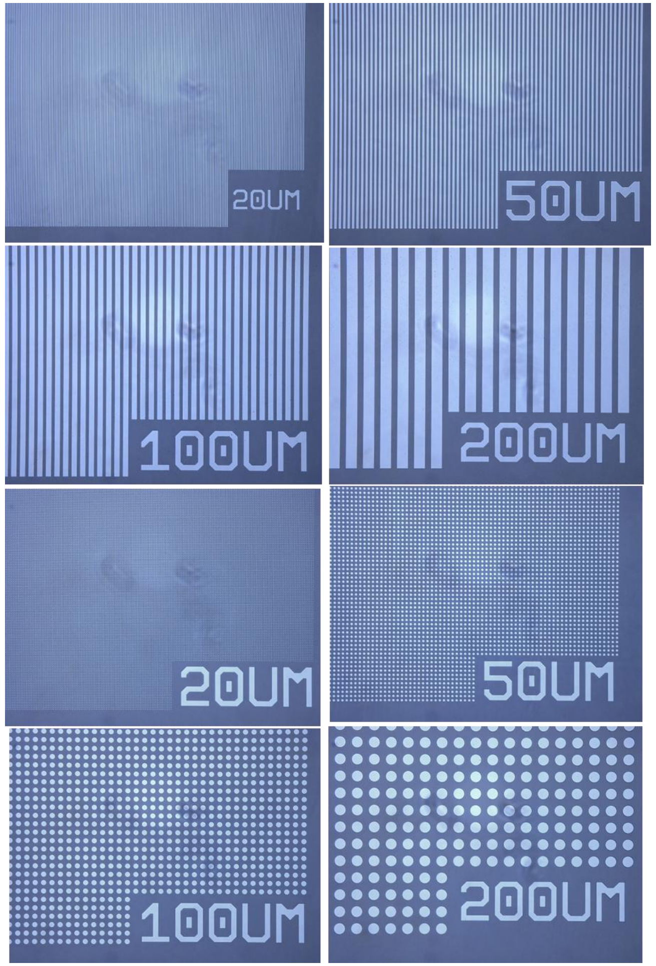


TASK 2: DEMONSTRATION OF MULTI-TIER INTEGRATION SCHEME

Fermilab EPIR

MULTI-TIER INTEGRATION PROCESS DEVELOPMENT

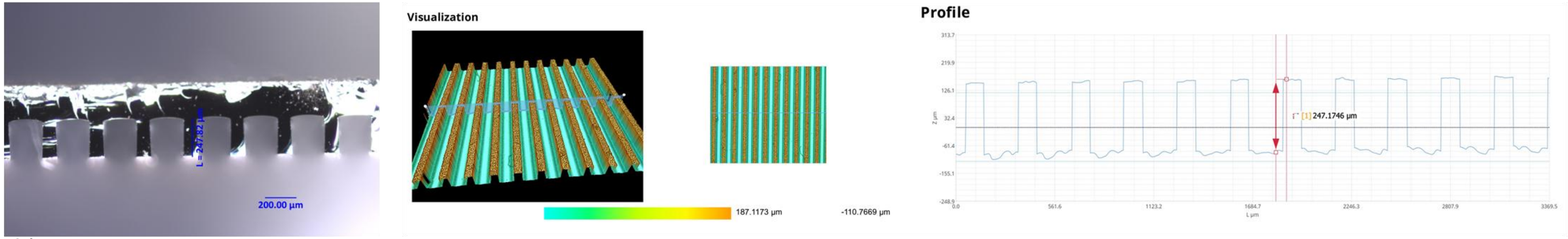




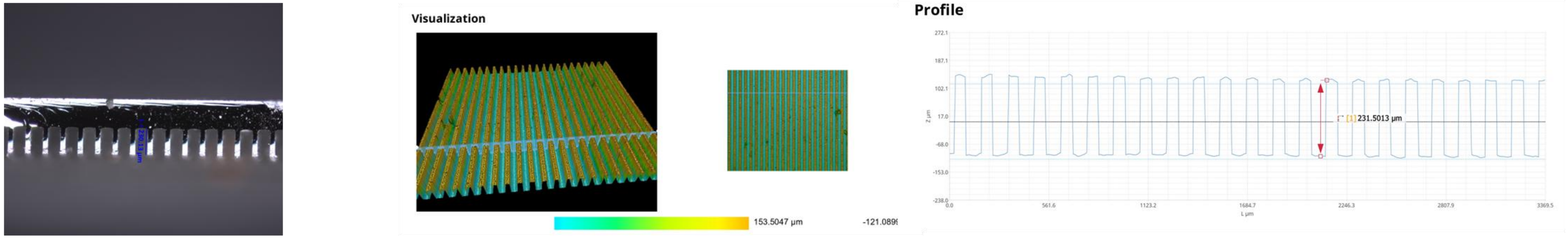
- Optimized lithography process
- Wafer-scale TSV development

MULTI-TIER INTEGRATION PROCESS DEVELOPMENT

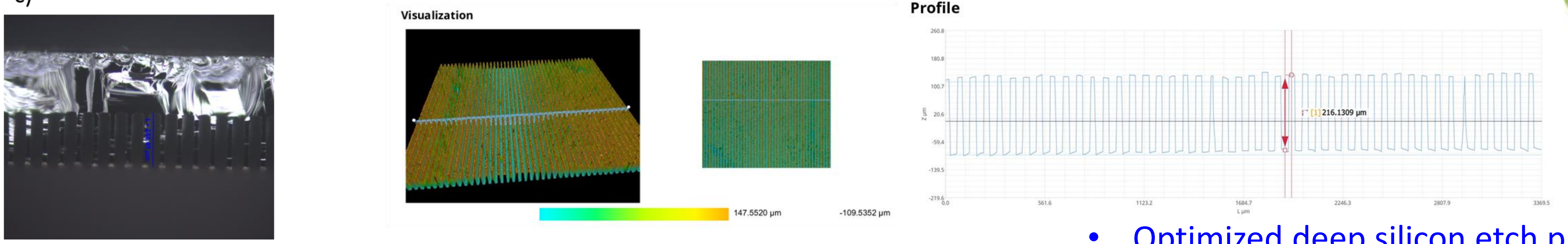
a)

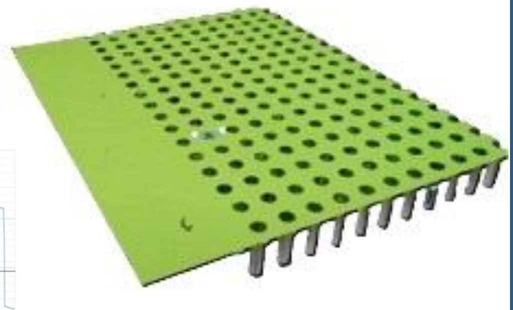


b)



c)

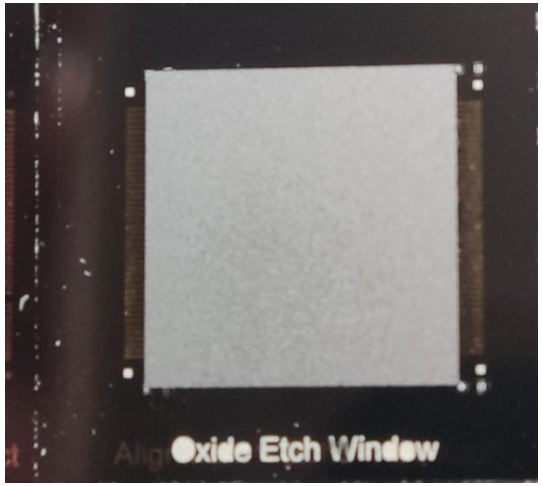


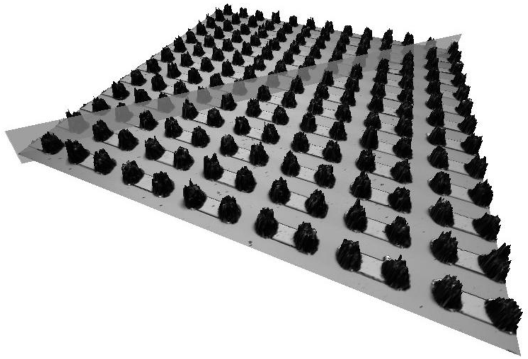


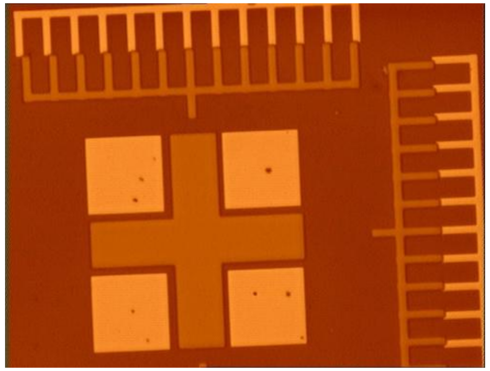
- Optimized deep silicon etch process
- Wafer-scale TSV development

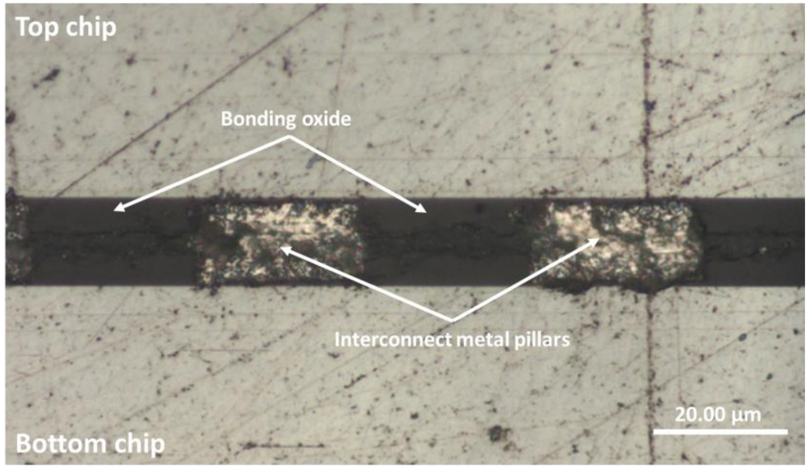
WAFER-SCALE BONDING PROCESS DEMONSTRATION

Die-to-die integration scheme

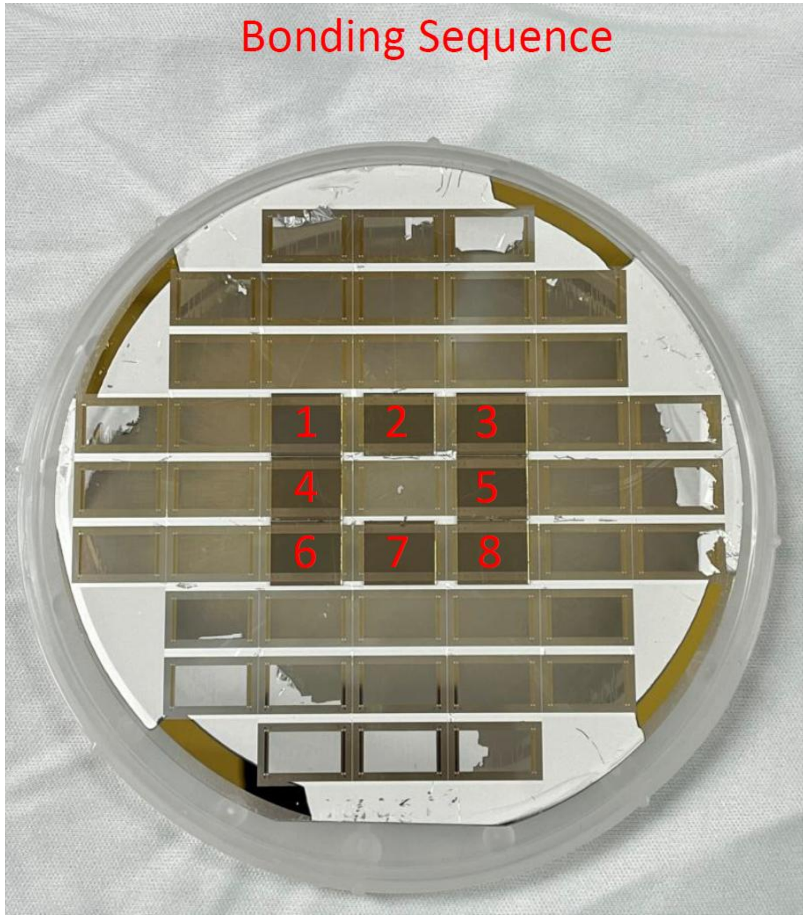








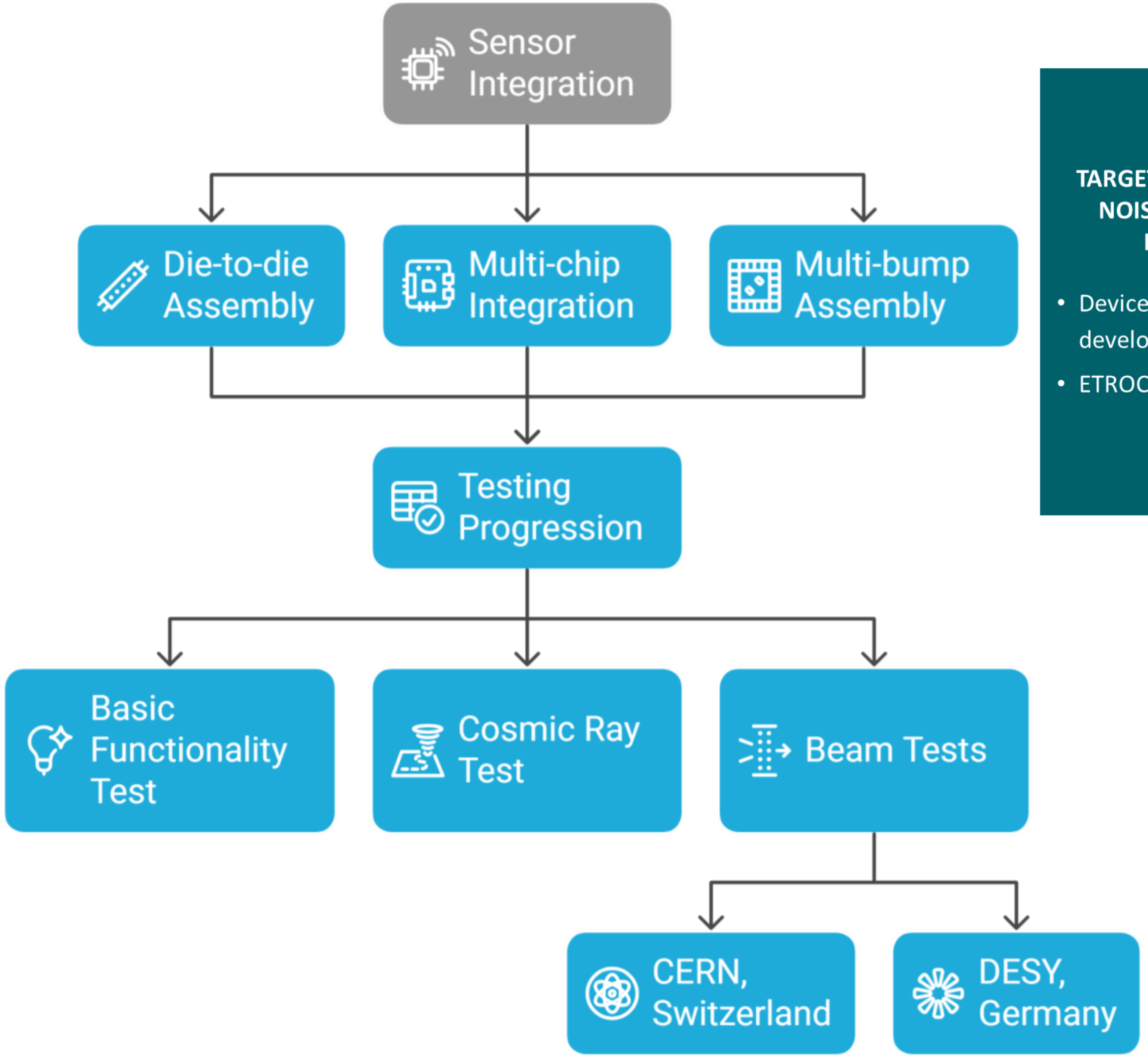
Die-to-wafer integration scheme



Conventional and DBI integration

- Excellent alignment accuracy: within 500nm
- Excellent vertical etch
- Void-free metal pillars
- Void-free interface: Metal interconnect and oxide are in very good contact
- Integration process for detectors down to 8µm pixel pitch

EARLY DEMONSTRATION OF VTROC (2D) – PLAN



EPIR, Inc.

TARGET: HIGH YIELD, LOW NOISE SENSOR ARRAY INTEGRATION

- Device process development
- ETROC2-LGAD integration

Fermilab

TARGET: BASELINE DEVICE VALIDATION

- Extensive chip level testing
- Baseline and noise width
- Cosmic ray data taking

CERN

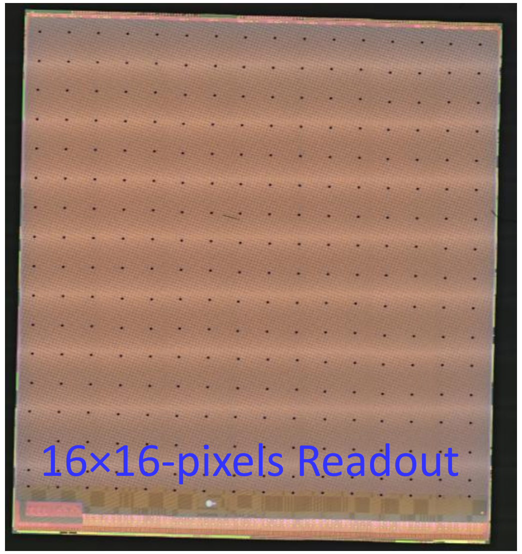
TARGET: BEAM TEST

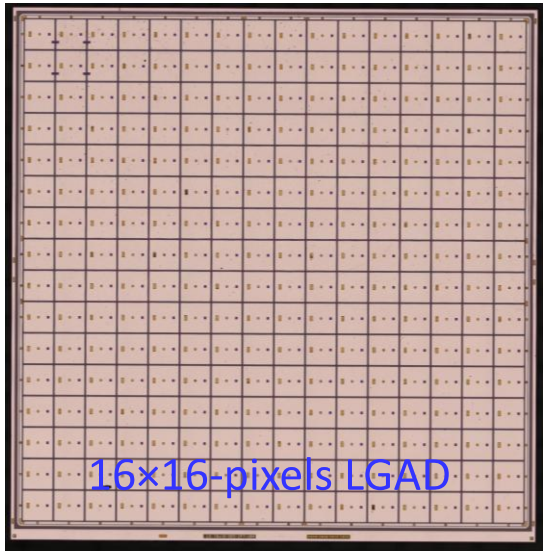
- Beam test with 120 GeV proton/pion beam at CERN

DESY

TARGET: BEAM TEST

- Beam test with 4 GeV electron beam at DESY (Hamburg)



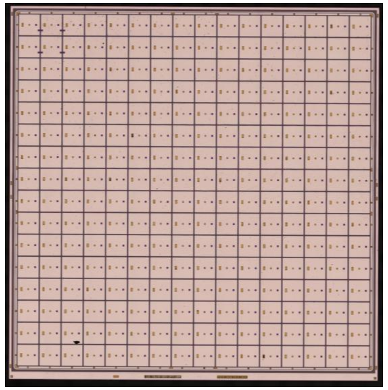


Representative device and characterization data follows.

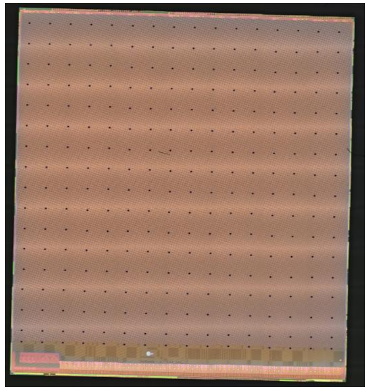
EARLY DEMONSTRATION OF VTROC (2D) – INTEGRATED ASSEMBLIES

Die-to-die assembly

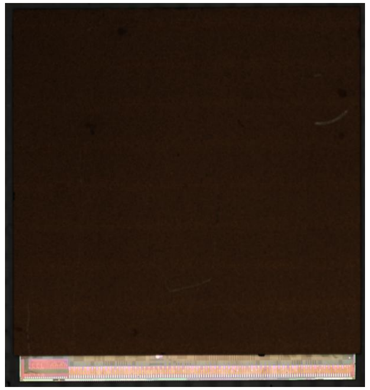
16×16-pixel sensor



16×16-pixel readout chip

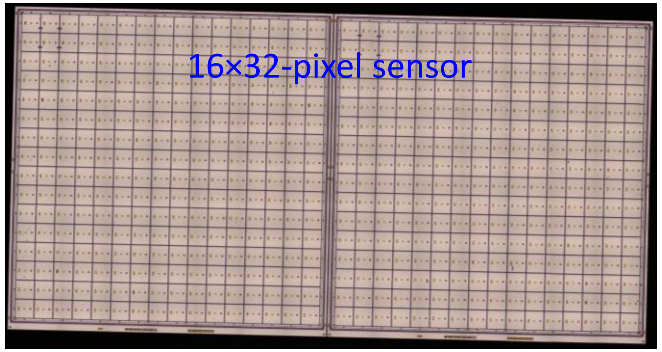


Integrated assembly

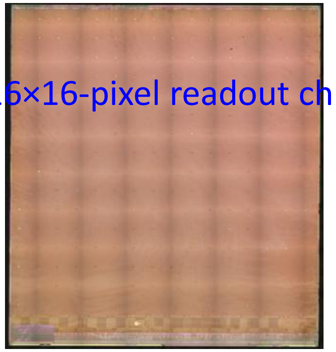


Multi-chip assembly

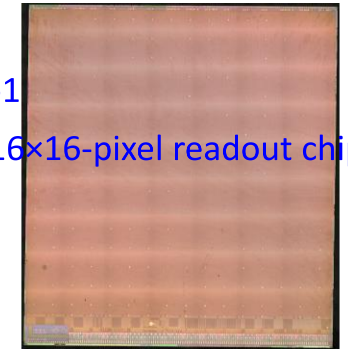
16×32-pixel sensor



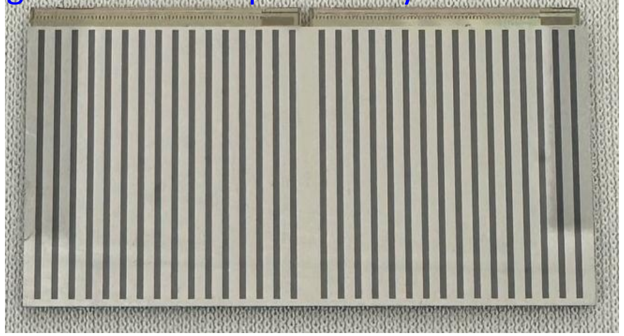
16×16-pixel readout chip1



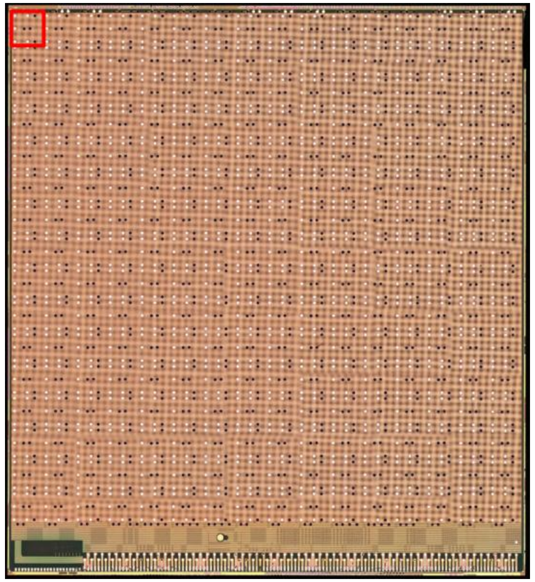
16×16-pixel readout chip2



Integrated multi-chip assembly: Sensor side view



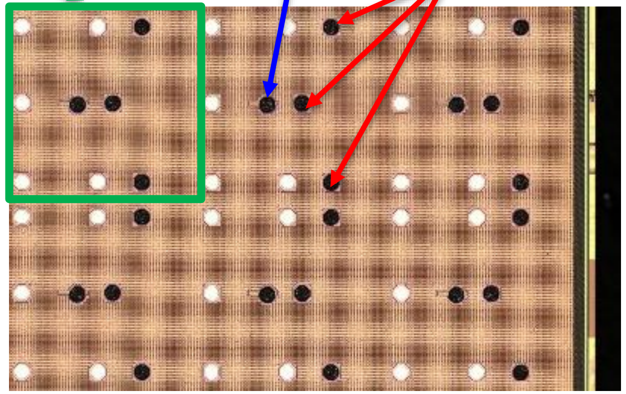
Multi-bump assembly



Single pixel

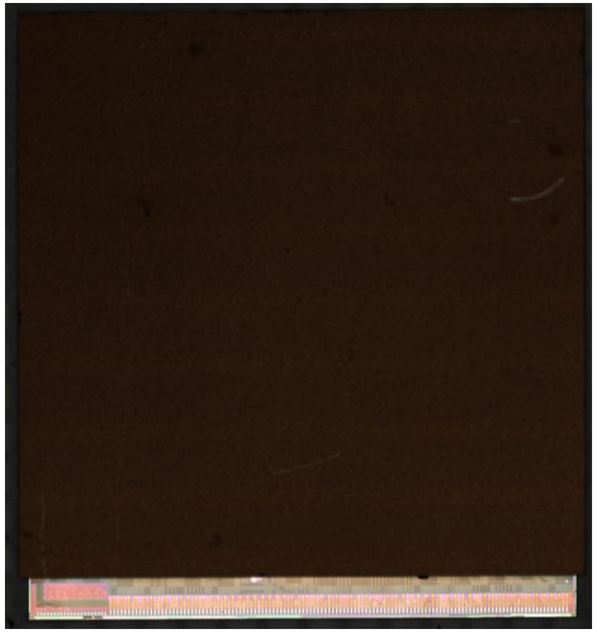
Central pixel pad with indium bump

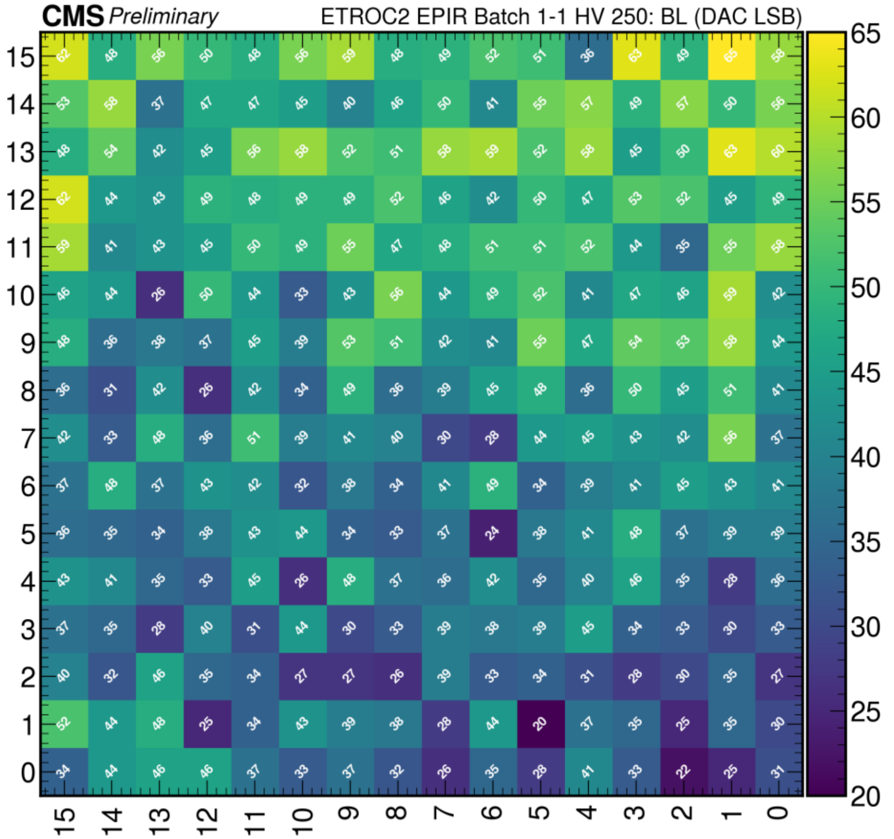
Additional dummy pads with indium bumps

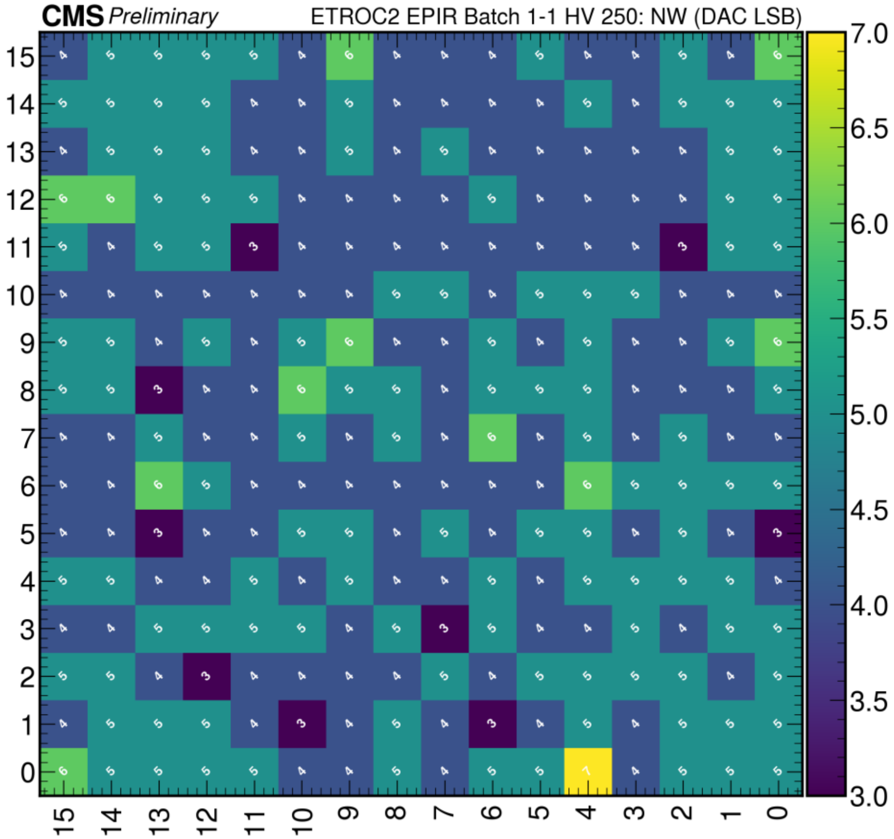


EARLY DEMONSTRATION OF VTROC (2D) – BASIC FUNCTIONALITY TEST

Integrated assembly

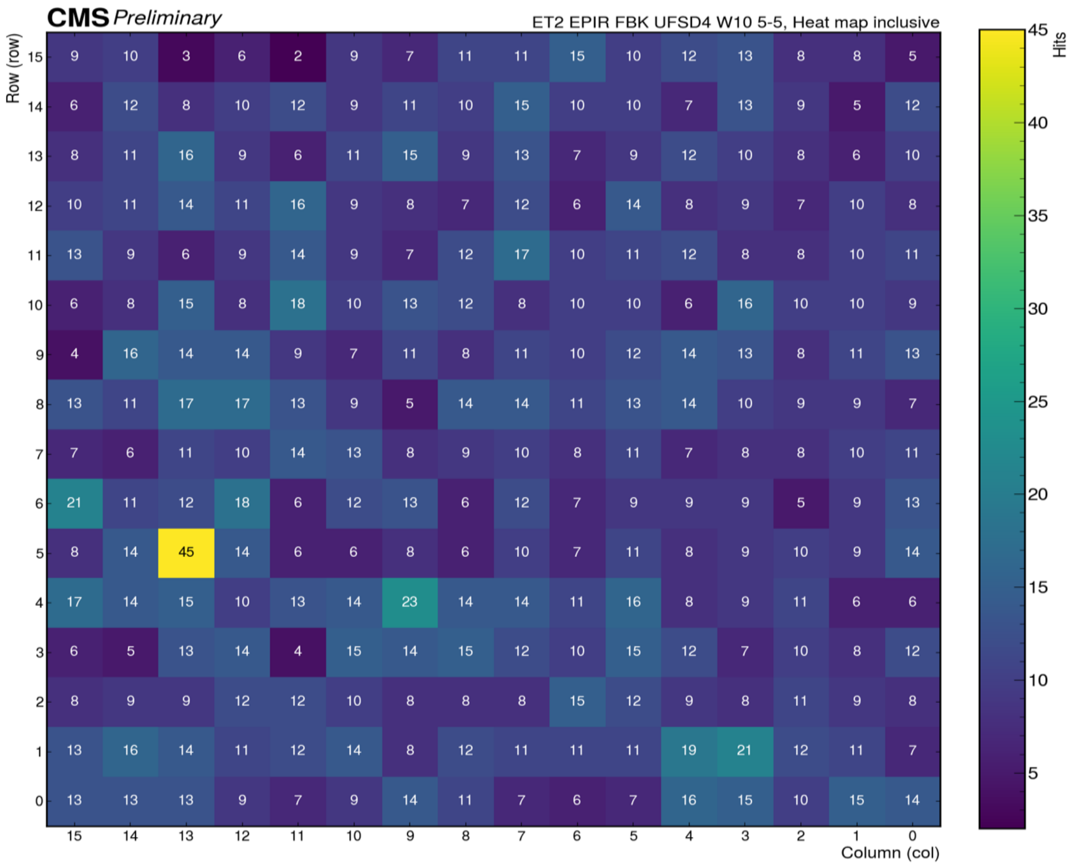


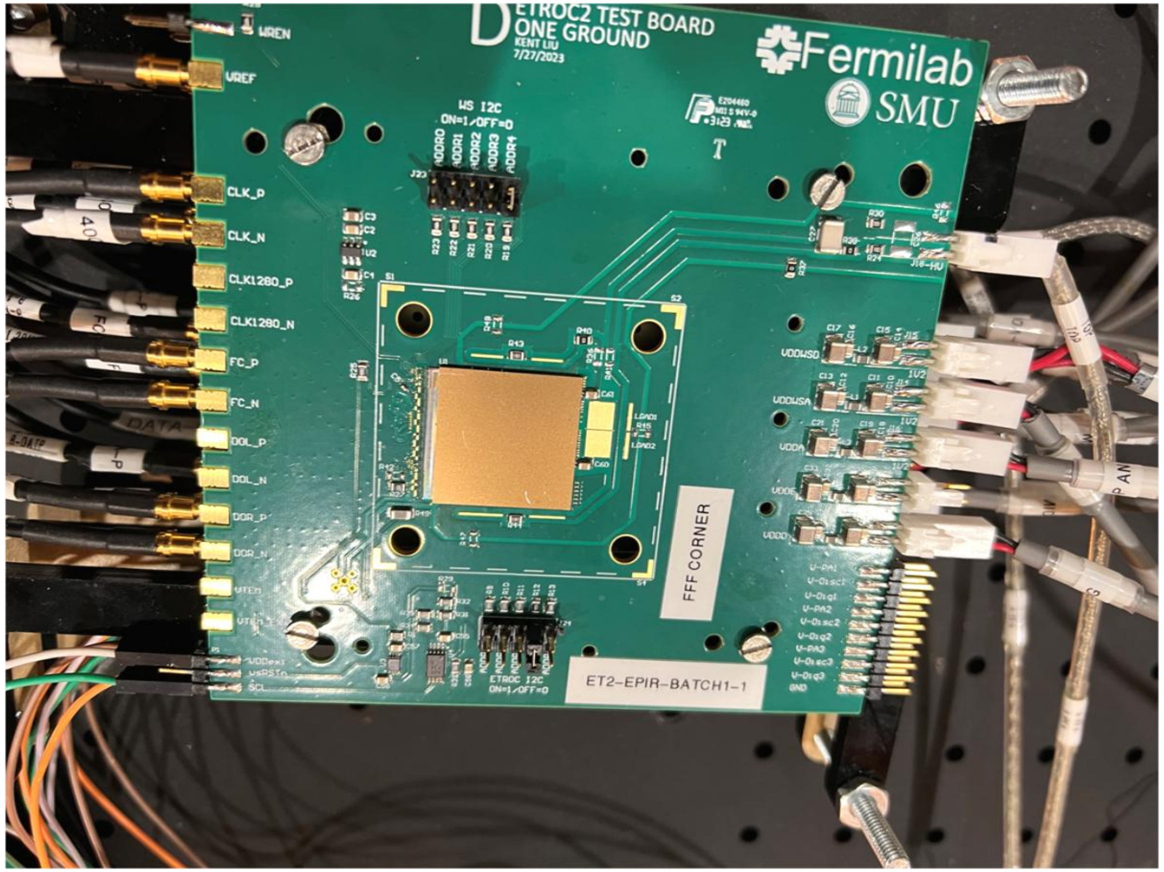




- Baseline and noise width
  - Center: Preamp output baseline calibration for all 256 pixels, with sensor biased at 250V.
  - Right: Noise width for each pixels with sensor biased at 250V.

EARLY DEMONSTRATION OF VTROC (2D) – COSMIC RAY

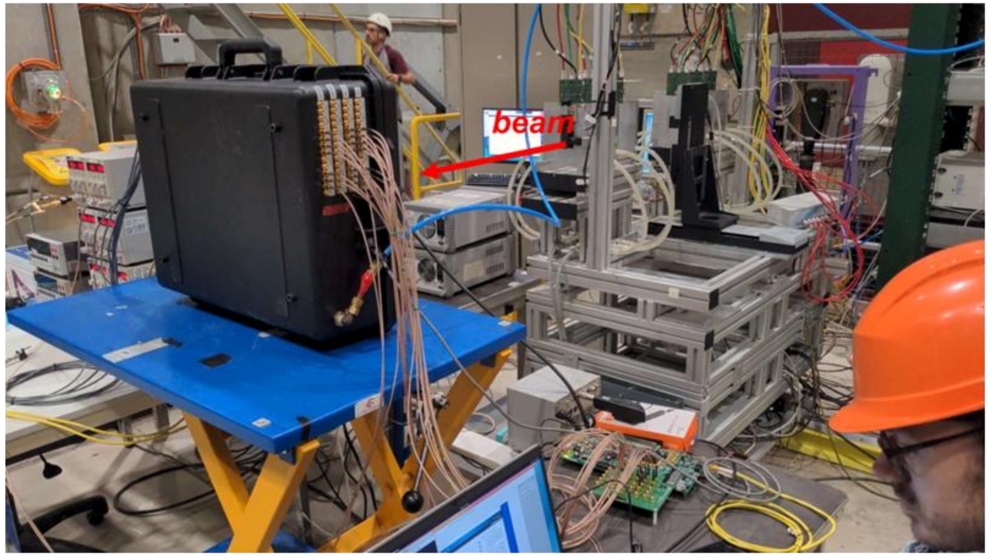




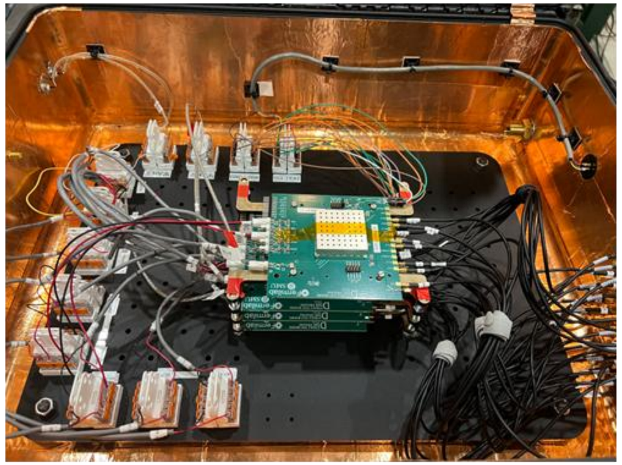
- Cosmic ray run
  - The chip is configured to be able to self-trigger on any pixel hit to capture cosmic rays.
  - Run overnight for 15 hours, expect about ~ 10 hits per pixel.
  - All 256 pixels are connected with sensor properly based on the hit map after 15 hours exposure.

EARLY DEMONSTRATION OF VTROC (2D) – BEAM TEST (CERN)

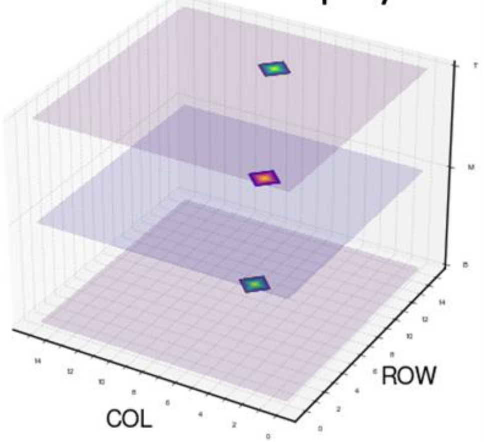
- 120 GeV hadron beam (proton and pion)



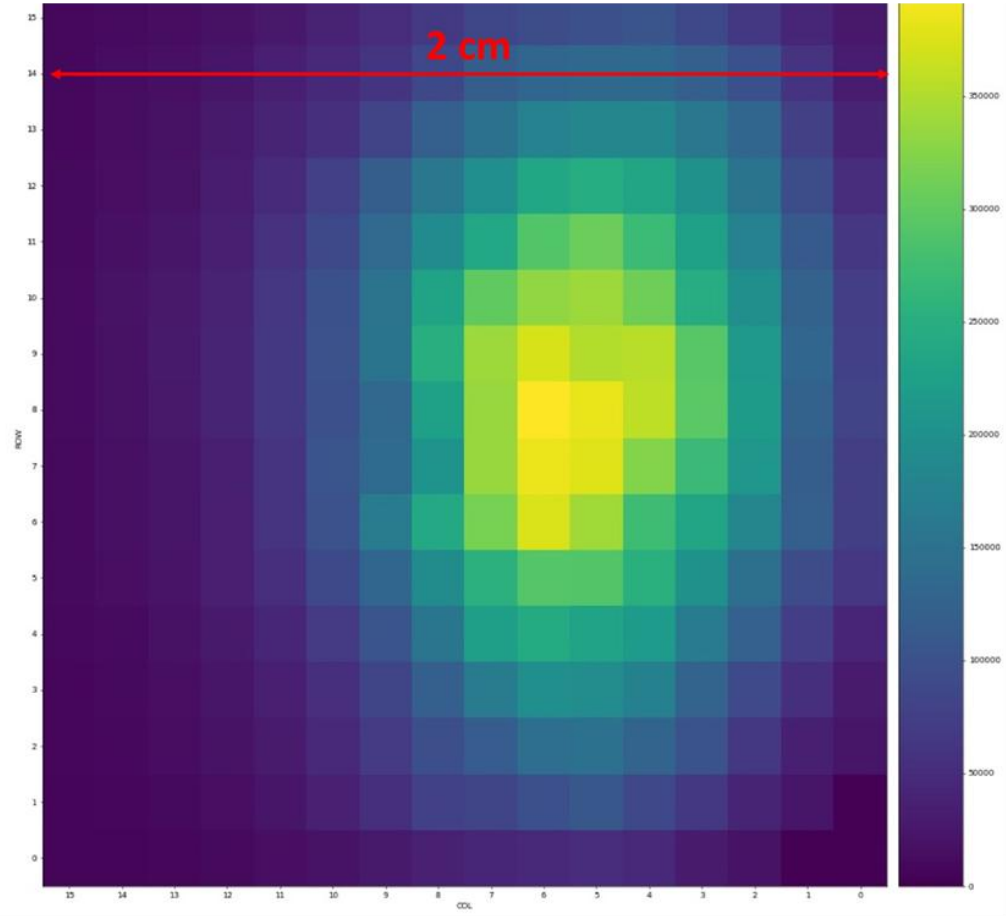
- Three layers of ETROC2 + sensor telescope



Event display



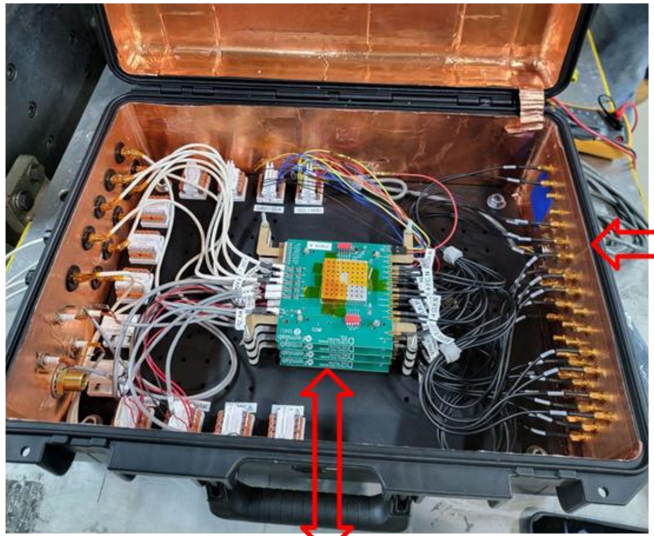
- Beam spot seen by EPIR bump bonded chip (as trigger board)

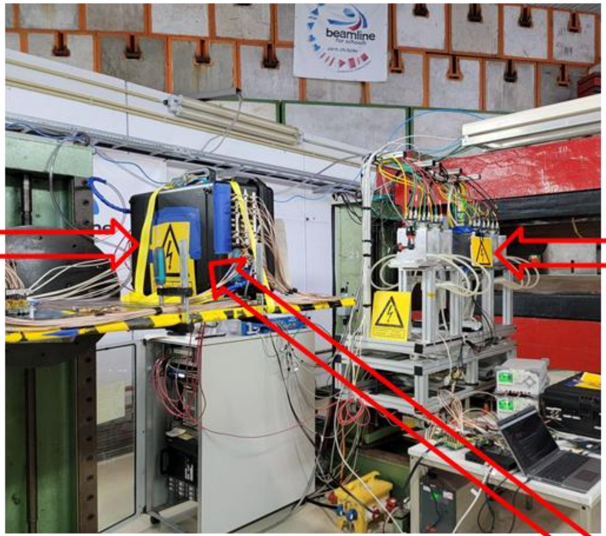


- This is the beam spot observed by EPIR bump bonded board.
- CERN hadron beam spot core size is 1cm × 1cm.
- Worked well on the first try, self triggered.

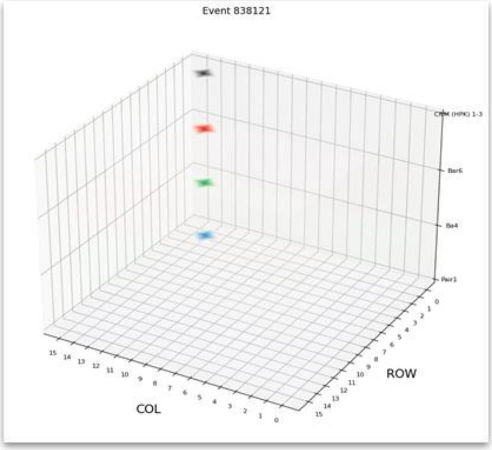
EARLY DEMONSTRATION OF VTROC (2D) – BEAM TEST (DESY)

The first beam test at DESY for ETROC2 with electron beam (with two independent setups)



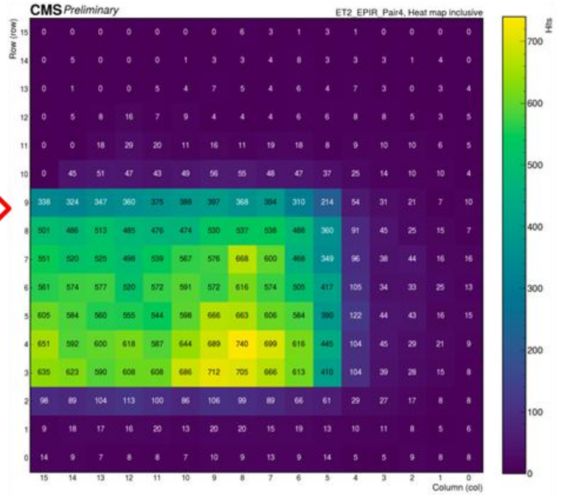


- Four layer of ETROC2+sensors in the Beam telescope (event display)

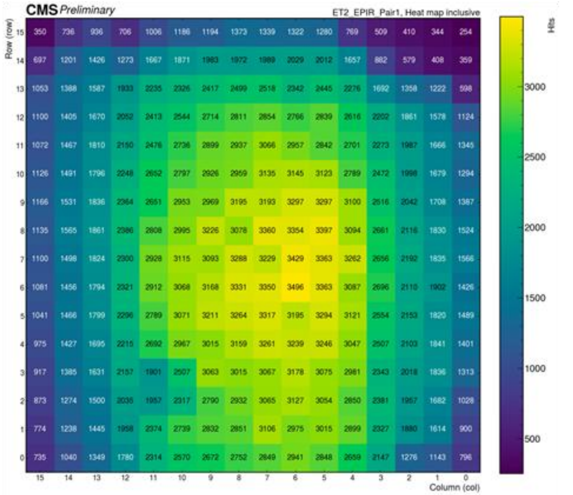


- DESY electron beam spot size is about 2 cm × 2 cm.
- The four-layer ETROC telescope is triggered by EPIR pair 1 chip.

- EPIR Pair 4 integrated with AIDA telescope, triggered by AIDA scintillators (smaller size)



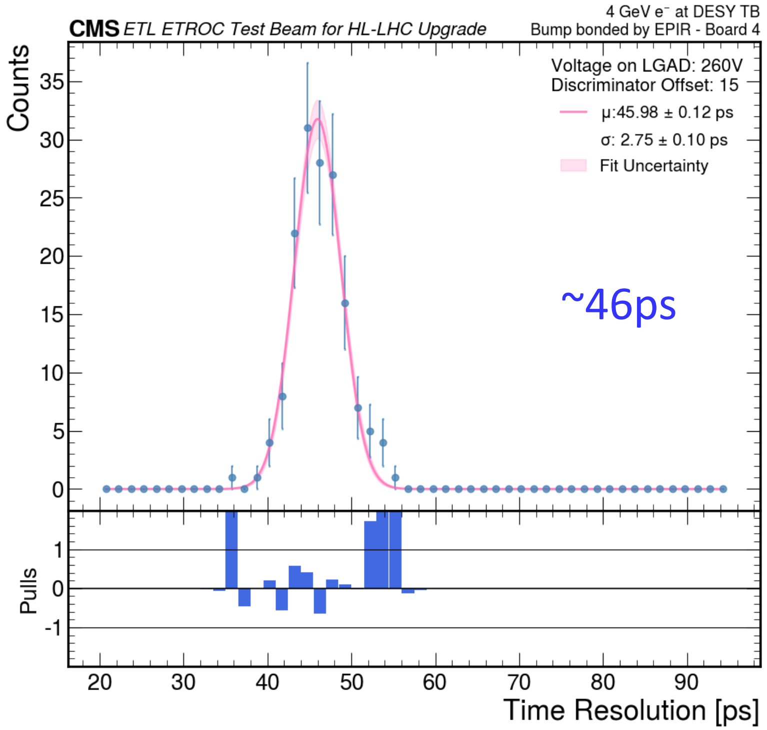
- Beam spot seen by ETROC2, self triggered with EPIR Pair 1



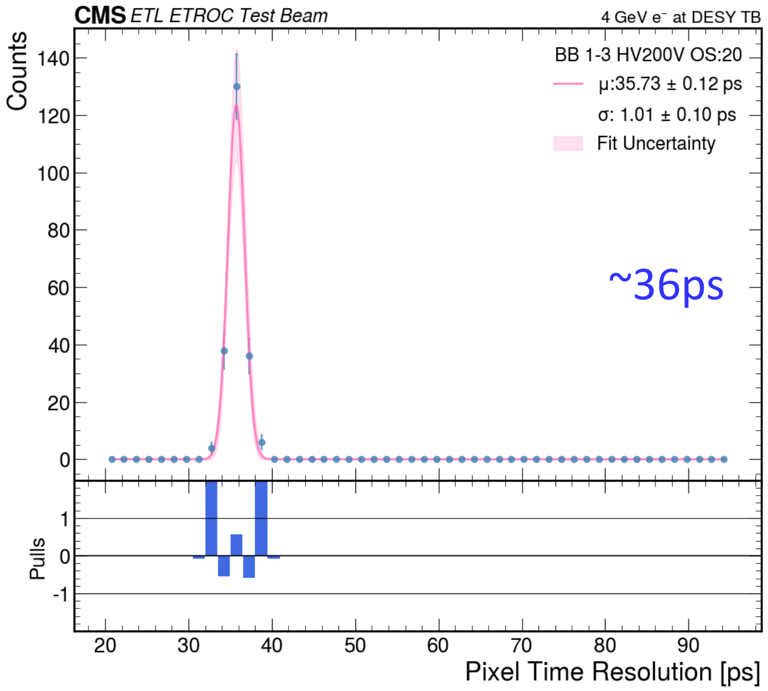
EARLY DEMONSTRATION OF VTROC (2D) – TIMING RESOLUTION

- Dozens of sensor-readout chip assemblies were integrated for testing

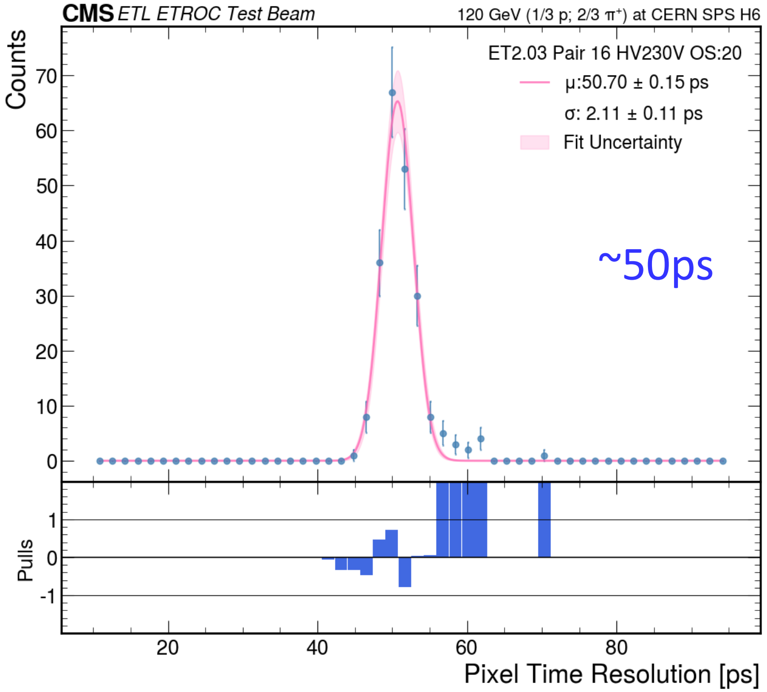
Type 1



Type 2



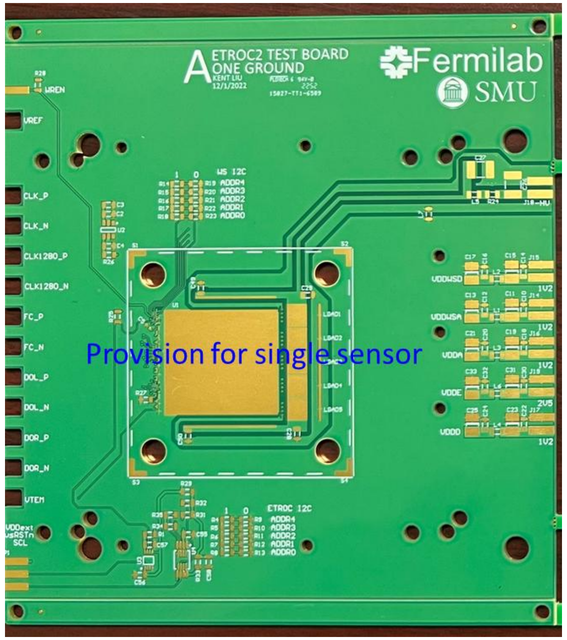
Type 3

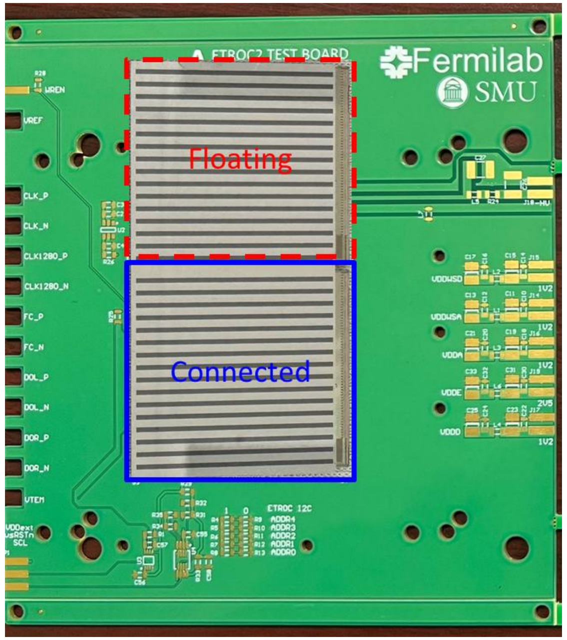


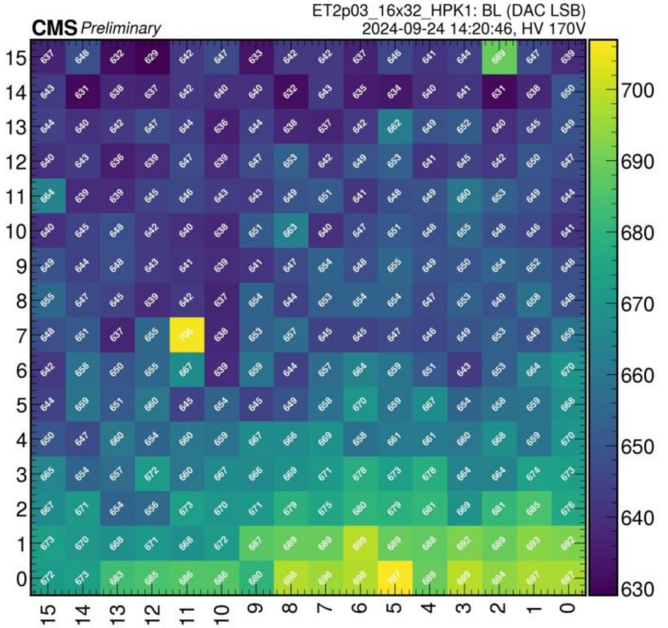
- Integrated assemblies are operated at optimum sensor bias
  - Beyond which the sensor will be in breakdown
- Timing resolution is limited by sensor performance

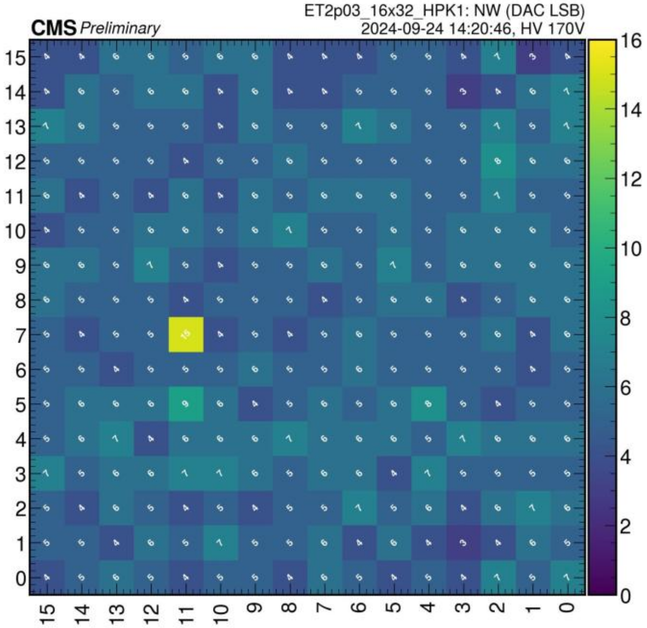
EARLY DEMONSTRATION OF VTROC (2D) – MULTI-CHIP ASSEMBLY

- Basic functionality test
  - Pream output
  - Noise width



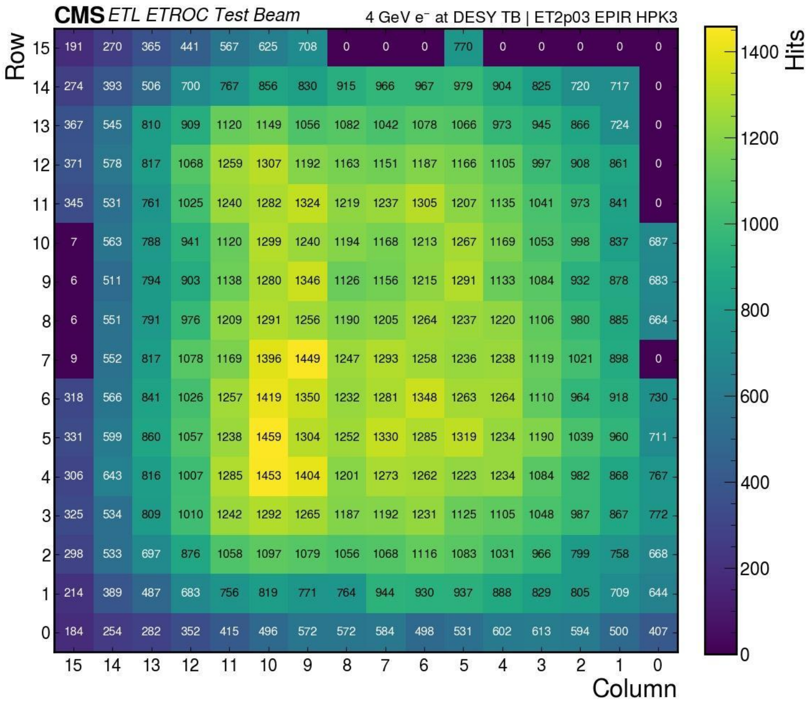




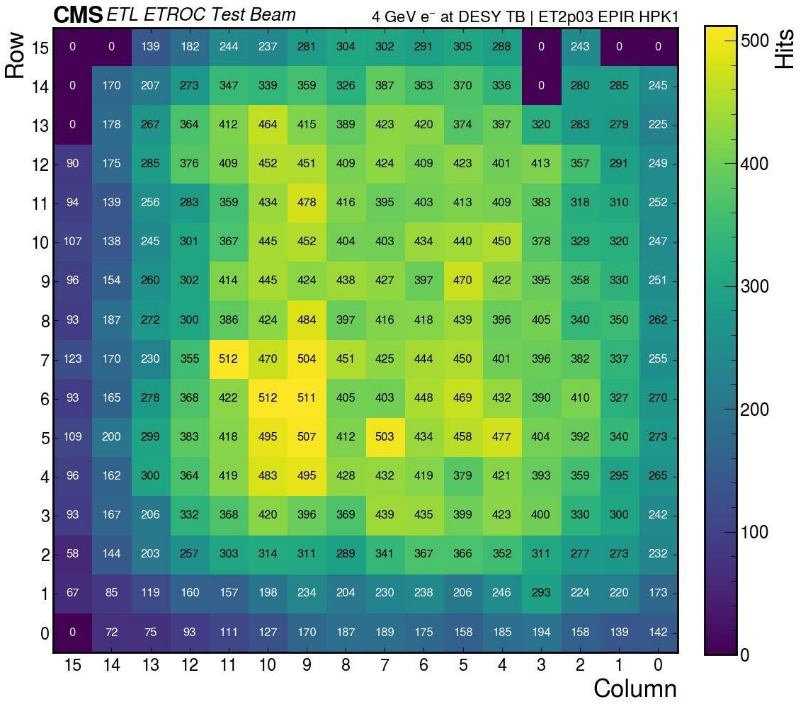


EARLY DEMONSTRATION OF VTROC (2D) – MULTI-CHIP ASSEMBLY BEAM TEST (DESY)

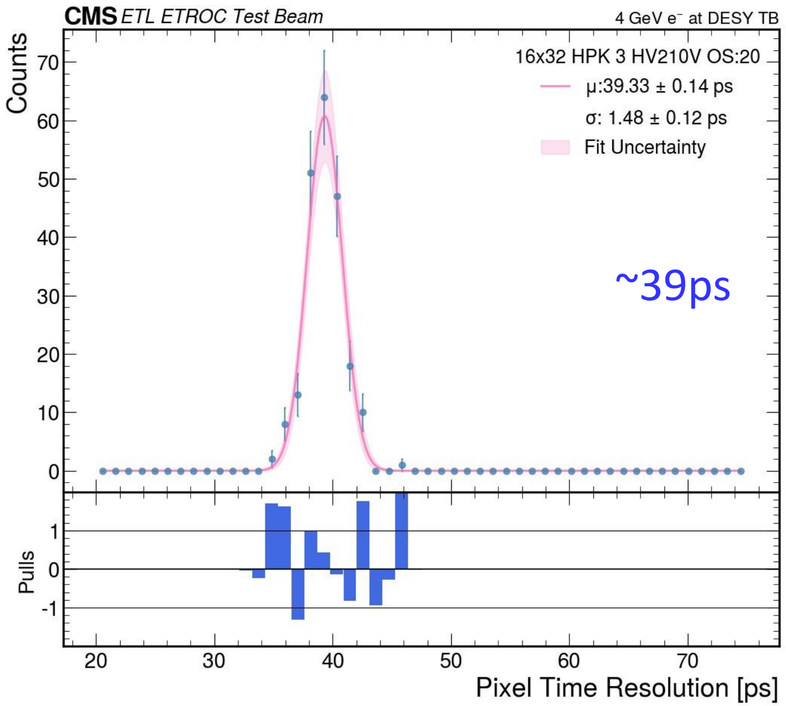
Multi-sensor assembly 1



Multi-sensor assembly 2



Timing resolution



- A minor performance degradation when compared to the timing resolution obtained from the earlier assemblies.
- This observed discrepancy can be attributed to an increased noise level originating from the floating configuration of the sensor-chip assembly.

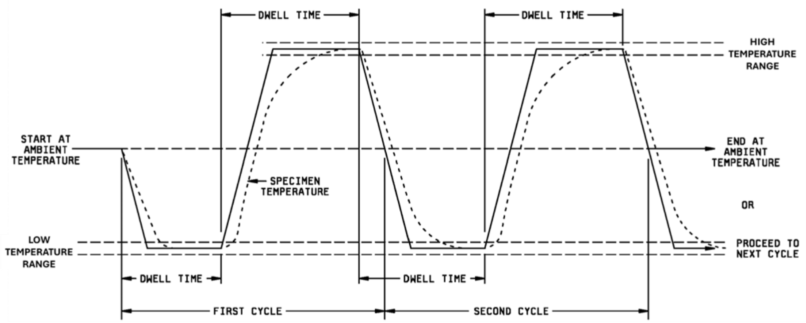
ONGOING EFFORTS

Technical

- Neutron irradiation study
  - Understanding/validating effects of irradiation on integrated assemblies

Fluence ($\times10^{15}$)	Die ID
0.2	W8-23, W8-24
0.5	W8-1, W8-2, W8-3, W8-4
1	W8-5, W8-7, W8-8, W8-9, TS1-W7
1.5	W8-10, W8-11, W8-12, W8-13
2	W8-14, W8-15, W8-16, W8-17, W8-18
3	W8-19, W8-29, W8-21, W8-22

- Reliability test under thermal cycling



Commercialization

- DOE customers
  - National Laboratories
    - Fermilab
    - Berkeley Lab
    - Facility for Rare Isotope Beams
    - Jefferson Lab
  - International Laboratories
    - CERN, Switzerland
    - DESY, Germany
- Seeking non-DOE customers
  - Have identified development partners
- Future development
  - Fundraising

Opportunity scouting

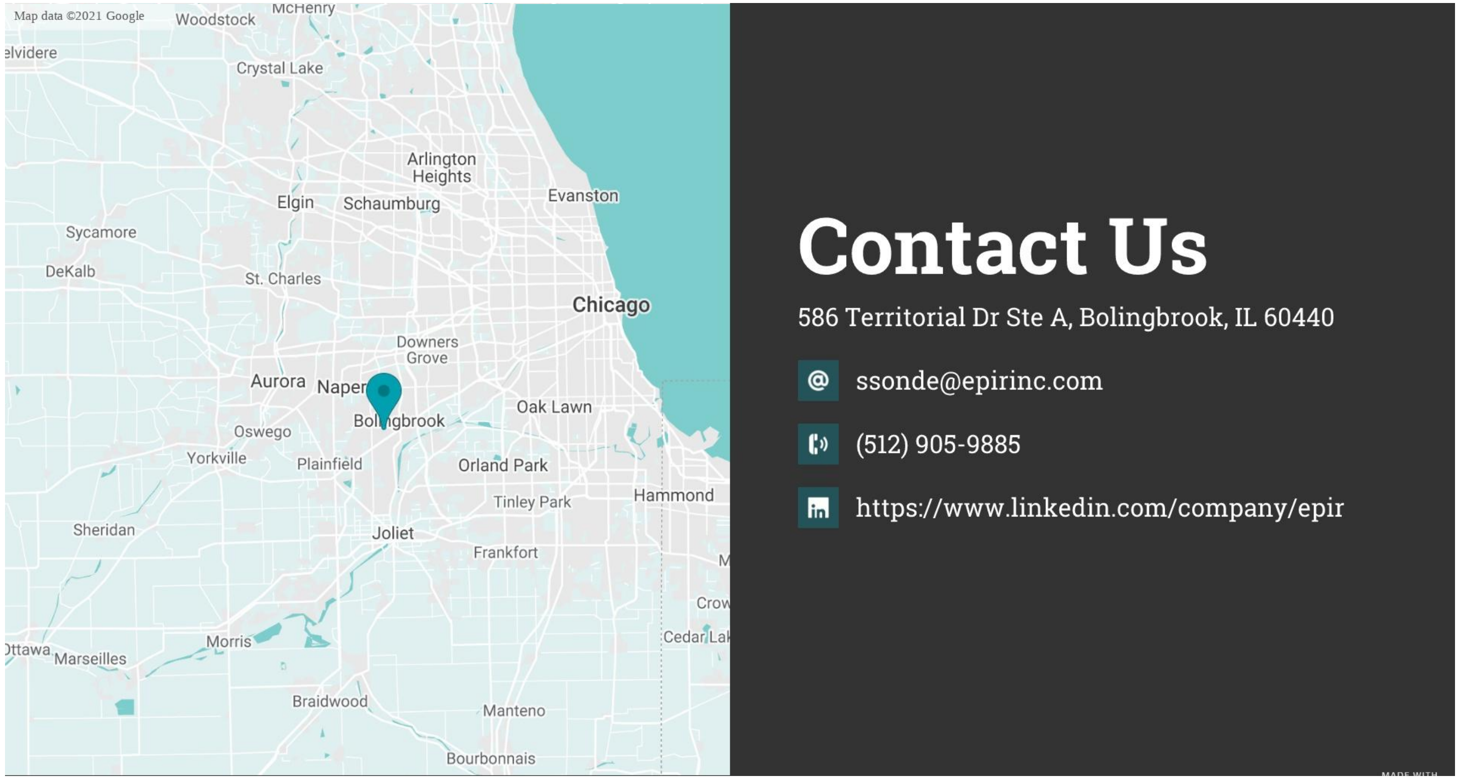
- Leveraging the high timing resolution and high spatial resolution platform for potential applications

a. A solid-state, scalable detector for neutron radiography.
   - Planar fabrication technology

b. High-resolution airborne tomographic LiDAR system
   - High-fidelity readout circuit receiver platform
   - Potential to enable centimeter-scale resolution

SUMMARY & OUTLOOK

- ASIC design
  - Completed 3-tier reduced footprint designs
  - TSV scheme optimized
- Integration scheme development
  - Demonstrated die-to-die and die-to-wafer integration scheme
  - DBI – 50µm, conventional high-density bumps – 8µm pitch
  - Alignment accuracy – 500nm
- Testing and validation
  - 100%-pixel bonding yield verified
  - Verified timing resolution ~36ps
- Outlook
  - Neutron irradiation study
  - Thermal cycling reliability
  - Opportunity scouting



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Thank you.