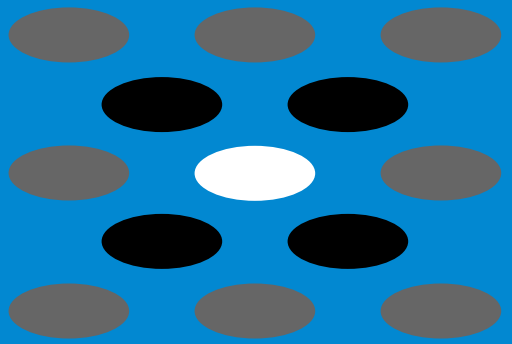


CAPORUS
TECHNOLOGIES

Novel Insulators in Silicon-on-Insulator Substrates to Improve Nuclear Physics Sensors and Circuits

July 29, 2025

Intro to Caporus & NLP™

Silicon on Insulator for NP

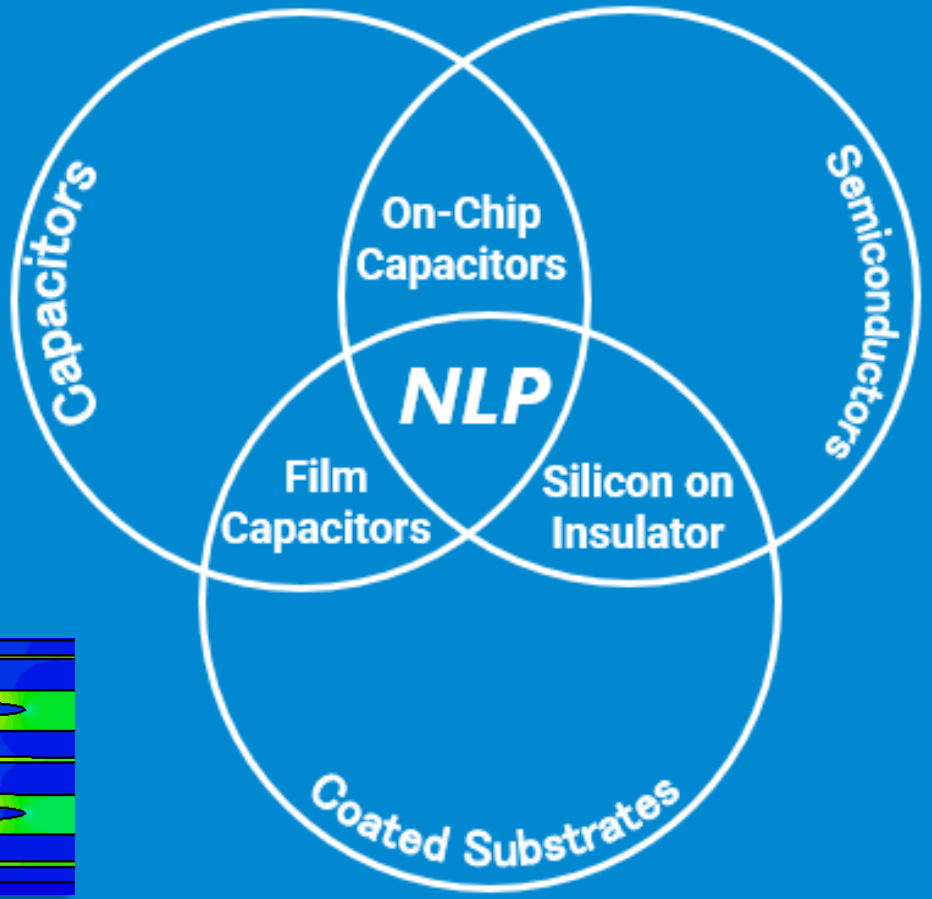
Phase II Demonstration

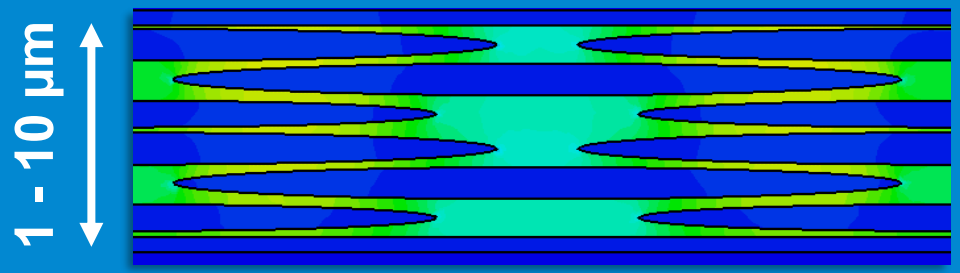
Caporus NLP™

CAPORUS TECHNOLOGIES

Nanoscale Lamellar Porosity™ (NLP™)

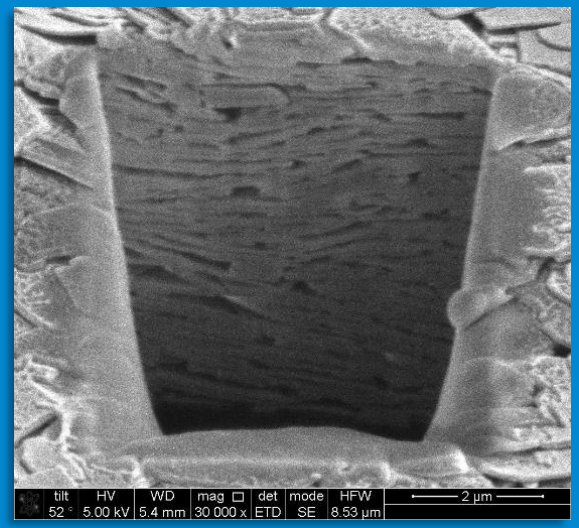
Controls the electric field distribution within a porous ceramic or semiconductor structure





illustration

Ceramic matrix (blue)
Porous regions (green)

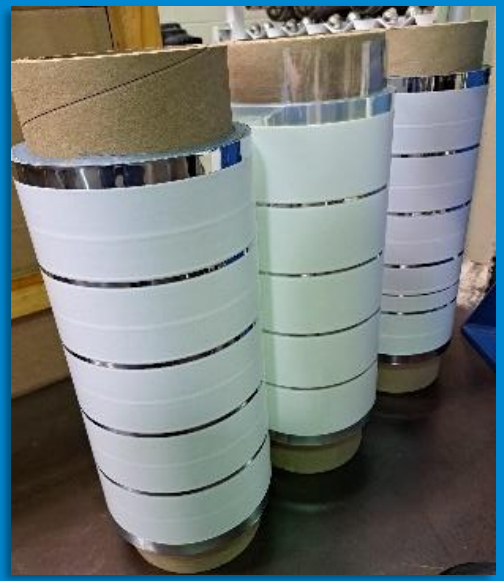


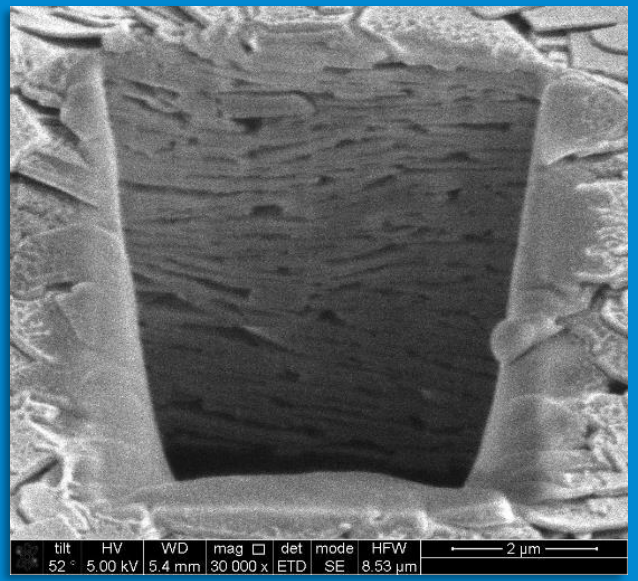
FIB image of material

NLP™ Technology | Production at Scale

Large Scale Slurry Production

High-Volume
Roll-to-Roll Manufacturing

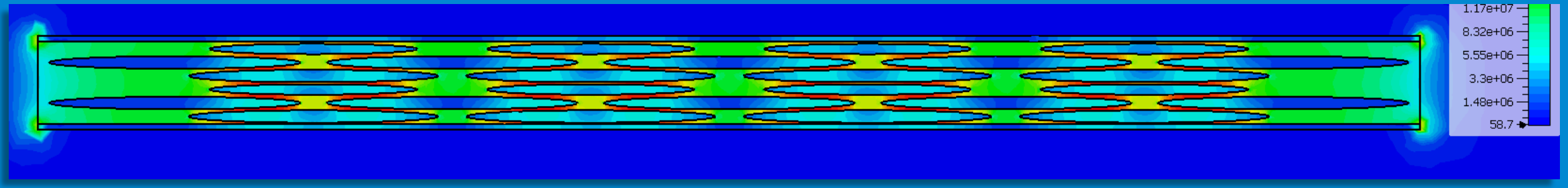




Nanoscale Lamellar Porosity over
Large Areas

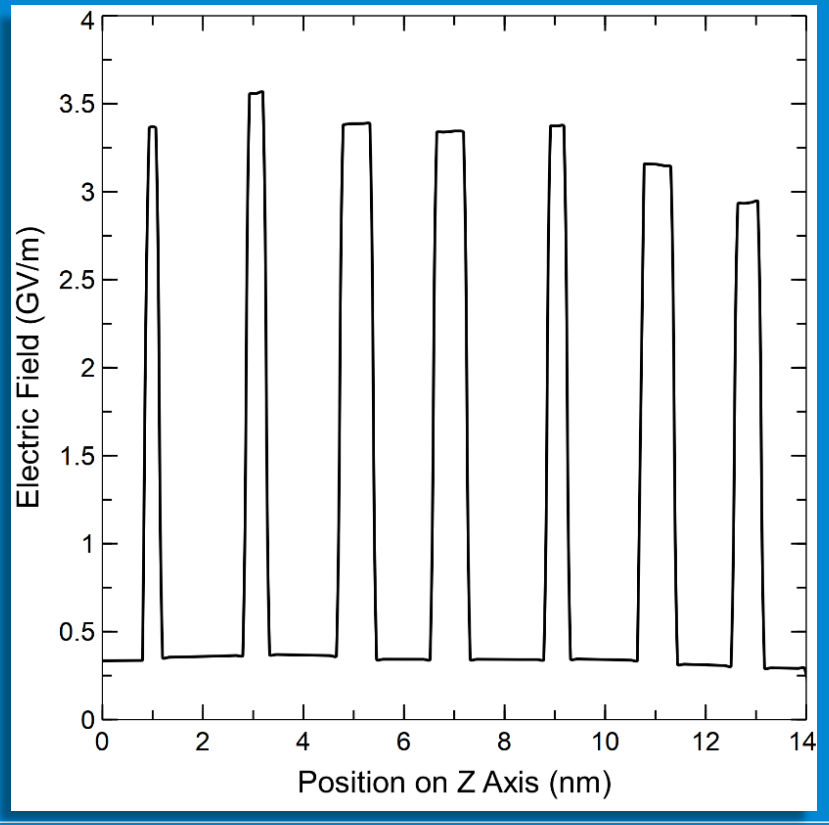
Slurry-based coating for R2R deposition of ceramic coating - No sintering required

NLP™| Technology Overview



Caporus' Proprietary Nanoscale Lamellar Porosity

- Structured porosity for electric field engineering
- ***Layered structure → redistribution of electric fields***

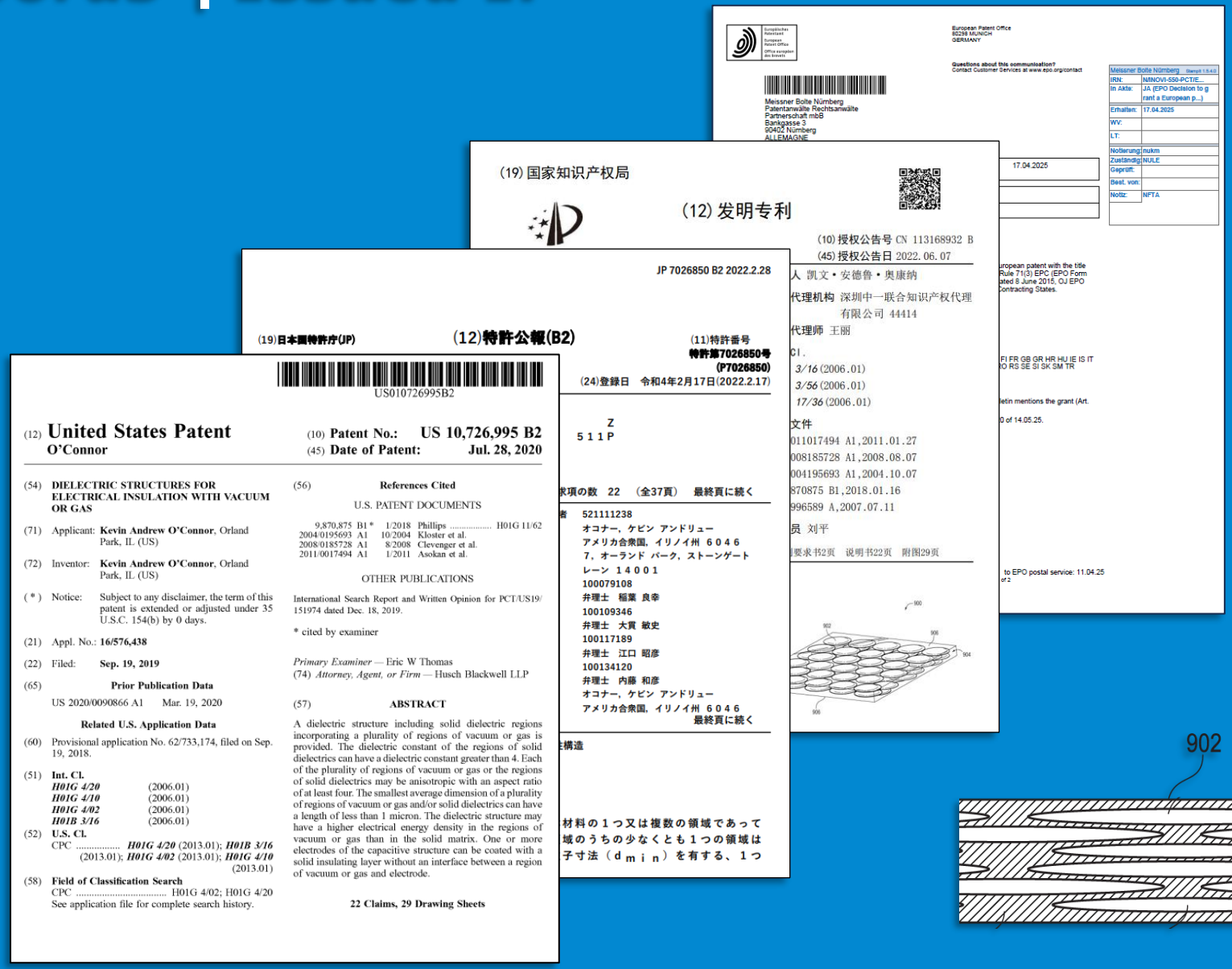


Caporus | Issued IP

CAPORUS TECHNOLOGIES

USPTO *issued July 2020*
JPO *issued March 2022*
CNIPA *issued June 2022*
EPO *issued May 2025*

Note: additional patents pending



(12) **United States Patent**
O'Connor

(10) **Patent No.: US 10,726,995 B2**
(45) **Date of Patent: Jul. 28, 2020**

(54) **DIELECTRIC STRUCTURES FOR ELECTRICAL INSULATION WITH VACUUM OR GAS**

(71) Applicant: **Kevin Andrew O'Connor**, Orland Park, IL (US)

(72) Inventor: **Kevin Andrew O'Connor**, Orland Park, IL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **16/576,438**

(22) Filed: **Sep. 19, 2019**

(65) **Prior Publication Data**

US 2020/0090866 A1 Mar. 19, 2020

Related U.S. Application Data

(60) Provisional application No. 62/733,174, filed on Sep. 19, 2018.

(51) **Int. Cl.**
H01G 4/20 (2006.01)
H01G 4/10 (2006.01)
H01G 4/02 (2006.01)
H01B 3/16 (2006.01)

(52) **U.S. Cl.**
CPC ***H01G 4/20*** (2013.01); ***H01B 3/16*** (2013.01); ***H01G 4/02*** (2013.01); ***H01G 4/10*** (2013.01)

(58) **Field of Classification Search**
CPC H01G 4/02; H01G 4/20
See application file for complete search history.

(56) **References Cited**

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2004/0195693 A1 10/2004 Kloster et al.
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OTHER PUBLICATIONS

International Search Report and Written Opinion for PCT/US19/151974 dated Dec. 18, 2019.

* cited by examiner

Primary Examiner — Eric W Thomas
(74) *Attorney, Agent, or Firm* — Husch Blackwell LLP

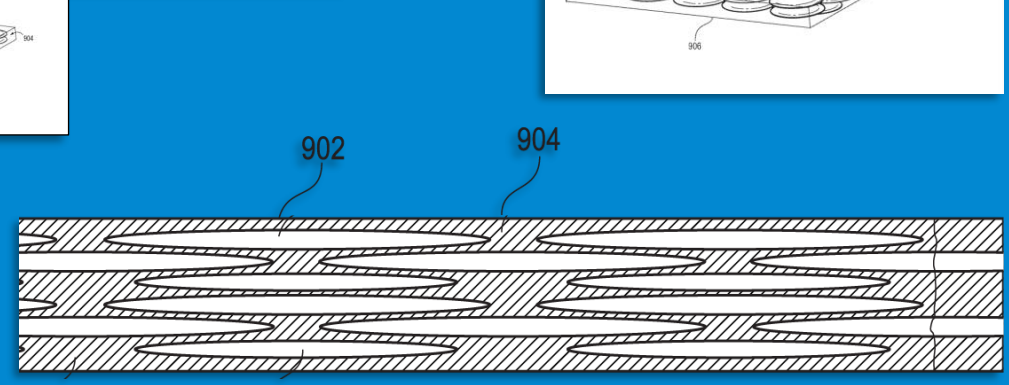
(57) **ABSTRACT**

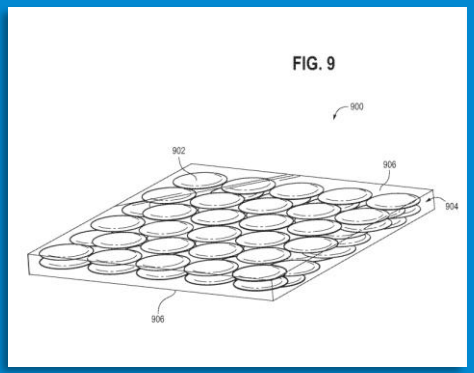
A dielectric structure including solid dielectric regions incorporating a plurality of regions of vacuum or gas is provided. The dielectric constant of the regions of solid dielectrics can have a dielectric constant greater than 4. Each of the plurality of regions of vacuum or gas or the regions of solid dielectrics may be anisotropic with an aspect ratio of at least four. The smallest average dimension of a plurality of regions of vacuum or gas and/or solid dielectrics can have a length of less than 1 micron. The dielectric structure may have a higher electrical energy density in the regions of vacuum or gas than in the solid matrix. One or more electrodes of the capacitive structure can be coated with a solid insulating layer without an interface between a region of vacuum or gas and electrode.

22 Claims, 29 Drawing Sheets

(19)日本国特許庁(JP)　(12)特許公報(B2)　(11)特許番号 特許第7026850号 (P7026850)
JP 7026850 B2 2022.2.28
(24)登録日　令和4年2月17日(2022.2.17)

(19) 国家知识产权局　(12) 发明专利
(10) 授权公告号 CN 113168932 B
(45) 授权公告日 2022.06.07

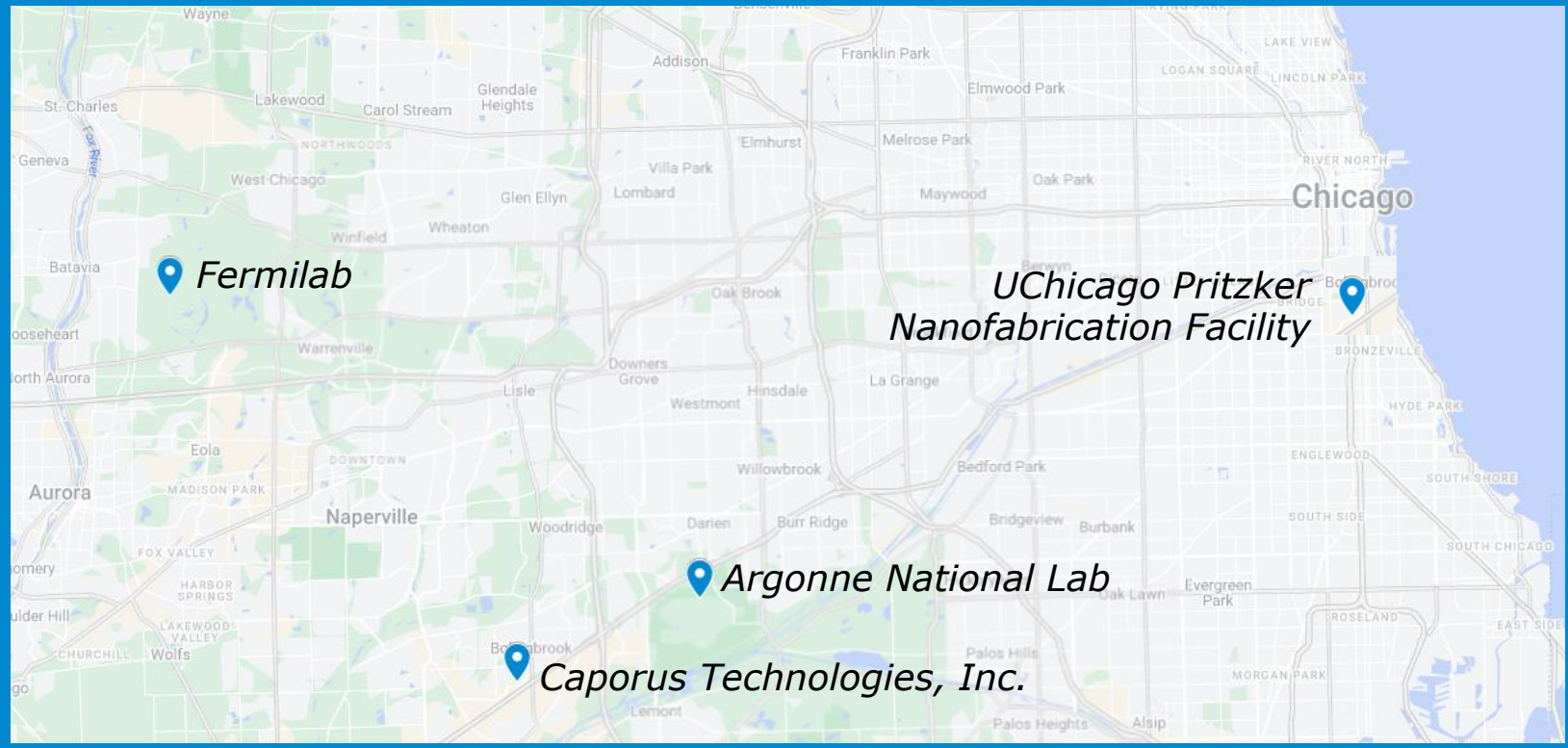




CAPORUS TECHNOLOGIES

CHAIN REACTION INNOVATIONS
Entrepreneurship at Argonne

Caporus is located near Fermilab and Argonne in Southwest Chicagoland



Caporus was previously embedded at Argonne through the Chain Reaction Innovations program. Operations are headquartered between Argonne and Fermilab.

Intro to Caporus & NLP™

Silicon on Insulator for NP

Phase II Demonstration

Silicon on Insulator (SOI)

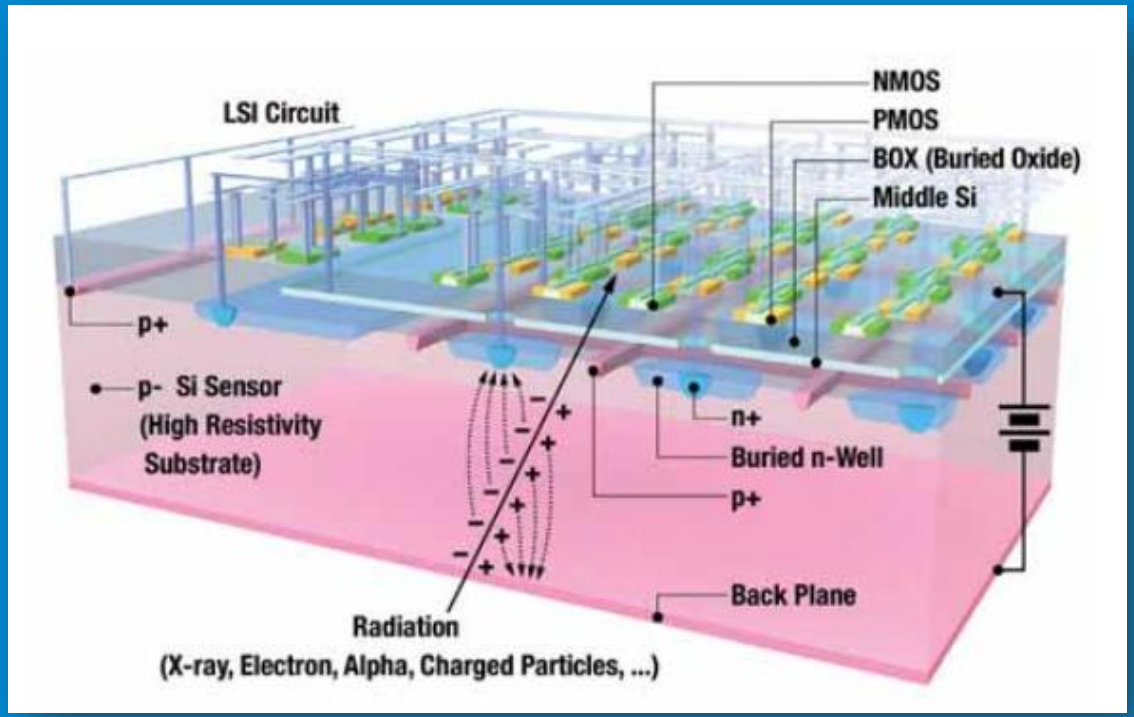
Commercial RF-SOI Substrate Structure

Image from SOITEC

SOI Advantages	SOI Disadvantages
Superior Single Event Upset Tolerance	Total Ionizing Dose Issues (Charge Effects)
Better Noise Isolation	Radiation Damage to BOX
Speed	Back-gate Effect due to Field Applied in Sensor
Density	Coupling of Charges in BOX and sensor

Improved SOI for MAPS

- Reduce unwanted coupling between substrate and front-end electronics
  - Reduced back-gate effect
  - Improve sensitivity
  - Reduce noise
- Elimination of inversion layer effects
  - Enable depletion with applied electric field
  - Improve sensitivity
- Improved radiation hardness
  - Lower radiation cross-section
  - Reduced coupling decreases effects of trapped charges

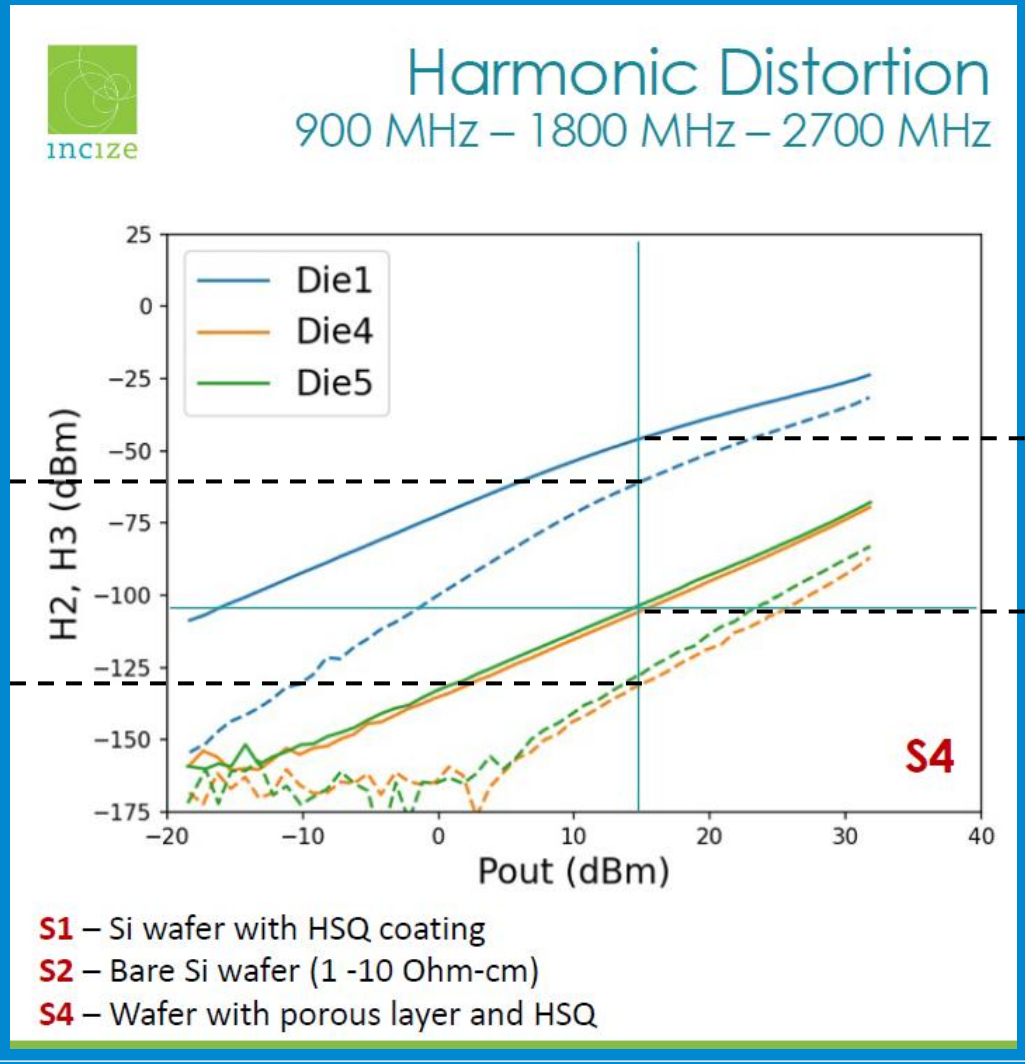


SOIPIX – 2016 KEK Annual Report

Early Development - Third-Party RF Testing

Third-Party testing has verified > 50 dBm reduction in 2nd and 3rd harmonic distortion through the addition of Caporus' porous materials.

> 50 dBm reduction of 3rd harmonic



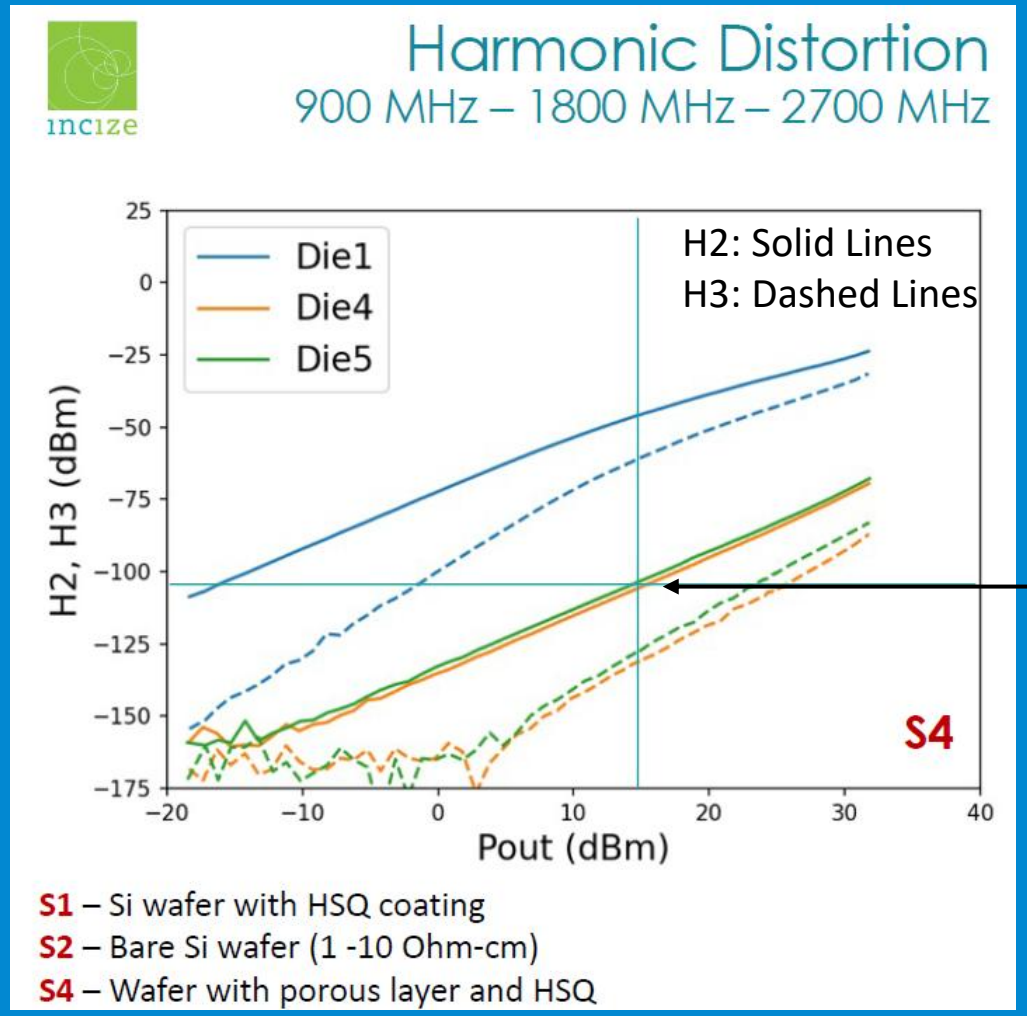
> 50 dBm reduction of 2nd harmonic

Early Development - Third-Party RF Testing

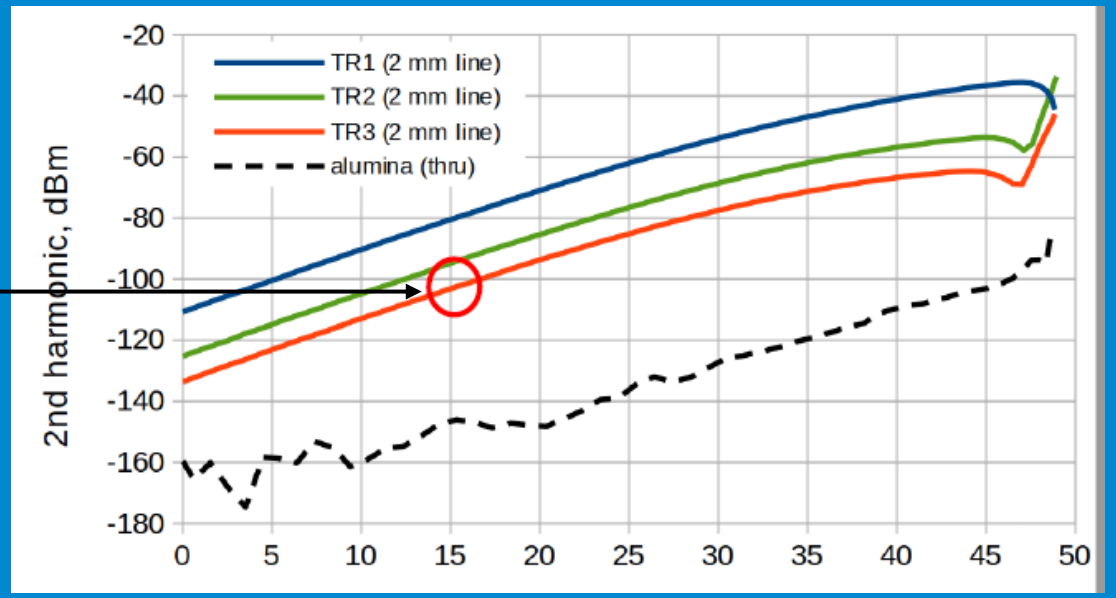
CAPORUS TECHNOLOGIES

Demonstrated Performance with Lower Cost Substrates

Wafers Without (Blue) and With (Green) Caporus' Porous Layer



Current State-of-the-Art High Resistivity, Trap-Rich Wafers



Intro to Caporus & NLP™

Silicon on Insulator for NP

Phase II Demonstration

Phase II Project Summary

- Priorities from Solicitation
  - Next generation of monolithic active pixel sensors (MAPS)
  - Radiation hardness (EIC luminosity of 10^{33} – 10^{34} $cm^{-2}s^{-1}$)
  - Apply E-field to substrate to fully deplete detection volume

- Proposed Technology
  - Implement MAPS on SOI
  - Improved single-event upset, better noise isolation, speed, and density compared to bulk process
  - Modified SOI with porous Si below BOX
    - Reduce capacitive coupling between Si layers (Lower ε_{eff} and greater non-BOX thickness of porous Si)
    - Reduce trapped charge in BOX with modified substrate
    - Eliminate parasitic conduction layer at interface of BOX and bulk Si (Trap-rich)

- Phase II Demonstration
  1. Scale processes for radiation testing
  2. Etching processes for porous layer
  3. Design CMOS and test structures
  4. Fabricate test devices
  5. Test for radiation hardness
     - With and without proprietary modification
     - Before and after irradiation

Phase II Resources

Phase II Team

- Caporus Technologies
  - Kevin O'Connor (PI)
  - Nikki Chang
  - Karabi Mondal
  - Eric Acosta
  - Bill Fortino
  - Michael Boehme
  - Jim Cable (Consultant - SOI Development and Commercialization)
  - Francis Chapman (Consultant - Materials Development)
- Subaward
  - Fermi National Accelerator Laboratory
    - Xiaoran Wang, Farah Fahim, Davide Braga (SOI – MAPS Design, Irradiation, Device Testing)

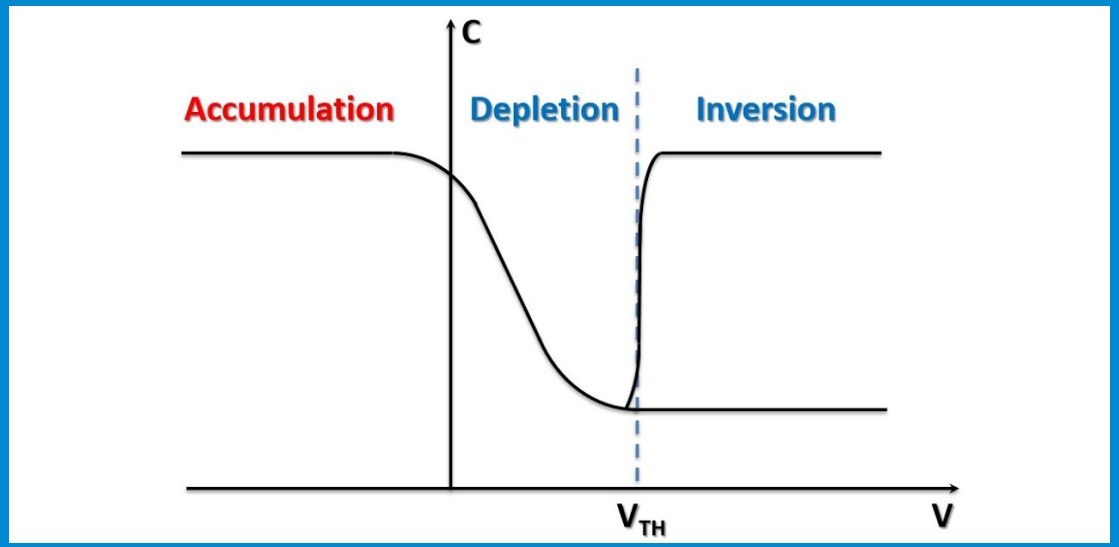
Additional Resources

- Foley and Lardner (TABA)
  - IP: USPTO and PCT applications
  - Contracts: Commercial engagement – pilot and license
- External Facilities
  - Argonne Center for Nanoscale Materials (CNM)
  - UChicago Pritzker Nanofabrication Facility
  - Northwestern Medicine Proton Center
- Carl Traynor (Consultant - Commercialization)

Radiation Testing: MOS Capacitor

MOS Capacitor

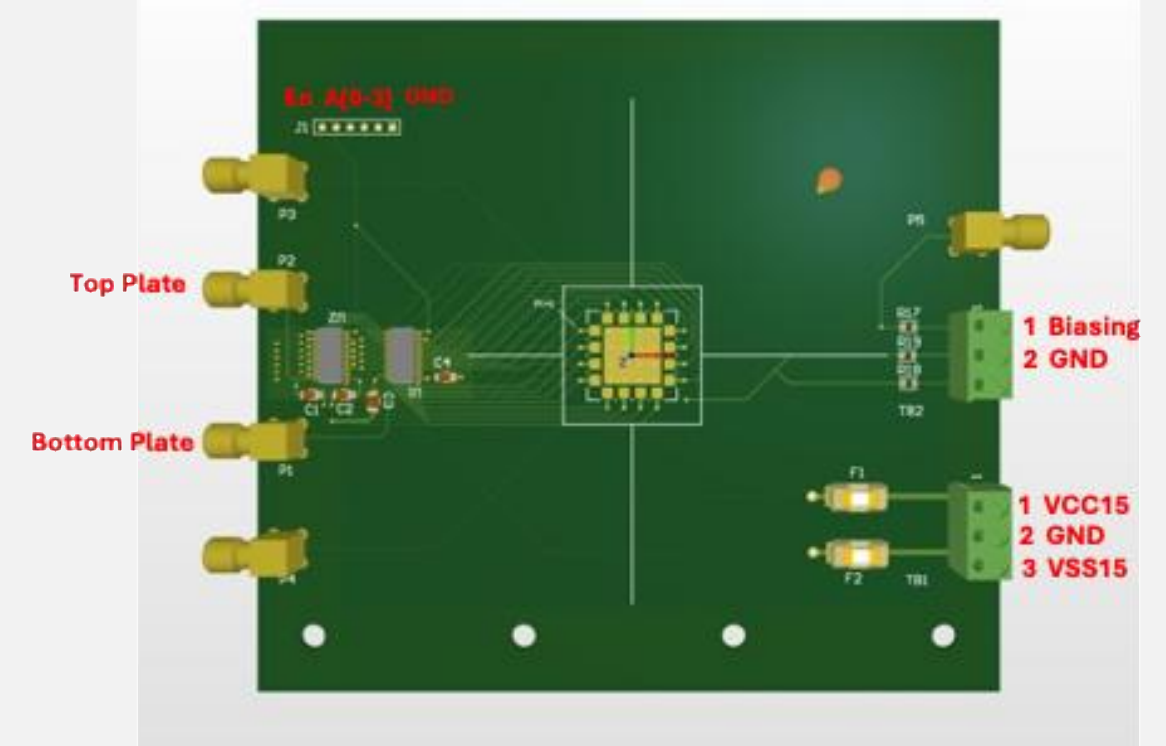
- C-V sweep
  - Accumulation, depletion, and inversion
  - Identify flatband voltage, threshold voltage
    Measurements are sensitive to trapped charge in the oxide
- Shift in the C-V curve enables comparison of ionization radiation damage due to trapped charge accumulation

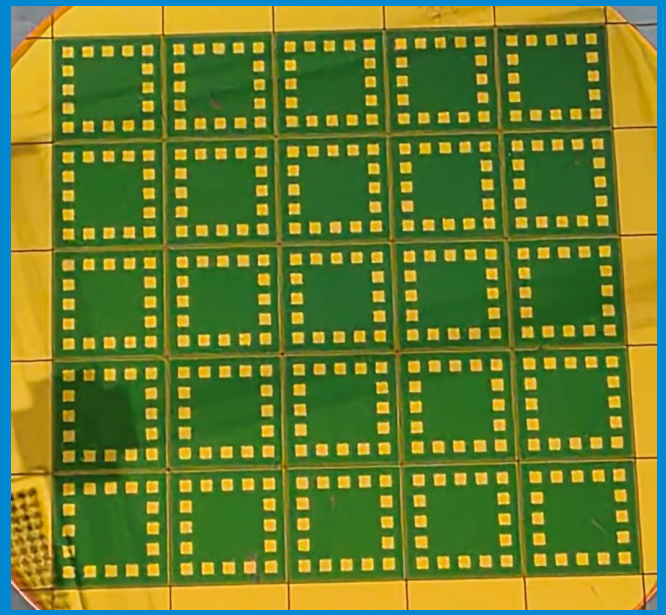


Radiation Testing: MOS Capacitor

SOI Dies

- 16 MOS capacitors per die
- Common proprietary modification for all 16 devices per die
  - 4 implementations of porosity across all dies
- Fabricated by Caporus

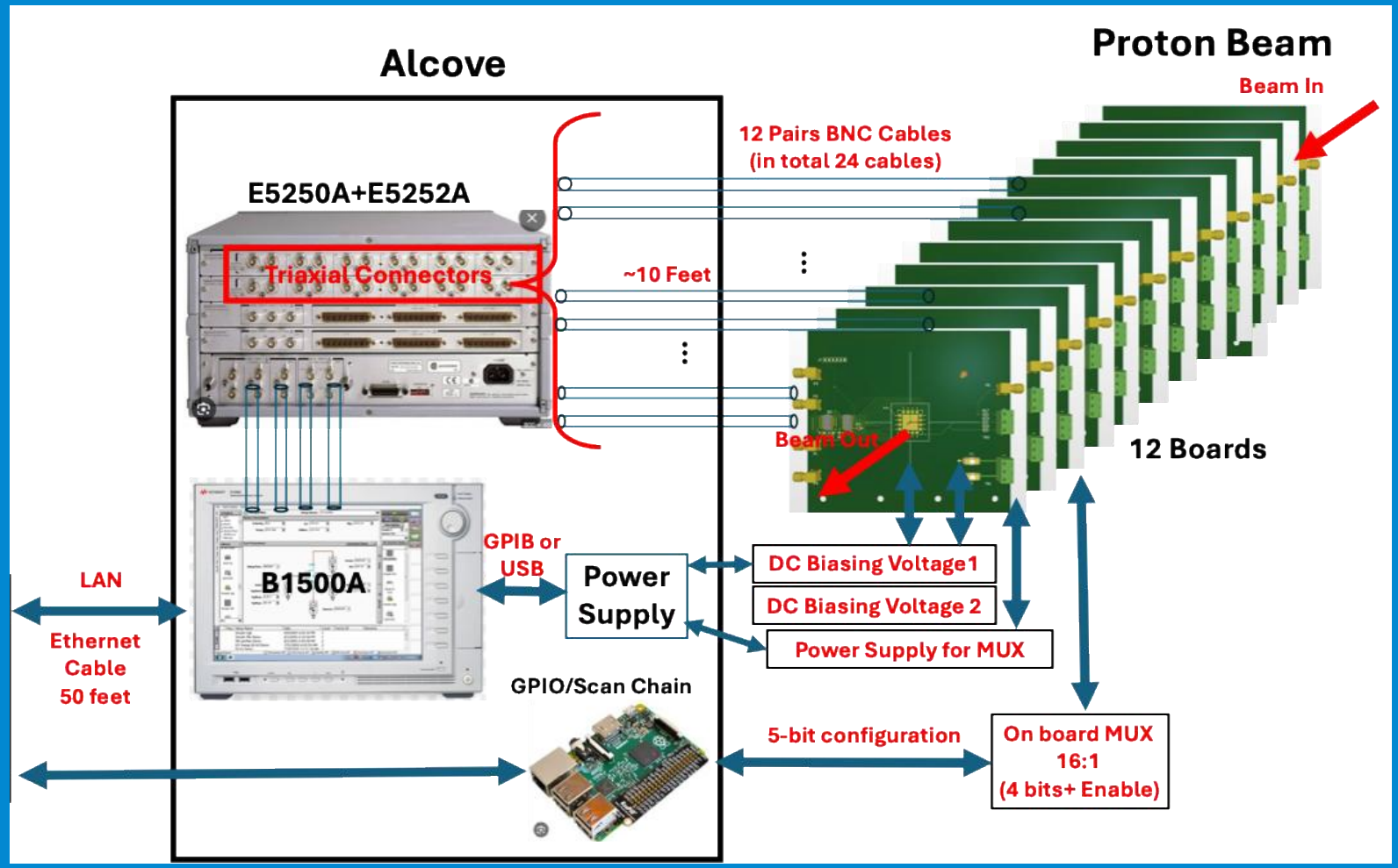




Test Boards

- 1 SOI die per board
- Onboard multiplexer selects between 16 devices
- Single bias voltage per board
- Fabricated by Fermilab

Radiation Testing: MOS Capacitor



Test Setup

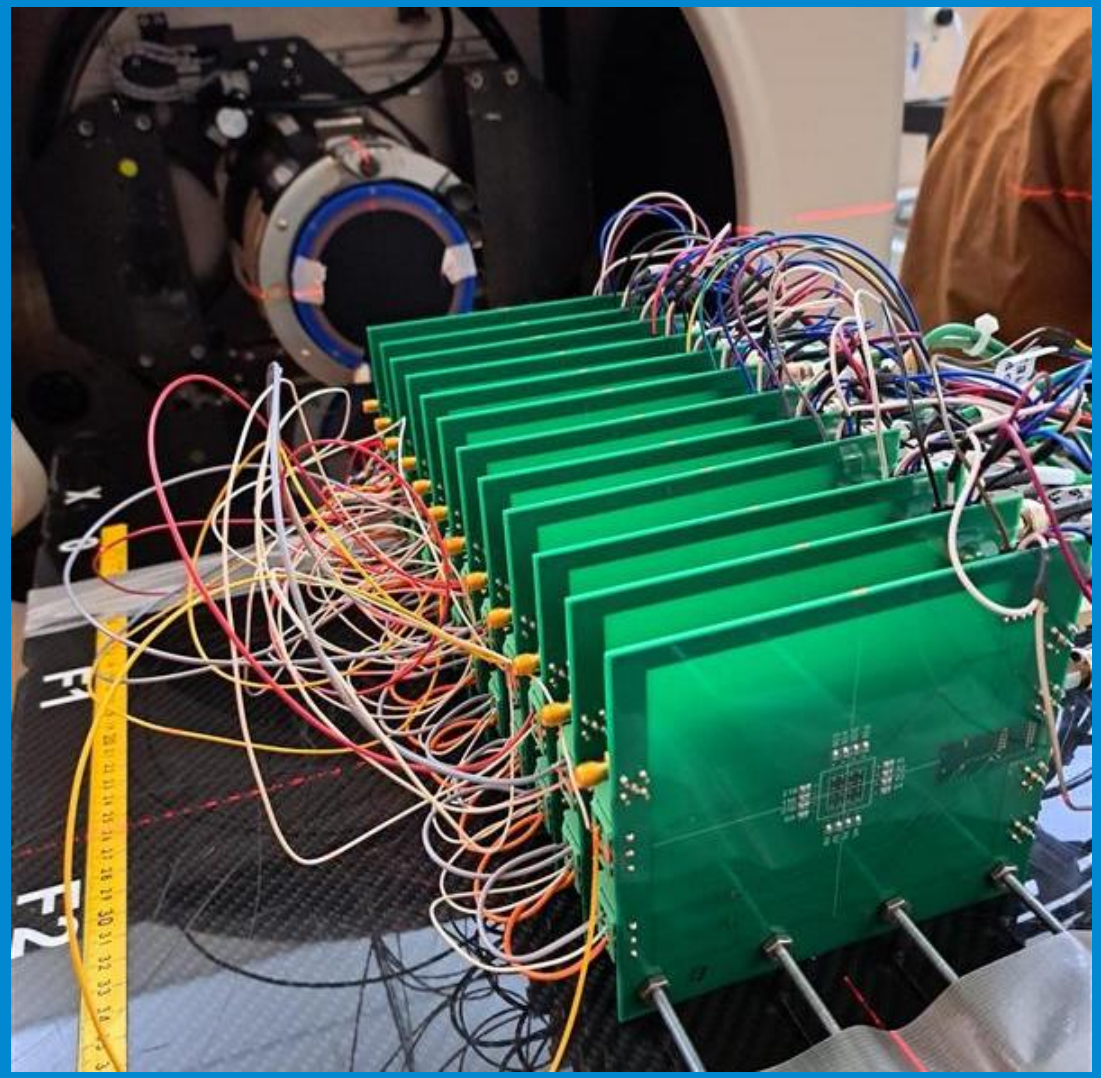
- 12 test boards
  - 4 die variations
  - 3 bias voltages (0, 10, and 15 V)
- 192 total devices under test

Measurement System

- Keysight B1500A
  - C-V sweep
  - 1 kHz – 5 MHz
- E5250A + E5252A
  - Select between the 12 boards

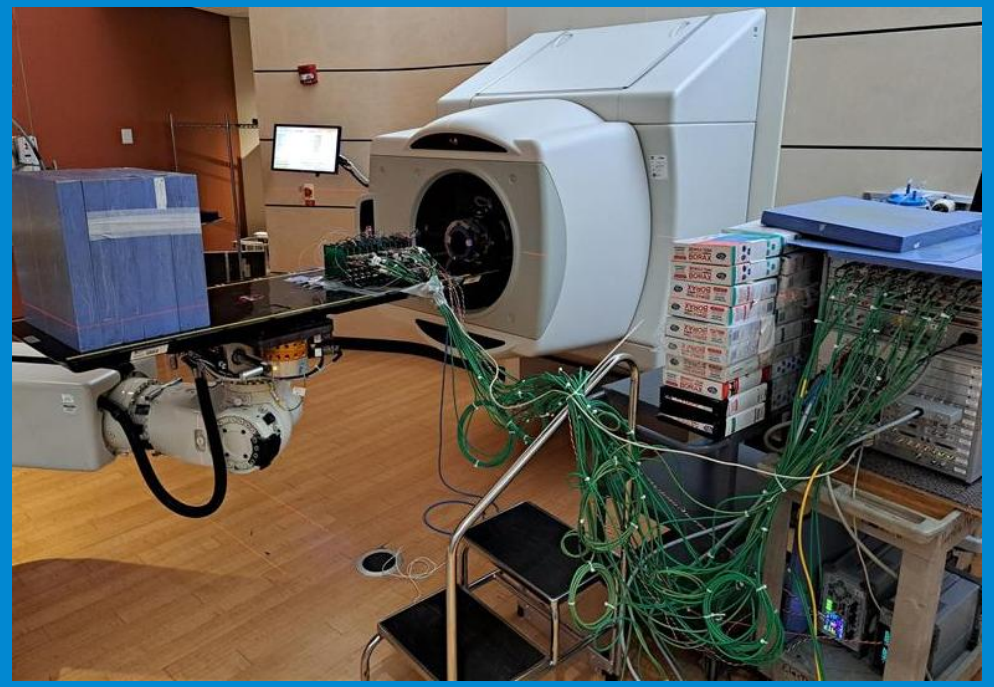
Test and measurement lead by Fermilab

Radiation Testing: 7/26 Tests



Testing at Northwestern Medicine Proton Center

- 175 MeV protons
- 1E9 p/cm^2/s
- Planned for 300 mins for 1 Mrad TID
- Completed first 60 mins (~200 krad) before proton center staff cancelled remaining radiation
- Post-radiation electrical measurements pending



Asks from NP Community

- Recommendations for radiation testing sources
  - Continued availability and suitability of the Northwestern Proton Center is unknown
  - Would testing with other radiation sources be more valuable to the NP community?

- Next steps
  - Complete measurements from 7/26 prototype irradiation
  - Conduct 2nd round of TID measurements (NCTE)

Contact

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oconnorka@caporus.com