Area X-ray Pixel Array Detectors for Time-resolved Synchrotron Applications

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The Need

• Detector capabilities are the BIGGEST limitation on better utilization of existing, much less future, synchrotron sources.

• Effectively, billions of dollars of investment are being poorly used.

• Pixel Array Detectors (PADs) are one of the most promising detector technologies.
PADs come in two varieties

Photon counting PADs

- Front ends count each x-ray individually. Existing variants include Pilatus (Dectris), Medipix.
- Drawback for high-speed imaging: Count-rate limited by electronics to $\sim 10^6$ - $10^7$ x-rays/pix/sec.

Integrating PADs

- Use an integrating front-end to avoid the count-rate bottleneck.
- Capable of handling enormous count-rate. Only practical case for most XFEL and many ERL expts.
- Existing variants include Cornell-LCLS, Cornell-ADSC, Acrorad

My remarks will focus exclusively on integrating PADs.
PAD #1

Gasoline fuel injector spray

Operated at instantaneous rates of $\sim 10^{13}$/pix/s

Collaboration with Jin Wang’s group at APS. Recent work: Liu et al., Appl. Phys. Lett. 94 (2009) 184101
Multi-Gain Concept

- Dynamic Range Compression required
- Relaxes ADC requirements
- Fits with CMOS complexity

Threefold analogue pipeline
On-chip ADC

C1 Cn

x1

x5

x20

STFC/RAL

University of Glasgow

(M. French, STFC)
The Adaptive Gain Integrating Pixel Detector

PSI/SLS - Villingen: chip design; interconnect and module assembly
Universität Bonn: chip design
Universität Hamburg: radiation damage tests, “charge explosion” studies; and sensor design
DESY: chip design, interface and control electronics, mechanics, cooling; overall coordination
Diesel fuel injector spray


Collaboration with Jin Wang’s group at APS. Recent work see Im et al., Phys. Rev. Lett. 102 (2009) 074501

Papers: see refs at end of talk: #272, 244, 241, 238, 209, 191, 179, 161, 153, 148, 141.
Collaboration w/ Todd Hufnagel at JHU.
• Cornell role: Design PAD chips, build single chip, cooled detector to spec. Completed.

• SLAC role: Build mosaic & mechanics, off-chip electronics, calibrate.

• 0.5 GB/s, 50 TB/day, continuously!

• Papers: See refs at end of talk: #225, 230, 243, 246, 267

PAD #3: Mixed-Mode PAD

<table>
<thead>
<tr>
<th>PAD Tile Format</th>
<th>128 x 128 pixels</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel Size</td>
<td>150 μm x 150 μm</td>
</tr>
<tr>
<td>Frame Rate</td>
<td>Up to 1,000 Hz</td>
</tr>
<tr>
<td>Read Noise</td>
<td>0.3 X-ray [12 keV] / pix</td>
</tr>
<tr>
<td>Well Capacity</td>
<td>2.6 x 10^7 X-ray [12 keV]/pix/frame</td>
</tr>
</tbody>
</table>

- Cornell role: Design PAD chips, build single chip, cooled detector to spec. Completed.
- ADSC role: Build large detectors & vend. In process.
- 65 MB/ASIC/s. For a 1k x 1k this is 400 TB/day, continuously!
- Papers: see refs at end of talk #196, 226, 265
- In process of building mosaic detectors for CXI, SAXS and other applications.
Mixed-Mode PAD has a HUGE dynamic range

MMPAD. AI @ CHESS F2. 1 sec expos. No Beamstop!
### PAD #4: KECK PAD

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Target Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Noise</td>
<td>(&lt;0.5) x-ray/pixel/accumulation</td>
</tr>
<tr>
<td>Minimum exposure time</td>
<td>150 ns for 8-bit imaging 1 (\mu) s for full-well imaging</td>
</tr>
<tr>
<td>Capacitor well depth</td>
<td>2000 – 4000 (\text{x-rays})</td>
</tr>
<tr>
<td>Nonlinearity (% full well)</td>
<td>(&lt;0.2%)</td>
</tr>
<tr>
<td>Diode conversion layer</td>
<td>500 (\mu) thick Si</td>
</tr>
<tr>
<td>Number of capacitor wells/pix</td>
<td>8</td>
</tr>
<tr>
<td>Full chip frame time</td>
<td>1 (\text{msec/frame, e.g., 8 msec for 8 capacitors})</td>
</tr>
<tr>
<td>Radiation lifetime</td>
<td>(&gt; 50) Mrad at detector face @ 8 keV</td>
</tr>
<tr>
<td>Pixel size</td>
<td>150 (\mu) on a side, or 128 x 128 pixels per IC</td>
</tr>
<tr>
<td>Detector chip format</td>
<td>2 x 4 chips = 256 x 512 pixels</td>
</tr>
<tr>
<td>Dark current</td>
<td>2 x-rays/pix/sec</td>
</tr>
</tbody>
</table>

• Designed for single bunch imaging at storage rings, e.g., APS.
• ASIC funded by Keck Foundation. Off-chip FPGA test bed via DOE-BES
• Status: Pixel developed, 16x16 detector built and tested. Meets spec. Full ASIC in fab.
• Papers: see refs at end of talk: #250,264
The PAD development cycle is long, often 5 or more years.

What can we do to shorten the development time?

FPGA-based PADs
What is an FPGA

- **Field programmable gate arrays.**
- **FPGAs** are digital integrated circuits that:
  - contain configurable (programmable) blocks of logic and interconnects
  - Can be reconfigured, or programed, “in the field” to perform a great variety of tasks. Firmware.
  - Large numbers of input/output (I/O) pins for interfacing
  - Fast powerful massively parallel processing engine.
  - Contains internal ultra-fast RAM that can be distributed across an application
# FPGAs Processing Power over Time

<table>
<thead>
<tr>
<th>Device Family</th>
<th>Logic Cells</th>
<th>Maximum Block RAM</th>
<th>DSP slices</th>
<th>PCI Express interfaces</th>
<th>Maximum User IO</th>
<th>Ultra-fast IO</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex 4</td>
<td>142,00</td>
<td>6 Mbits</td>
<td>512</td>
<td>0</td>
<td>960</td>
<td>24</td>
</tr>
<tr>
<td>Virtex 5</td>
<td>330000</td>
<td>18 Mbits</td>
<td>1056</td>
<td>4 (2 soft)</td>
<td>1000</td>
<td>48</td>
</tr>
<tr>
<td>Virtex 6</td>
<td>549,888</td>
<td>38 Mbits</td>
<td>2000</td>
<td>4</td>
<td>1200</td>
<td>48</td>
</tr>
<tr>
<td>Virtex 7</td>
<td>1,954,560</td>
<td>56 Mbits</td>
<td>3900</td>
<td>4</td>
<td>1200</td>
<td>72</td>
</tr>
</tbody>
</table>
Typical DAQ System for PADs

- Tiled PAD mounted onto circuit board
- Board to board or flex connectors connect PAD to support circuitry
- High Speed connection conveys high data throughput from PAD
- Support circuitry – ADCs, DACs, may contain FPGA for simple control
- FPGA for control, buffering and protocol exchange
- High Speed DAQ board
- High Speed Serial IO to data storage
- Massive Data Storage System
- Bottleneck
- Off-line processing of massive data set
- Bottleneck
- Bottleneck
- Bottleneck
- Bottleneck
Long Term Goals of DOE-BES Project

• Remove bottlenecks via mating of detector CMOS ASIC and the FPGA so that the FPGA is an integral resident part of the detector, rather than just a part of the control hardware.

• Fast, simple pixel integrating front end.

• FPGA back-end whose reconfigurable implementation can be tailored to meet various applications.

• Configurations being considered (with no hardware changes):
  – MHz autocorrelator/pixel speckle detector
  – X-ray lock-in per pixel detector
  – Sequential snapshot in log-time detector
Implementation: Multi-Pronged Strategy

1. Extend capability of existing ASICs (e.g., MMPAD and Keck PAD) by developing wide-bandwidth off-ASIC electronics to an FPGA platform to make a firmware reconfigurable system. **Status: Circuit boards are in design and fab.**

2. Test this by application to challenging time-resolved science problems, such as high count rate coherent x-ray imaging. **Status: Plans have been discussed with beamline scientists at the APS and Swiss Light Source.**

3. Develop new pixels and ASICs specifically designed for mating with FPGAs. These will eventually be scaled into full-sized detectors (e.g., “FPGA-PAD”) and tested with, e.g., x-ray speckle applications. **Status: An ASIC to test pixel ideas will be submitted for fabrication to MOSIS in Sept.**
Acknowledgements

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  – Daniel Schuette (Lincoln Labs) --- Alper Ercan

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  – Area Detector Systems Corporation (ADSC)/NIH-NCRR
  – Keck Foundation
**References**


END