Area X-ray Pixel Array Detectors for Time-resolved Synchrotron Applications

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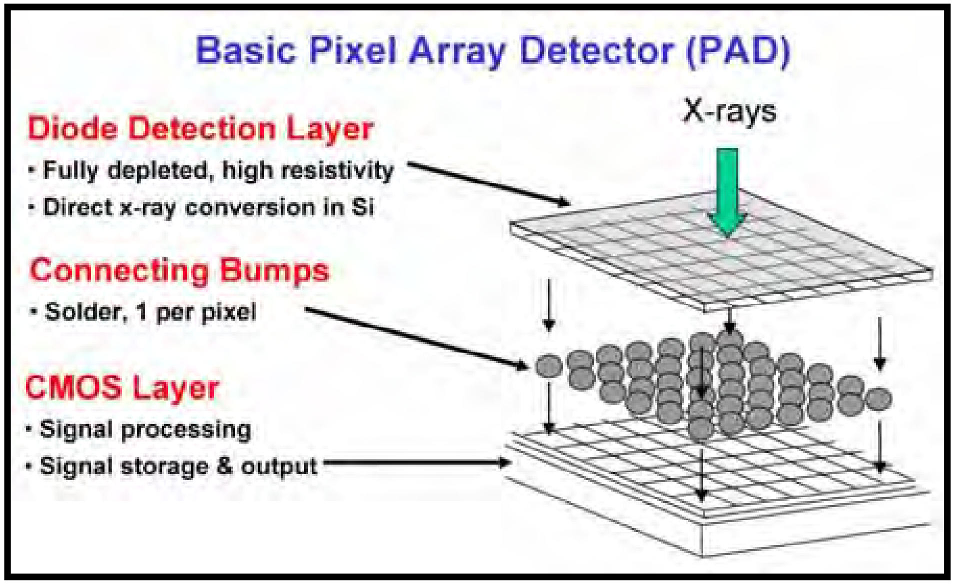
The Need

- **Detector capabilities are the BIGGEST limitation on better utilization of existing, much less future, synchrotron sources.**
- **Effectively, billions of dollars of investment are being poorly used.**
- **Pixel Array Detectors (PADs) are one of the most promising detector technologies.**



PADs come in two varieties

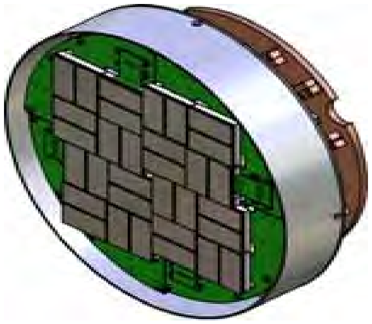
Photon counting PADs

- Front ends count each x-ray individually. Existing variants include Pilatus (Dectris), Medipix.
- Drawback for high-speed imaging: Count-rate limited by electronics to ~10^6 -10^7 x-rays/pix/sec.

SLS PILATUS

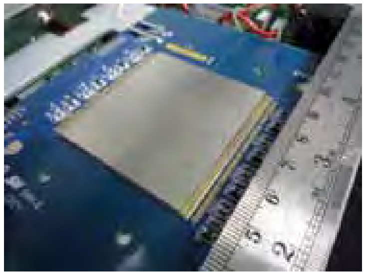
Integrating PADs

- Use an integrating front-end to avoid the count-rate bottleneck.
- Capable of handling enormous count-rate. Only practical case for most XFEL and many ERL expts.
- Existing variants include Cornell-LCLS, Cornell-ADSC, Acrorad



Cornell-SLAC LCLS

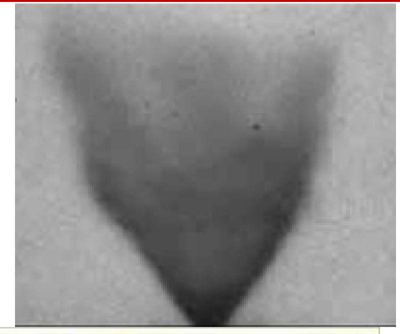
My remarks will focus exclusively on integrating PADs.

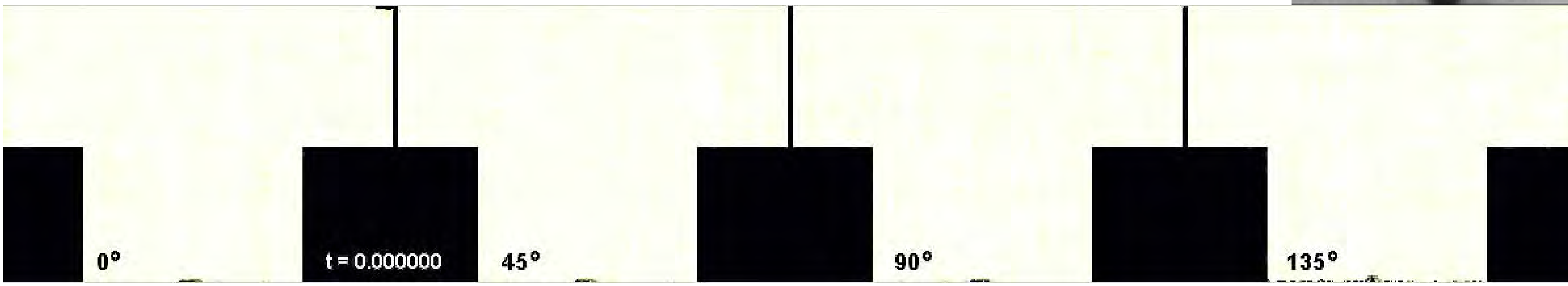


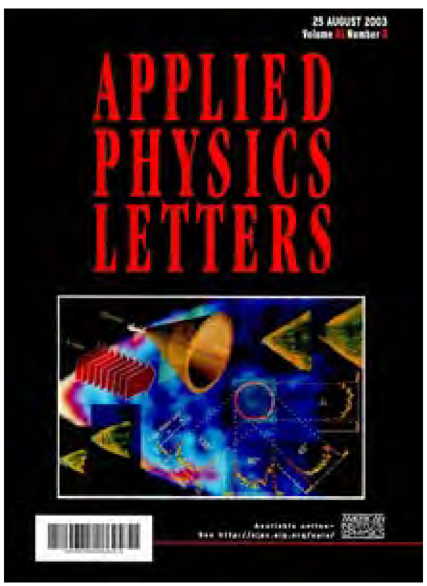
Acrorad CdTe

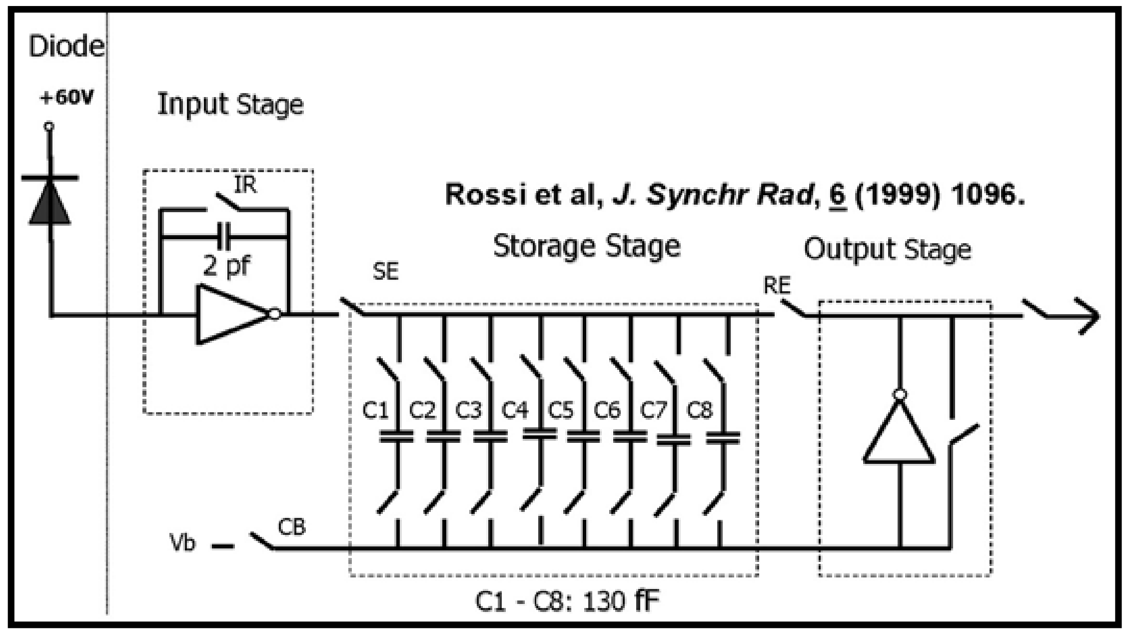
PAD #1
Gasoline fuel injector spray

Operated at instantaneous rates of ~10^{13}/pix/s







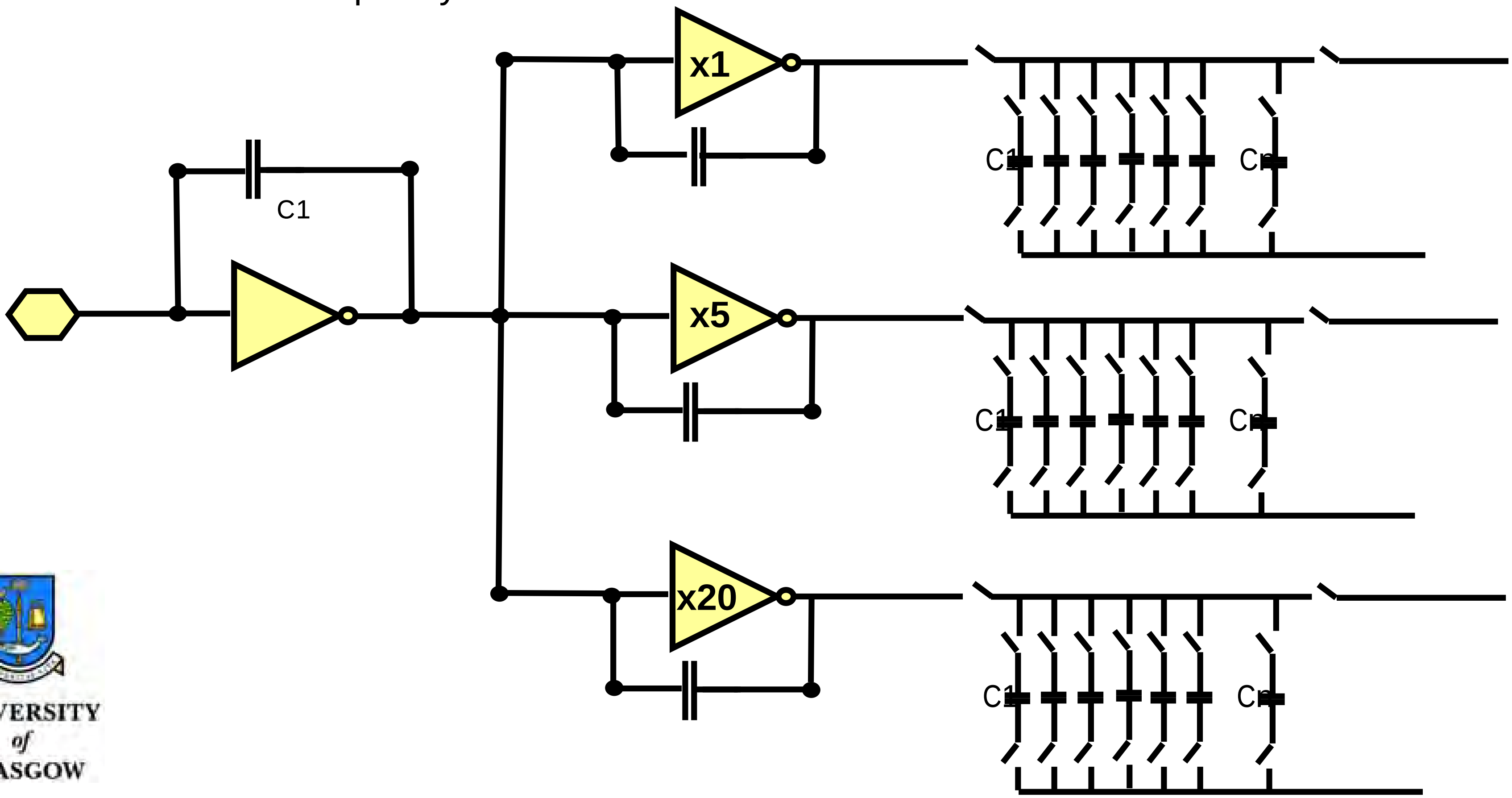


Collaboration with Jin Wang's group at APS. Recent work: Liu *et al.*, Appl. Phys. Lett. **94** (2009) 184101

> Multi-Gain Concept

- > Dynamic Range Compression required
- > Relaxes ADC requirements
- > Fits with CMOS complexity

Threefold analogue pipeline
On-chip ADC



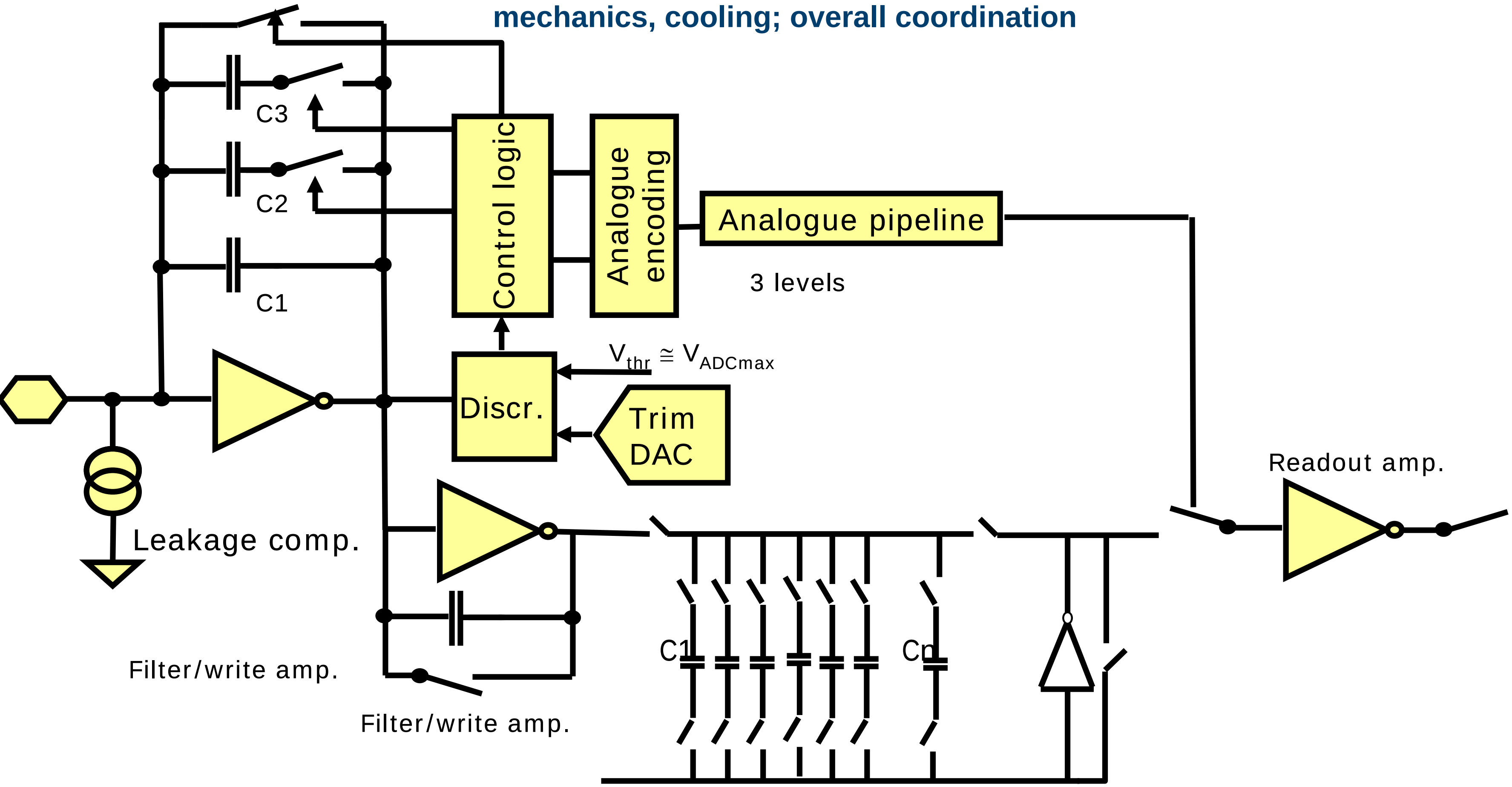
(M. French, STFC)

> STFC/RAL

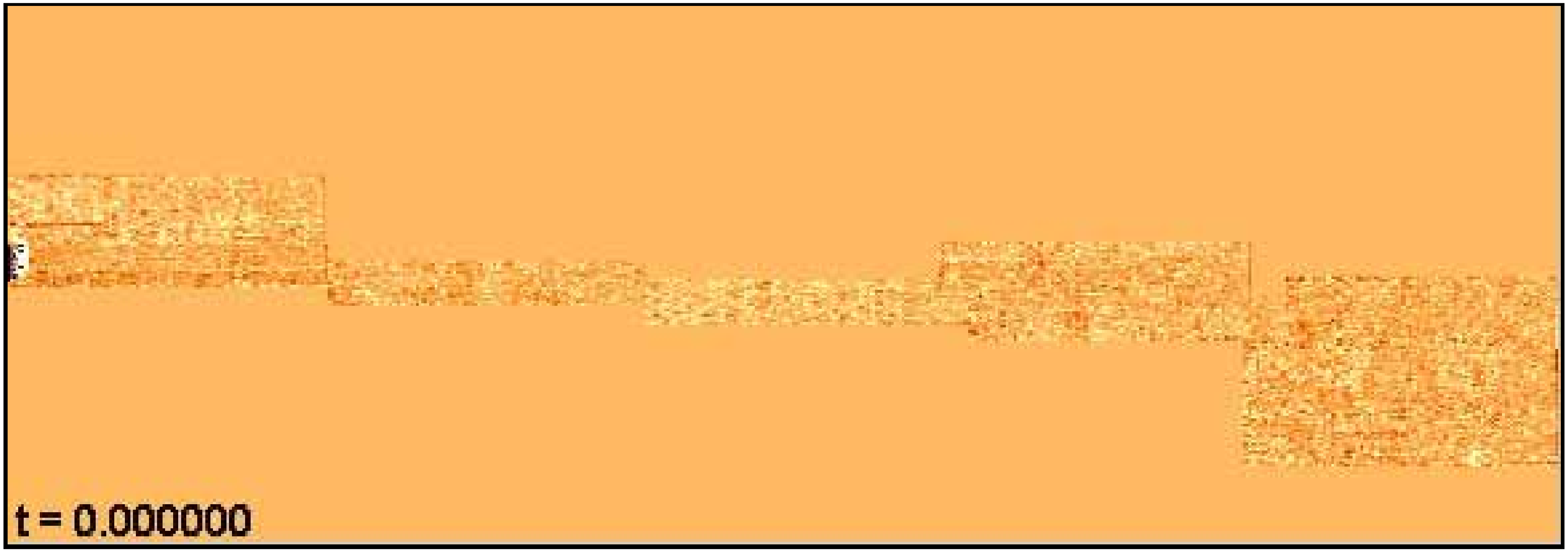
> University of Glasgow

The Adaptive Gain Integrating Pixel Detector

PSI/SLS -Villingen: chip design; interconnect and module assembly
Universität Bonn: chip design
Universität Hamburg: radiation damage tests, “charge explosion” studies; and sensor design
DESY: chip design, interface and control electronics, mechanics, cooling; overall coordination



Diesel fuel injector spray



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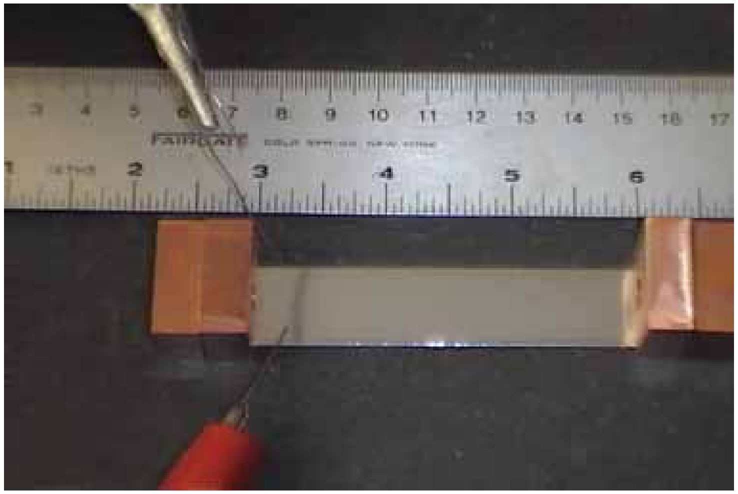
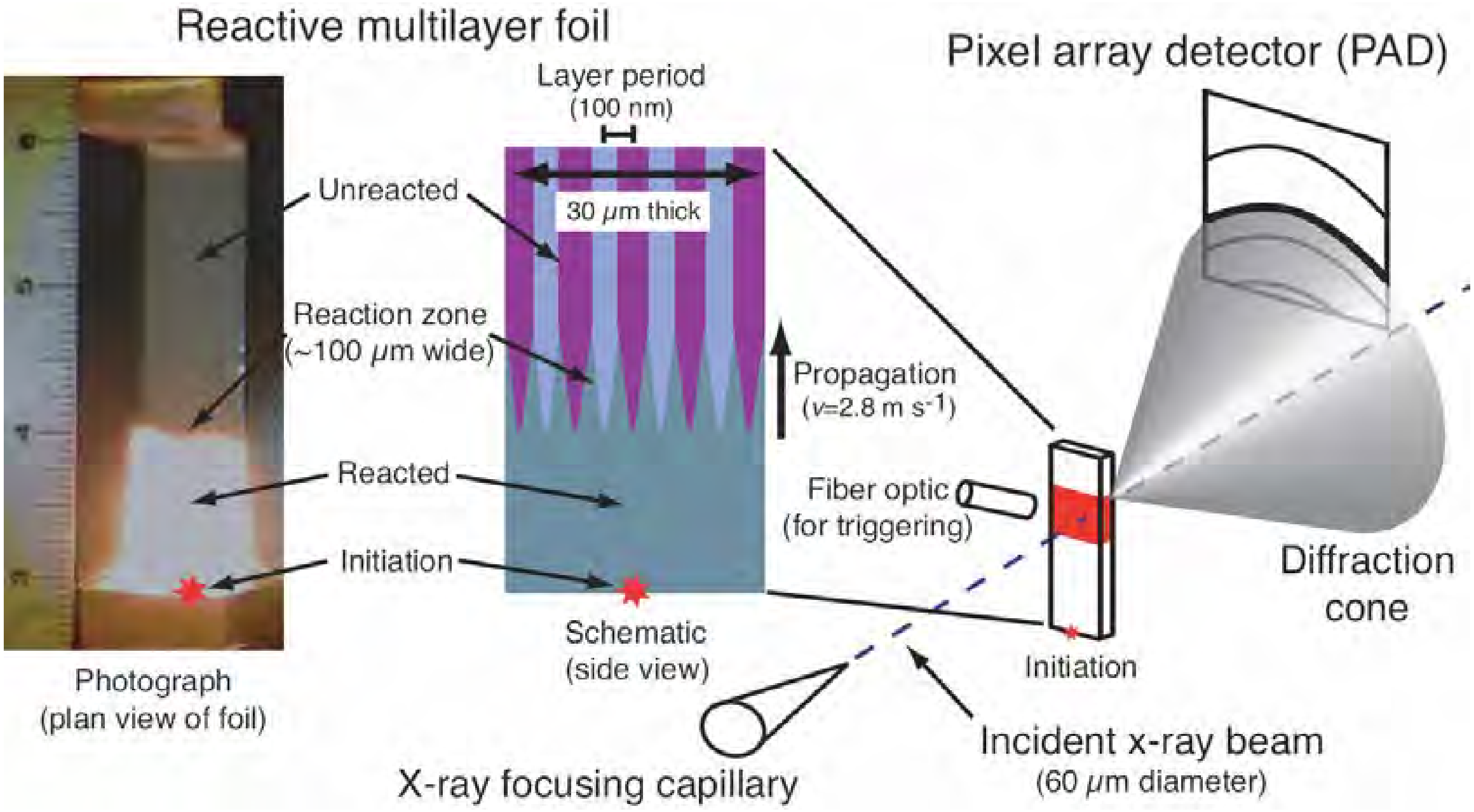
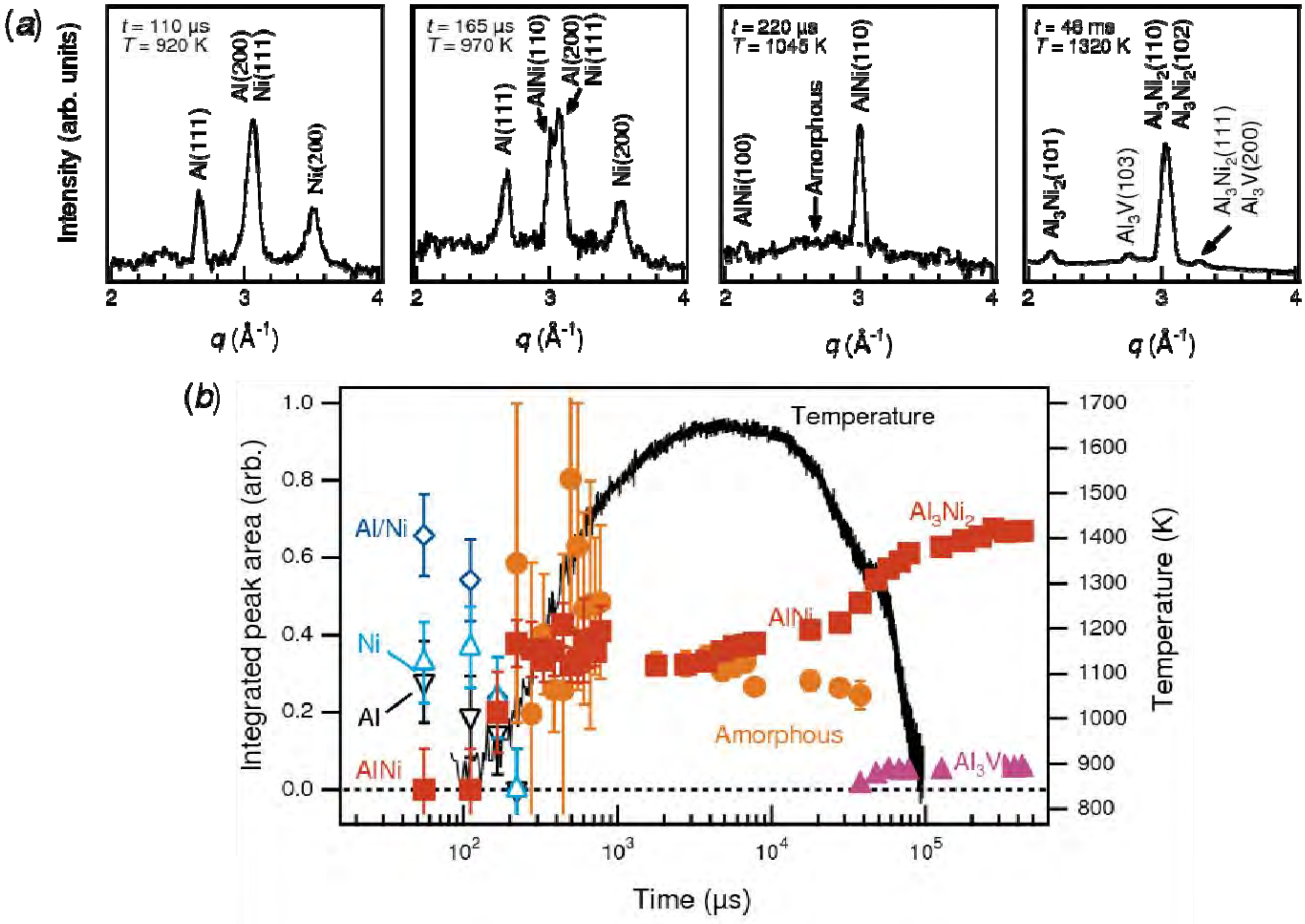
Collaboration with Jin Wang's group at APS. Recent work see Im *et al.*, Phys. Rev. Lett. **102** (2009) 074501
Papers: see refs at end of talk: #272, 244, 241, 238, 209, 191, 179, 161, 153, 148, 141.

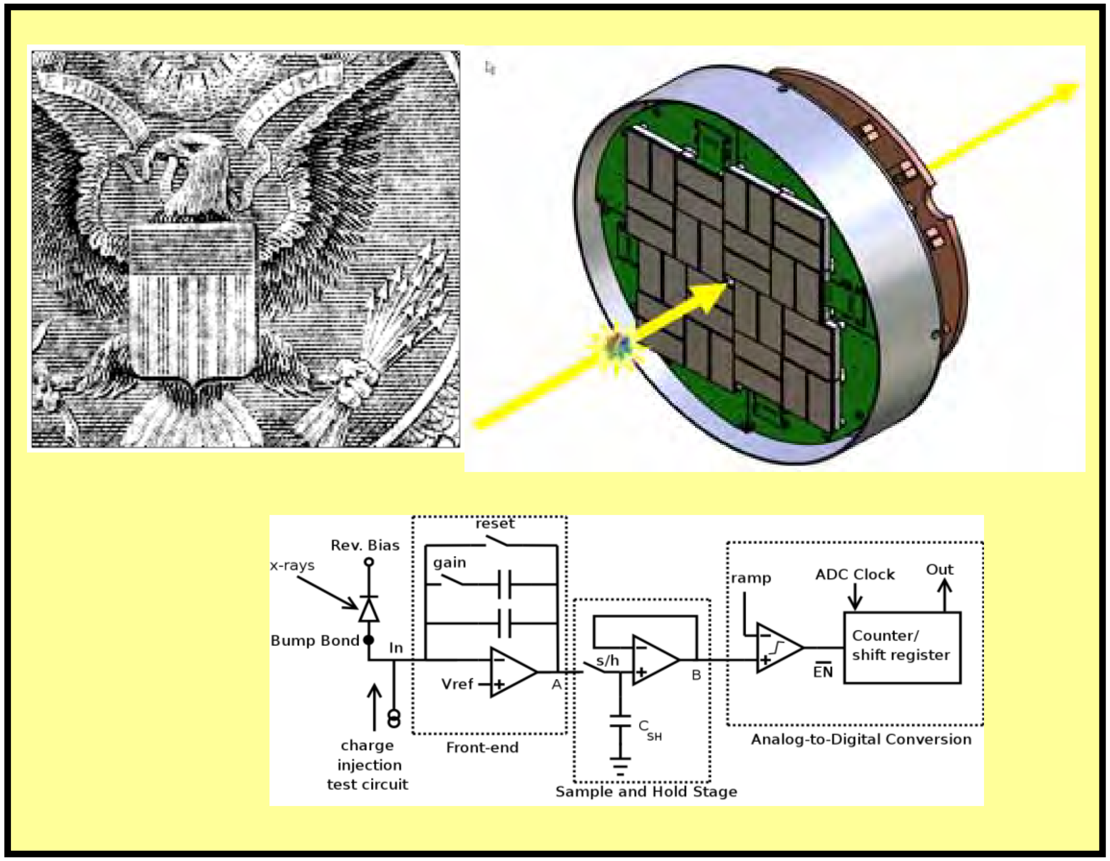
Collaboration w/ Todd Hufnagel at JHU.







J. C. Trenkle, L. J. Koerner, *et al*. *Phase Transformations During Rapid Heating of Al/Ni Multilayer Foils*, Applied Physics Letters (2008) 93, 081903.

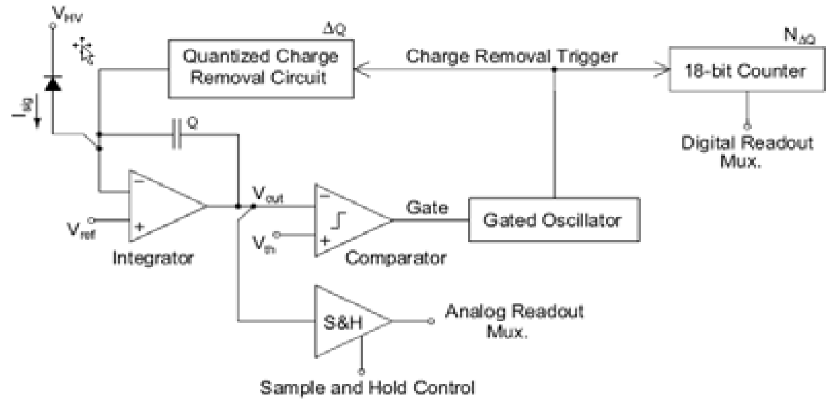


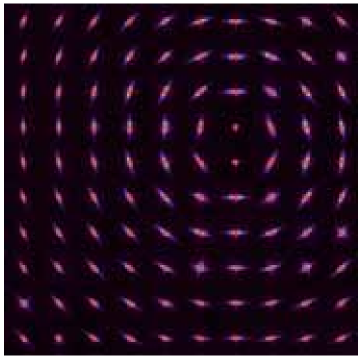
PAD #2: LCLS PAD

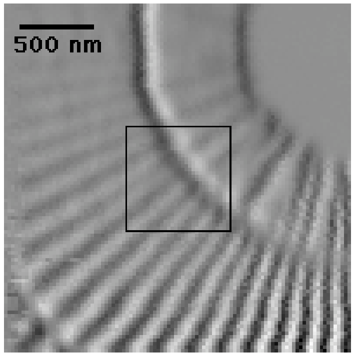
- **Cornell role: Design PAD chips, build single chip, cooled detector to spec. Completed.**
- **SLAC role: Build mosaic & mechanicals, off-chip electronics, calibrate.**
- **0.5 GB/s, 50 TB/day, continuously!**
- **Papers: See refs at end of talk: #225, 230, 243, 246, 267**
- **Most recently applied at CHESS to monitor real-time nanotube forest growth – collaborations with John Hart et al at Mich. State U. (In preparation).**

PAD #3: Mixed-Mode PAD

PAD Tile Format	128 x 128 pixels
Pixel Size	150 µm x 150 µm
Frame Rate	Up to 1,000 Hz
Read Noise	0.3 X-ray [12 keV] / pix
Well Capacity	2.6 x 10^7 X-ray [12 keV]/pix/frame

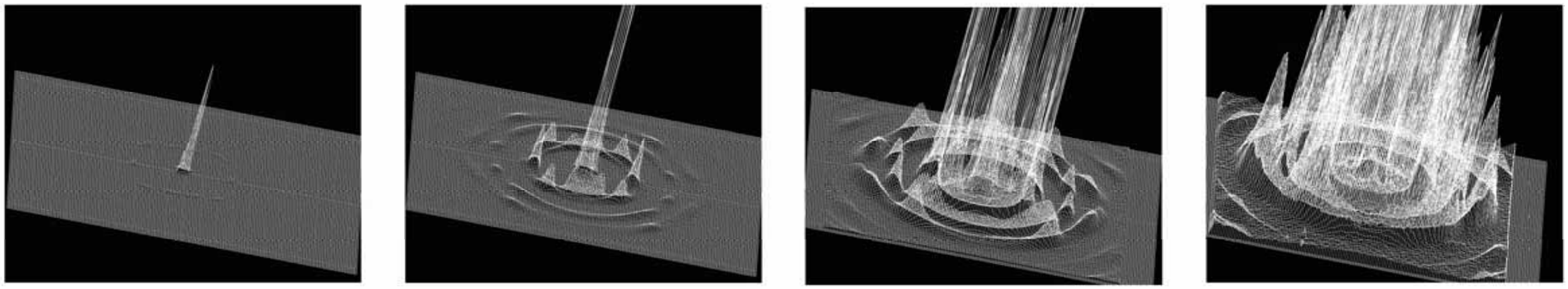




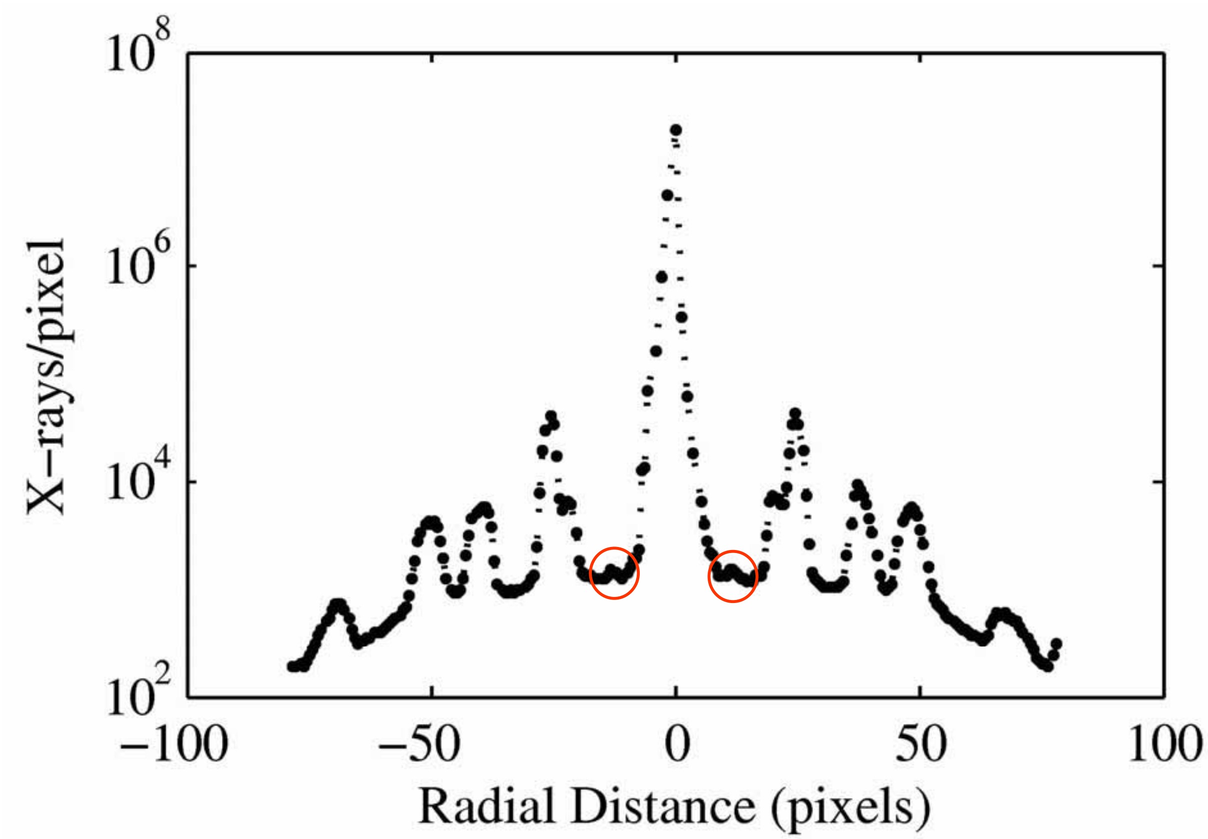


- Cornell role: Design PAD chips, build single chip, cooled detector to spec. Completed.
- ADSC role: Build large detectors & vend. In process.
- 65 MB/ASIC/s. For a 1k x 1k this is 400 TB/day, continuously!
- Papers: see refs at tend of talk #196, 226, 265
- In process of building mosaic detectors for CXI, SAXS and other applications.

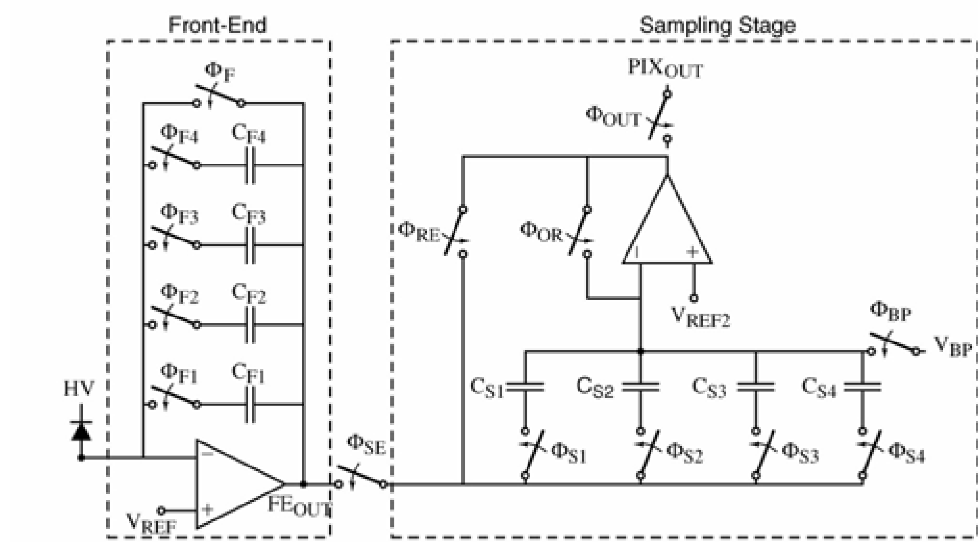
Mixed-Mode PAD has a HUGE dynamic range

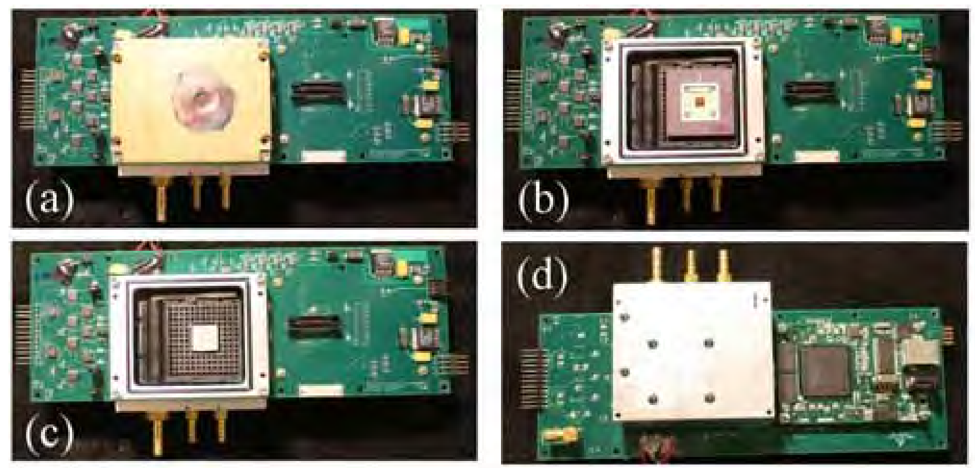


MMPAD. Al @ CHESS F2. 1 sec expos. No Beamstop!



PAD #4: KECK PAD	
Parameter	**Target Value**
Noise	< 0.5 x-ray/pixel/accumulation
Minimum exposure time	150 ns for 8-bit imaging 1 µs for full-well imaging
Capacitor well depth	2000 – 4000 x-rays
Nonlinearity (% full well)	< 0.2%
Diode conversion layer	500 µm thick Si
Number of capacitor wells/pix	8
Full chip frame time	1 msec/frame, e.g., 8 msec for 8 capacitors
Radiation lifetime	> 50 Mrad at detector face @ 8 keV
Pixel size	150 µm on a side, or 128 x 128 pixels per IC
Detector chip format	2 x 4 chips = 256 x 512 pixels
Dark current	2 x-rays/pix/sec





- **Designed for single bunch imaging at storage rings, e.g., APS.**
- **ASIC funded by Keck Foundation. Off- chip FPGA test bed via DOE-BES**
- **Status: Pixel developed, 16x16 detector built and tested. Meets spec. Full ASIC in fab.**
- **Papers: see refs at end of talk: #250,264**

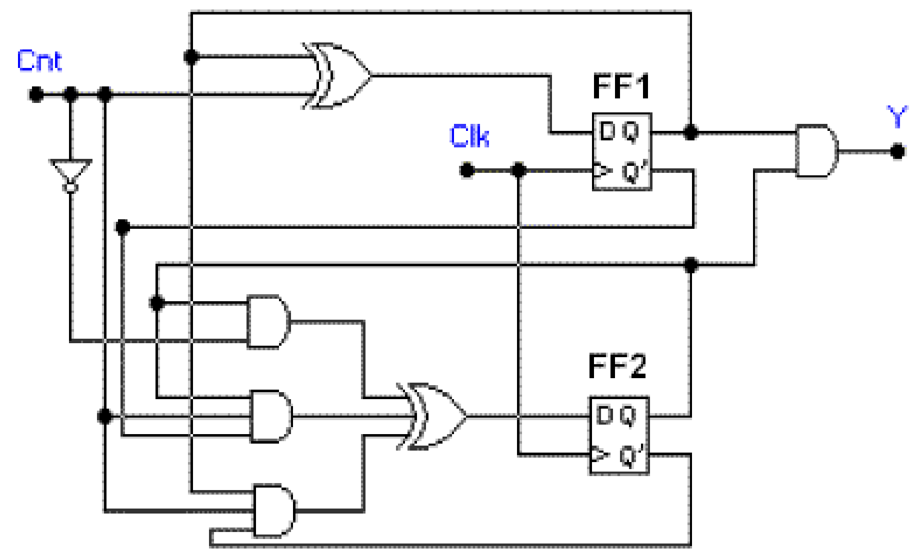
The PAD development cycle is long, often 5 or more years.

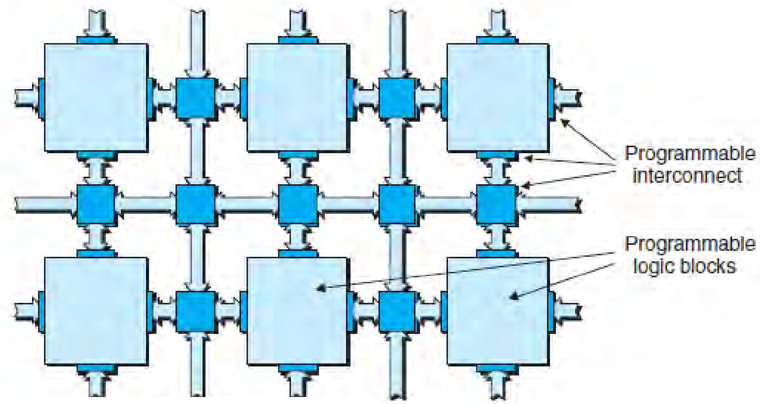
What can we do to shorten the development time?

FPGA-based PADs

What is an FPGA

- ***Field programmable gate arrays.***
- ***FPGAs* are digital integrated circuits that:**
  - **contain configurable (programmable) blocks of logic and interconnects**
  - **Can be reconfigured, or programed, “in the field” to perform a great variety of tasks. Firmware.**
  - **Large numbers of input/output (I/O) pins for interfacing**
  - **Fast powerful massively parallel processing engine.**
  - **Contains internal ultra-fast RAM that can be distributed across an application**

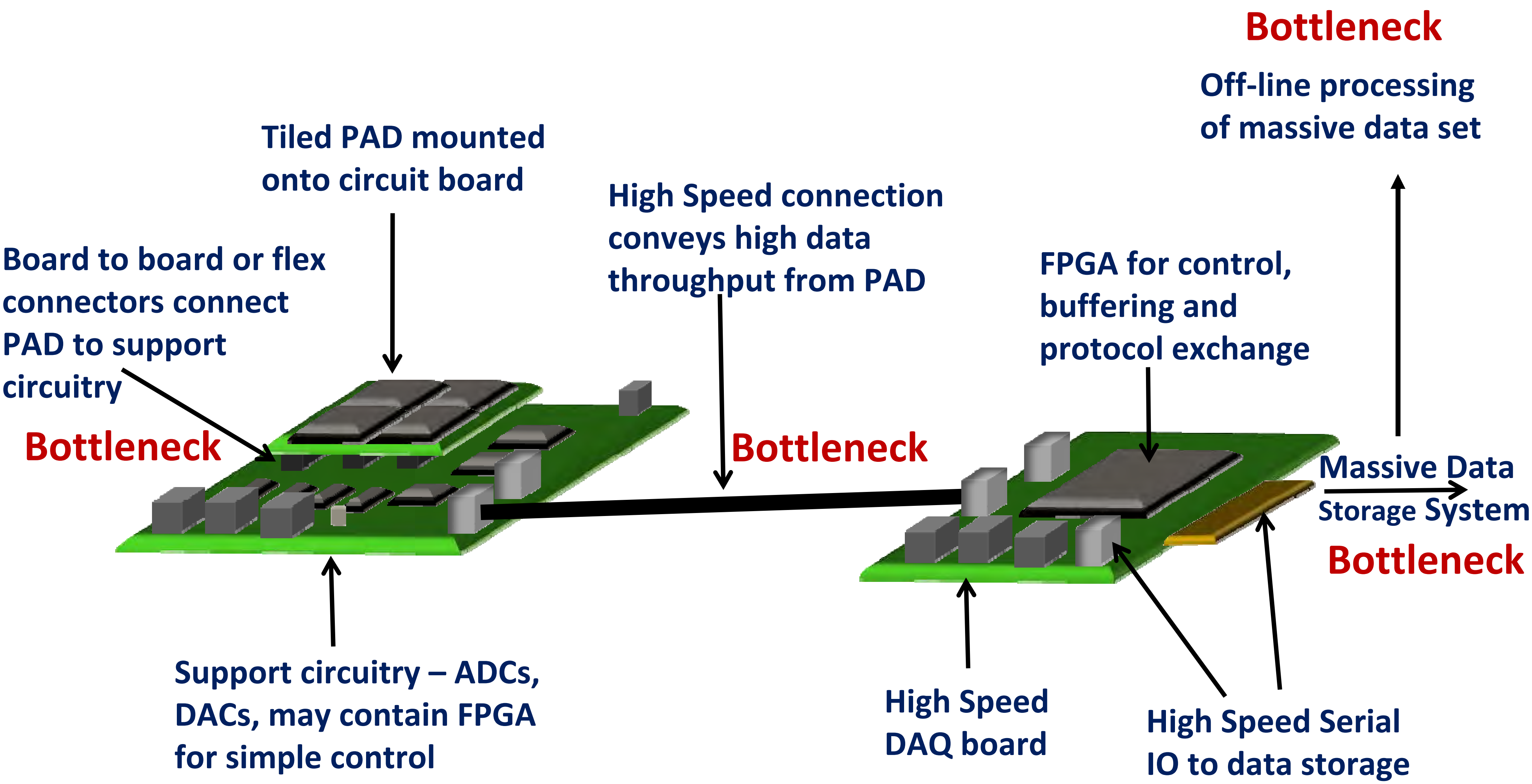




FPGAs Processing Power over Time

Device Family	Logic Cells	Maximum Block RAM	DSP slices	PCI Express interfaces	Maximum User IO	Ultra-fast IO
Virtex 4	142,00	6 Mbits	512	0	960	24
Virtex 5	330000	18 Mbits	1056	4 (2 soft)	1000	48
Virtex 6	549,888	38 Mbits	2000	4	1200	48
Virtex 7	1,954,560	56 Mbits	3900	4	1200	72

Typical DAQ System for PADs



Long Term Goals of DOE-BES Project

- **Remove bottlenecks via mating of detector CMOS ASIC and the FPGA so that the FPGA is an *integral resident part of the detector*, rather than just a part of the control hardware.**
- **Fast, simple pixel integrating front end.**
- **FPGA back-end whose reconfigurable implementation can be tailored to meet various applications.**
- **Configurations b eing considered (with no hardware changes):**
  - **MHz autocorrelator/pixel speckle detector**
  - **X-ray lock-in per pixel detector**
  - **Sequential snapshot in log-time detector**

Implementation: Multi-Pronged Strategy

1. **Extend capability of existing ASICs (e.g., MMPAD and Keck PAD) by developing wide-bandwidth off-ASIC electronics to an FPGA platform to make a firmware reconfigurable system. Status: Circuit boards are in design and fab.**

2. **Test this by application to challenging time-resolved science problems, such as high count rate coherent x-ray imaging. Status: Plans have been discussed with beamline scientists at the APS and Swiss Light Source.**

3. **Develop new pixels and ASICs specifically designed for mating with FPGAs. These will eventually be scaled into full-sized detectors (e.g., "FPGA-PAD") and tested with, e.g., x-ray speckle applications. Status: An ASIC to test pixel ideas will be submitted for fabrication to MOSIS in Sept.**

Acknowledgements

- Cornell Detector Development Group
  - Sol Gruner -- Mark Tate
  - Hugh Philipp -- Kate Green
  - Darol Chamberlain -- Prafull Purohit
  - Marianne Hromalik
- Recent members of Cornell Detector Development Group
  - Lucas Koerner (APL, Johns Hopkins) --- Matt Renzi (MIT)
  - Daniel Schuette (Lincoln Labs) --- Alper Ercan
- Sponsors and Collaborators
  - National Science Foundation : NSF-DMR (DMR-0936384)
  - Department of Energy DOE-BES (DE-SC0004079) ,DOE-BER (DE-FG02-97ER62443))
  - LCLS Detector Group at SLAC
  - Area Detector Systems Corporation (ADSC)/NIH-NCRR
  - Keck Foundation

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