Advanced Detectors for Synchrotron Radiation
FWP# LS-015

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Abstract

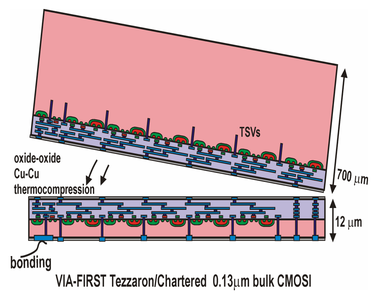
The project has two primary directions:

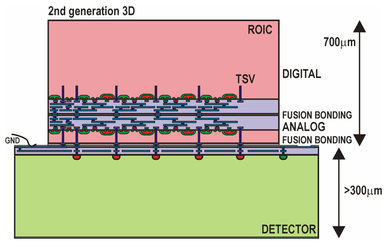
(a) To explore the feasibility of using 3D integration techniques as a means to enhance the signal processing capabilities in each pixel, i.e. towards making 'smart detectors'.

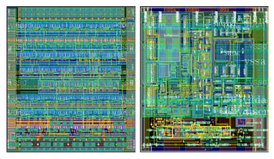
(b) To develop a planar process for the fabrication of hyper-pure germanium detectors, thereby allowing the production of similar devices to those routinely made in silicon such as microstrip detectors and drift detectors.

3D integration.

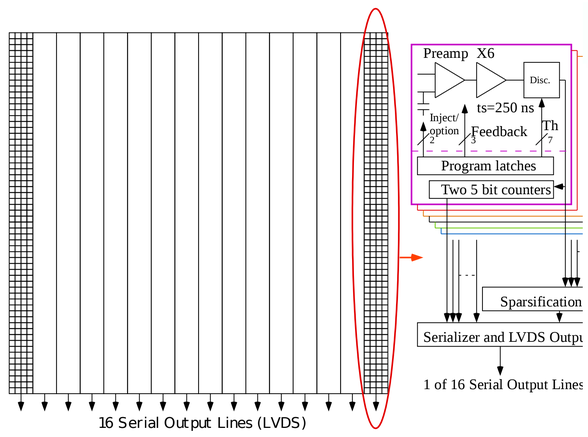
3D integration is a new technology aimed at increasing the density of microcircuits by expanding in the third dimension, by stacking CMOS chips one atop the other and providing high-density interconnections between the layers. The two figures below summarise the process. First, two wafers are prepared with CMOS circuits on one face. The difference between these circuits and conventional ones is the presence of so-called Through-Silicon Vias (TSVs). These are the small projections protruding into the bulk silicon wafer. After the two wafers are bonded together (also connected together electrically in the process), then one of them is ground down to expose these TSVs (the bottom wafer in the figure). We now have the possibility to connect to the circuits by electrically contacting these vias. The right-hand diagram shows how we can connect a third layer, the x-ray sensor to this 2-layer CMOS stack.



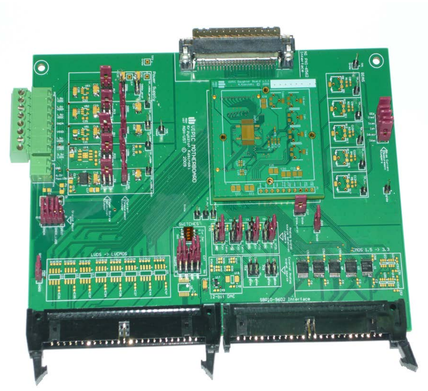




The silicon layout for the analog and digital layers of one pixel. These designs are implemented in silicon and then bonded face-to-face to form the 3D integrated circuit. VIPIC carries 4096 of each of these circuits.



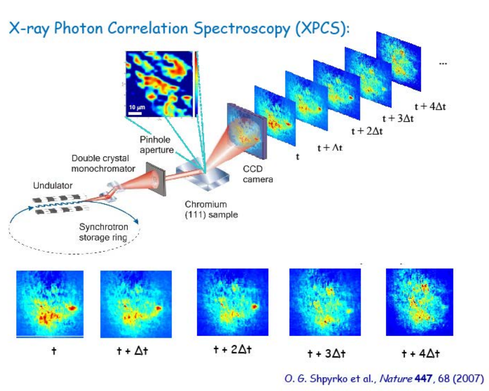
A schematic view of the internal architecture of VIPIC. IT is arranged as 16 blocks of 256 pixels. Each pixel holds, on the analog layer, a preamplifier and shaping amplifier plus a pulse height comparator which sets a lower threshold for the signal amplitudes which get processed. The digital layer holds the pulse counters and hit registers, plus the logic which permits only non-zero pixels to be read (sparsification).



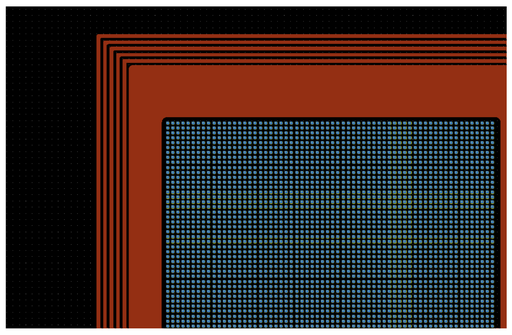
A printed circuit board which provides support for testing the VIPIC chips, including power supplies, signal buffers and connectors to transmit the event stream to a data acquisition system.

VIPIC: A detector for real-time X-ray correlation Spectroscopy

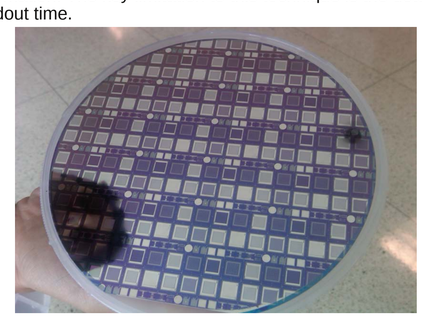
The detector under construction is a unique design, being the first imaging detector with functionality custom designed for the XCS experiment. It was designed by a collaboration including BNL, Fermilab and AGH University, Krakow. It can operate in two modes, either a low-occupancy mode, in which only non-zero count pixels are read out, labeled with the pixel location, and a fast-framing mode in which all pixels are read out sequentially. In the first mode, the data volume is reduced. In the second, an imaging detector with a 100kHz frame rate results. In the latter mode, the pixel depth is 32 photons, corresponding to an average rate of 3 Mph/s/pixel. For our 4k pixel prototype this is a 2GB/s data rate. Larger arrays would generate proportionally larger data rates. In either mode, it provides a shortest correlation time of 10us. We describe below external circuits to process this data stream in real time.

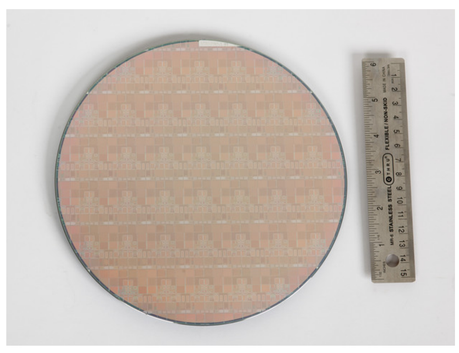


X-ray correlation allows us to measure the atomic scale internal motions of a sample. As the objects in the sample move, the phase of their scattered x-rays changes, causing time-dependent interference maxima and minima. Performing a time-autocorrellation pattern on these “speckles” provides this information. The key limitation to this technique is the detector readout time.



Part of the lithography mask set for the sensor wafer designed to match the VIPIC chip. It consists of a 64 x 64 array of photodiodes with 80 micrometers pitch. The red areas are guard structures which will allow us to protect the ASIC from any possible electrical breakdown. The photodiodes will need to be biased to over 100V to provide full depletion and hence maximum efficiency.

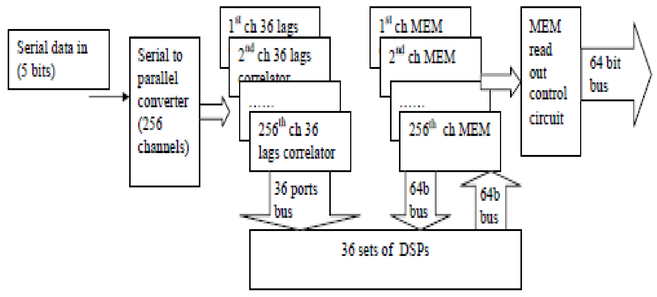




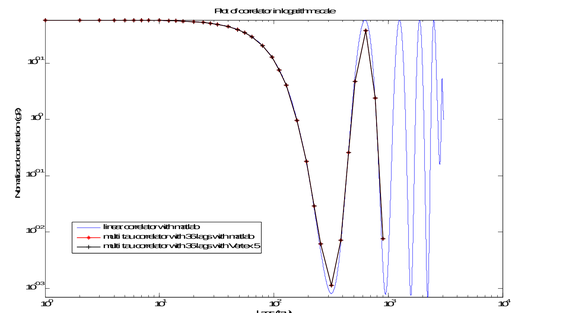
Finished wafers for the detector. On the left is the 6” high-resistivity wafer carrying the sensors for eight projects which are part of the collaboration. On the right is an 8” wafer, patterned with the integrated circuits which will eventually be bonded to the sensor wafer on the left. The 8” wafer will be diced into individual blocks and then bonded to the sensr using “chip-to-wafer” bonding techniques.

Real-time Autocorrelation

The detector will produce a stream of photon detection events, and the scientific interest is in the time autocorrelation of the event stream from each pixel. This means we must design a system with 4096 autocorrelators for each 64 x 64 block of a VIPIC detector. We have designed the basic block of such a system in the form of an FPGA containing 256 multiple-Tau autocorrelators covering the time range 10us to 10ms. The FPGA code can be interpreted to produce a full-custom ASIC design which could accommodate 4 of these devices. Thus, 4 ASICs would service one VIPIC.



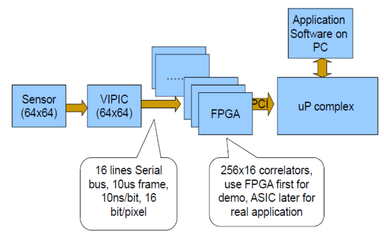
Block diagram of the multiple-Tau autocorrelator architecture. It takes as input one serial bit stream from one of VIPIC's 16 serial outputs, de-serializes it and performs the autocorrelation, storing the outputs in on-chip memory. Autocorrelation data is passed to the user via a 64-bit PCI bus.



The output of the autocorrelator for a sinusoidal input signal. The data produced by the FPGA device is compared with the output of the equivalent calculation performed in software, and with the theoretical linear correlator also implemented in software. It is clear that the FPGA output is identical with the equivalent software result.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	98141	301440	32%
Number of Slice LUTs	146540	150720	97%
Number of fully used LUT-FF pairs	46818	197863	23%
Number of bonded IOBs	0	600	0%
Number of BUFG/BUFGCTRLs	13	32	40%
Number of DSP48E1s	24	768	3%

Table showing the utilization of the resources provided by the Virtex6 FPGA used for this study. Clearly the result is dominated by the LUTs, i.e. basic gates. Implementation in an ASIC would greatly reduce this problem since ASIC basic gates are very area-efficient.



Suggested system configuration.

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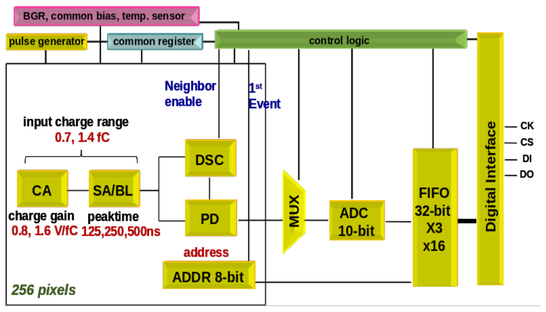
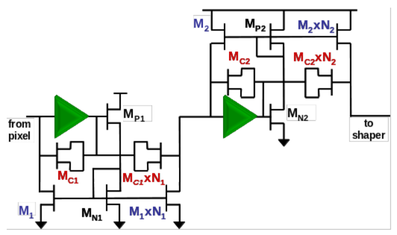
HIXD: A Hyperspectral Imaging X-ray Detector

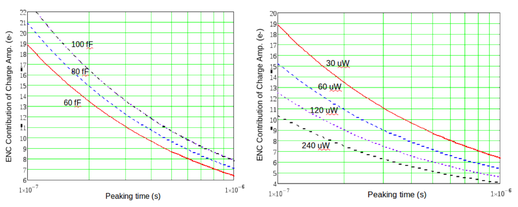
There is a need for an imaging x-ray detector capable of providing photon energy information on a per-pixel basis as well as intensity, effectively adding an extra dimension to the detector. We have begun to design such a detector. We are aiming at a pixel size of around 200um. Although the final design will probably require 3D integration, our first prototype will address the analog design challenges in a single-layer CMOS design before attempting a second layer to handle the significant digital I/O challenges.



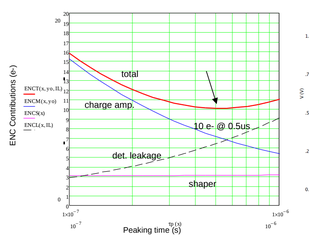
Proposed architecture of the HIXD detector. One of the problems with energy-resolving detectors with small pixels is that of charge-sharing between neighbors. If not corrected, this leads to a low-energy tail in the spectral response, which can hide weak signals below intense higher-energy peaks. This architecture attempts to reconstitute the full charge by recognizing a shared event and acquiring the charge in the neighbors. Logic in the pixel then combines these neighbor charges to re-form the full-charge event.



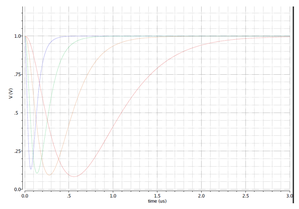
Schematic of the first circuit in the signal chain, the charge amplifier. This is typically the most critical circuit since it will dominate the noise performance of the detector. This circuit has been shown to give an ENC of around 10 electrons RMS (see the graphs following).



These graphs show the engineering tradeoffs which need to be made in designing such a circuit. There are many parameters to be fixed in such a design. In the above, the value of the feedback capacitor and the power dissipation are graphed against the filter shaping time to show their impact on the noise performance.



This graph shows the estimated total noise performance of a pixel, indicating the various system noise components.



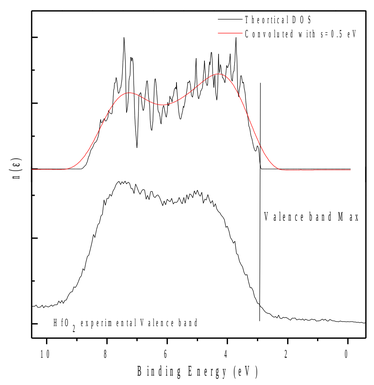
Spice simulations of the pulse shape following the shaper, based on a transistor-level design

A planar process for monolithic multi-element germanium detectors

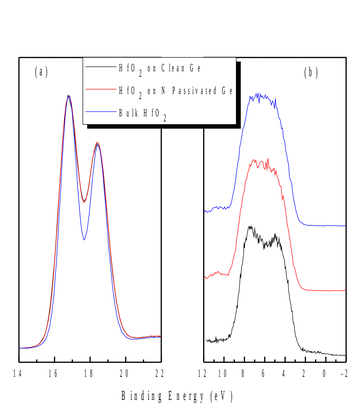
Multi-element germanium detectors have traditionally been formed by fabricating mechanically distinct sensors and then assembling them into a common cooling structure. This technology is not compatible with the fabrication of micropatterned devices such as microstrip or pixel detectors. Silicon-based detectors have had much success with a planar technology introduced by Joseph Kemmer(NIM 226 (1984) 89-93). Germanium is not at all suited to a simple modification of this technology, primarily because its oxide is unstable and water-soluble. The silicon planar process relies heavily on the excellent properties of SiO2. Our first task was therefore to find a replacement for SiO2 which was compatible with germanium. We have settled on one of the recently developed high-K dielectrics, HfO2. As part of this decision we needed to know the alignment of the band gaps of germanium and HfO2.

Band Offset Measurements: Kraut's Method

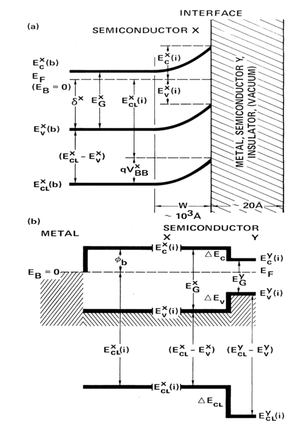
$$\Delta E_v = (E^{bulkGe}_{Ge3d} - E^{bulkGe}_{VBM}) - (E^{oxide/Ge}_{Ge3d} - E^{oxide/Ge}_{Hf4f}) - (E^{Bulkoxide}_{Hf4f} - E^{bulkoxide}_{VBM})$$

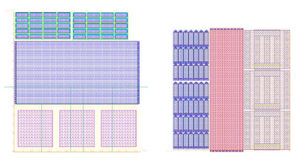


Valence band max was determined by convoluting theoretically calculated DOS to account for instrument broadening.

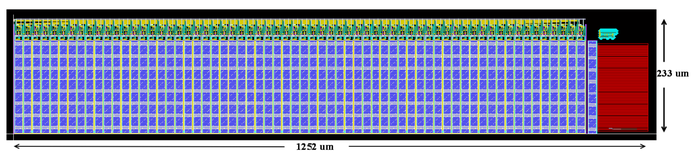


Homogenous stochiometric film with no evidence of N incorporation

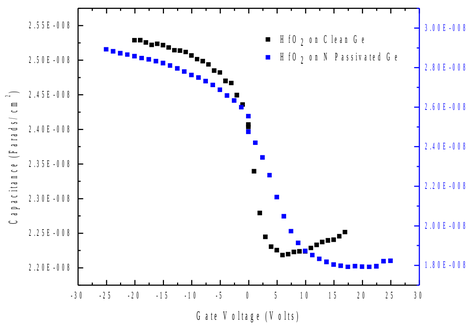




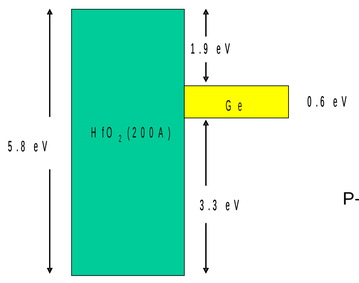
Layout of the charge amplifier in two candidate technologies, TSMC and IBM, both with 130nm design rules.



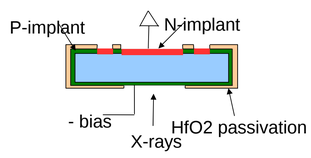
Layout for a 12-bit ADC which will digitize the analog signals produced by several pixels.



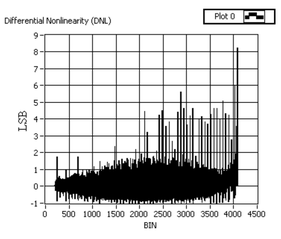
Both N passivated and clean Ge grown samples shows negative fixed charge The flat-band voltage measured for HfO2 on untreated Ge was about 0.9 V, while for the HfO2 on N passivated Ge it was about 3.1 V

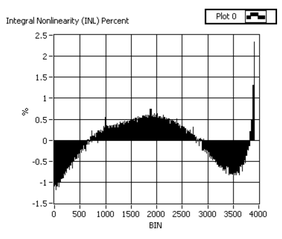


Alignment of band-gaps in HfO2 and Ge. The fact that the Ge gap is roughly centered in the HfO2 gap ensures that the HfO2 will act as a barrier equally well for holes and electrons.



Proposed structure for n-in-p photodiodes.





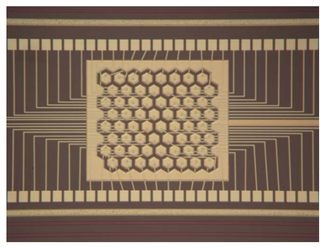
Performance of the ADC design shown above. This level of performance is adequate for our application.

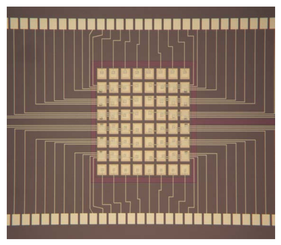
Fabrication of devices

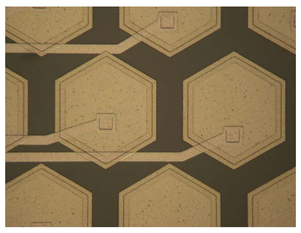
Below we show the lithography mask design used to fabricate devices, and the first wafer at a fairly late stage in its processing. The processing is greatly complicated by the relative fragility of germanium, both mechanically and chemically. It is easy to remove a significant thickness of germanium by an unwise choice of solvent or etchant.

Studying charge sharing

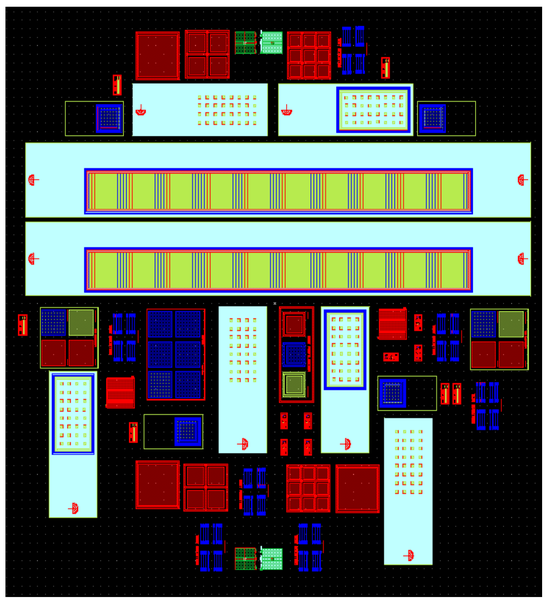
We need to gain a better understanding of events which result in the photo-generated charge being split between two or more adjacent pixels. In order to do this quickly we desinged a diode array with geometry close to that which we expect to use in our final detector, but modified to allow us to read the signals from each pixel using electronics which is already available. The electronics which is at the heart of our Maia detector system has exactly what we need for this. The amplifier ASIC used in Maia has 32 channels with alinear pitch of 125um, so we made a square array of 8 x 8 pixels and added a second metal layoer to fan out these pixels to two linear bonding pad arrays. In this way we will be able to record all detected photons, and by recording also their arrival time and pixel location, be able to reconstruct simultaneous events in neighboring pixels which must have come from a single photoabsorption. We will be able to study the limits on the reconstruction accuracy and the additional noise introduced by the need to sum channels.

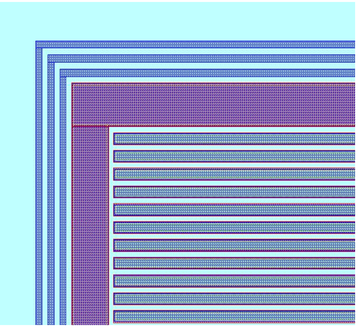




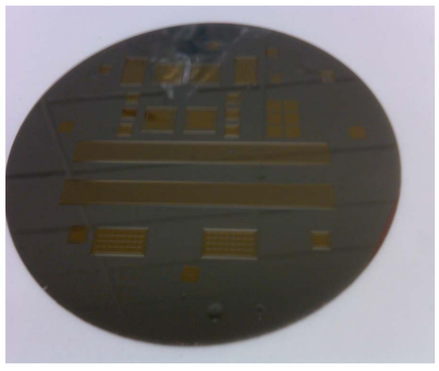


Micrographs of the diode arrays fabricated to allow early studies of charge-sharing in pixelated detectors. It is essential to develop a technique for reconstituting these split events if we are to achieve a true spectroscopic quality imaging detector.





3 inch Mask designed for Ge wafers. The design contains arrays of 1mm x 1mm diodes and a microstrip detector with 384 strips, each 4mm x 0.125mm. Above right shows an enlarged portion of the microstrip array, and to the right is a photograph of one of the 0.5mm thick germanium wafers at a late stage in the processing.



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