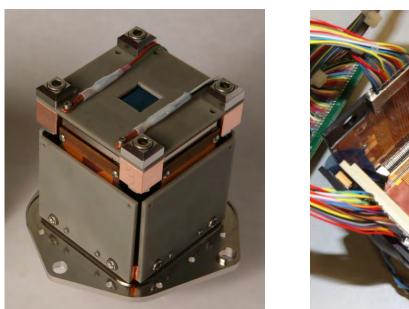
# Detector R&D at LBNL

P. Denes, N. Andresen, D. Contarato, D. Doering, D. Gnani, C. Grace, B. Krieger, J. Joseph, H. von der Lippe, P. McVittie, H. Padmore, C. Tindall, JP Walder, B. Zheng

#### Fast CCD



**Ptychography** 

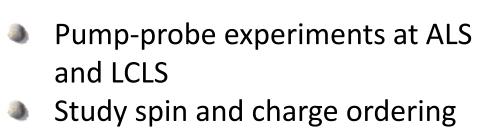
(ALS BL 9.0.3)



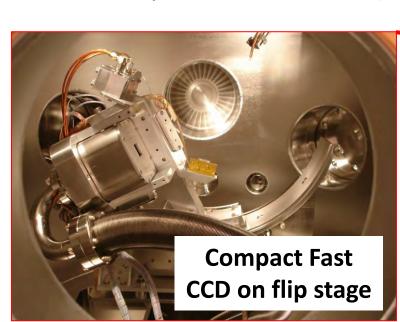
- Direct detection
- Fully-depleted, back-illuminated CCD

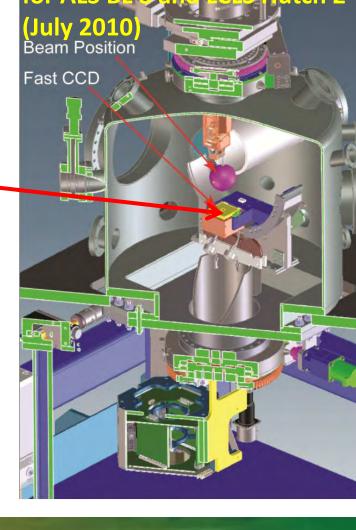
- 200 μm thick, 480×480 pixels, 30x30 μm<sup>2</sup>
- 96 outputs, (almost) column parallel
- 200 frame/s readout rate
- Custom 0.25 μm CMOS readout ASIC
- Developed in collaboration with ANL/APS
- Performance:
- 15-bit dynamic range
- 250-300 eV FWHM
- PSF < 1 pixel</p>
- Several uses at Advanced Light Source beamlines:
  - Microdiffraction
- Ptychography / STXM
- Resonant Soft X-ray Scattering
- Tomography
- High-pressure

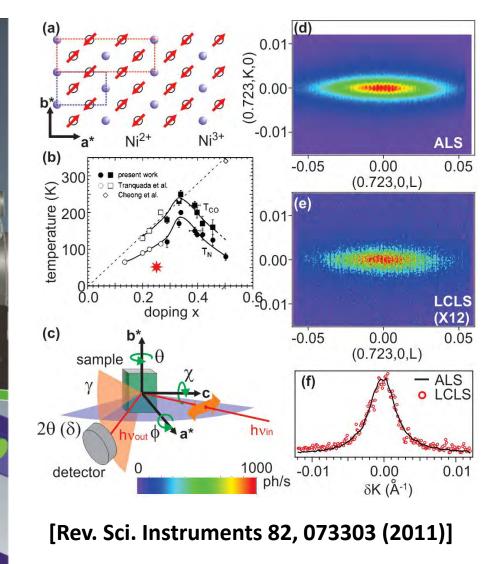
# Fast, energy resolved (ALS BL 12.3.2)



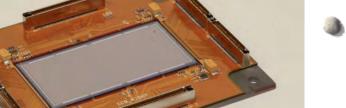
transitions in (La,Sr)<sub>2</sub>NiO<sub>4</sub> 854 eV, up to 120 frame/s (LCLS)







### 1k Frame Store CCD



desiration - Fathering

- 1920×960 pixels, two operation modes:
- 2k × 1k, 100 frame/s direct detection CCD
- shutter (Frame Store CCD)
- 192 outputs
- 200 frame/s
- Speed-enhancing buffer ASIC
- Full detector systems being developed under Recovery Act funding, to be delivered to ALS and APS in late 2011

Prototype CCD with fully

production

technology:

Megapixels/s

column-parallel readout in

288×288 pixels, 50 μm pitch

**HIPPO:** custom multi-channel

readout ASIC in 65 nm CMOS

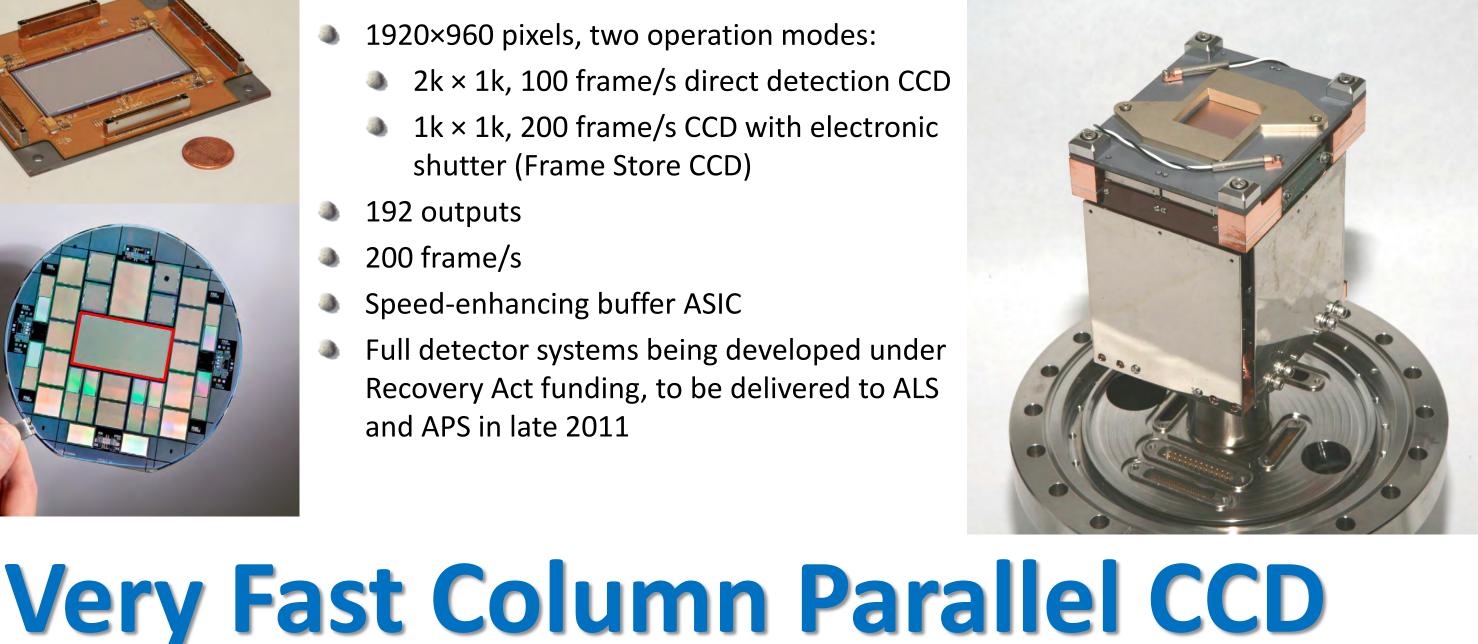
80 MHz, 12-bit ADC on 50 μm

Compression algorithms

Multiplex 4 inputs

Frame rate up to 10,000

R&D on high data rates



# Thin window R&D

- R&D on low temperature (< 500°C)</p> processes to avoid damage to sensor metallization
- Need 100 Å window thickness for O(100 eV) X-ray sensitivity Several processes under test, including in-house developments

(cold implantation, a-Si)

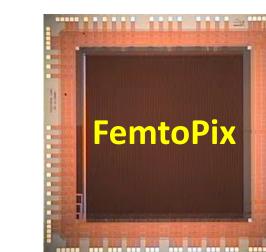
Process	Window thickness	Status
ow energy implantation + 600°C annealing	1000-2000 Å	Process dependent, several SOI prototypes functional
ow energy implantation + aser annealing	400-700 Å	Several SOI prototypes functional
-Si contact deposition by puttering	300 Å	Prototypes functional after processing, high leakage
Molecular Beam Epitaxy	50-75 Å	Building in-house capability

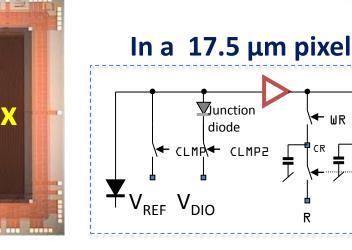
### SOI pixel R&D

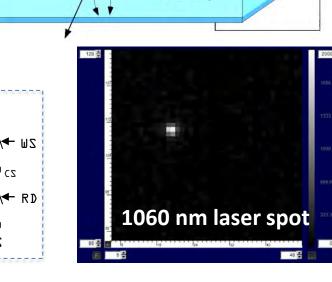
Integration of CMOS electronic and high-resistivity substrate: possibility for small pitch pixel sensors with high density, full CMOS readout



- 0.20 μm SOI-CMOS process
- 192×192 pixels, 17.5 μm pitch
- In-pixel CDS
- 4,000 frame/s readout



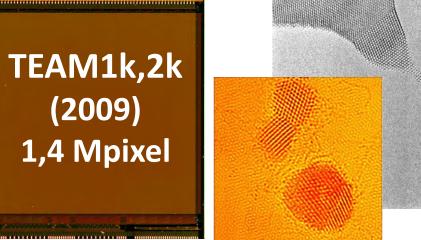




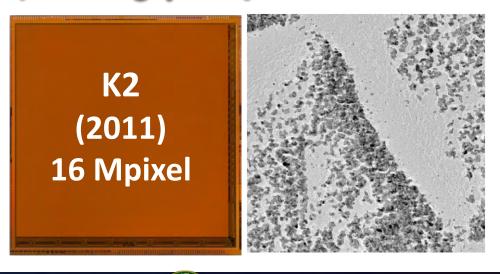
## Other synergistic activities

Development of fast, high-resolution, radiation hardened pixels for Transmission Electron Microscopy

#### 400 Megapixels/s



#### 6,400 Megapixels/s



Office of Science



U.S. DEPARTMENT OF ENERGY