CHIPS R&D Goals

**U.S. Technology Leadership**
The U.S. invents, develops, and deploys the foundational semiconductor technology of the future.

**Accelerate Ideas to Market**
A thriving ecosystem that is focused on getting the best ideas to commercial scale as quickly and cost effectively as possible.

**Robust Workforce**
A new generation of skilled workers, inventors, designers, researchers, technicians, and others able to build and sustain semiconductor manufacturing in the U.S.
CHIPS for America R&D

- To strengthen and advance U.S. leadership in R&D
- An integrated ecosystem that drives innovation
- In partnership with industry, academia, government, and allies
- A strategic view of R&D infrastructure, participant value-proposition, and technology focus areas
- Informed by the Industrial Advisory Committee
# Program Development Timeline

<table>
<thead>
<tr>
<th>National Semiconductor Technology Center</th>
<th>National Advanced Packaging Manufacturing Program</th>
<th>Manufacturing USA institute(s)</th>
<th>Metrology Program (NIST)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPRING 2023 Vision/strategy paper published</td>
<td>SUMMER 2023 Selection Committee identifies Board of Trustees</td>
<td>WINTER 2023 NAPMP vision and strategy paper</td>
<td>FALL 2023 Select topic(s); begin proposal process</td>
</tr>
<tr>
<td>NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY</td>
<td>NATIONAL INSTITUTE OF STANDARD AND TECHNOLOGY</td>
<td>NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY</td>
<td>NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY</td>
</tr>
<tr>
<td>NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER</td>
<td>NATIONAL ADVANCED PACKAGING MANUFACTURING PROGRAM</td>
<td>MANUFACTURING USA INSTITUTE(S)</td>
<td>METROLOGY PROGRAM (NIST)</td>
</tr>
<tr>
<td>USA institute(s)</td>
<td>Metrology gaps report published</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
National Semiconductor Technology Center
NSTC VISION

By the decade’s end, the NSTC should be viewed throughout the world as an essential resource within the broad semiconductor ecosystem with a network of respected scientists and engineers, state-of-the-art facilities, effective programs, and demonstrated technical achievements.
Programs

Technology leadership

Community assets

Workforce
Membership

- Businesses of all sizes and at all stages
  - Fabless companies
  - Foundries
  - Integrated device manufacturers
  - Equipment vendors
  - Materials suppliers
- Research institutions, including minority serving institutions
  - Community colleges
  - State and local governments
  - National labs
  - Labor unions
  - Sector investors
# POTENTIAL AFFILIATED TECHNICAL CENTERS

<table>
<thead>
<tr>
<th>Design tools</th>
<th>Power</th>
<th>Process and production R&amp;D</th>
<th>RF, analog, and mixed signal</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microelectromechanical systems</td>
<td>Mature node</td>
<td>Bioelectronics</td>
<td>Photonics</td>
<td>Device security</td>
</tr>
</tbody>
</table>

- Baseline CMOS and CMOS R&D
- Advanced packaging

NSTC HQ core functions
Workforce Programs

FOR SCIENTISTS, ENGINEERS, AND TECHNICIANS

- Outreach to groups, including those traditionally underrepresented
- Support scale-up of existing quality programs
- Develop novel approaches to training
National Advanced Packaging Manufacturing Program
National Advanced Packaging Manufacturing Program

- Strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem
- Leverage public-private partnerships, that can include support for facilities managed by the NSTC and MUSA
- Broad range of technologies:
  - Heterogeneous integration
  - Wafer and panel-based approaches
  - Tooling and automation
  - Substrate technology
NAPMP Approach and Target Areas

Technology innovation

Create an R&D environment advancing the state-of-the-art in advanced packaging.

Ecosystem support

Investments to bolster the growth in domestic capacity and enhance capabilities for competitive edge.

Co-design and simulation  Chiplets  Pilot packaging facilities  Tooling and automation  Materials and substrates
Pilot Packaging Facility(ies)

- The NAPMP will utilize the NSTC to support (a) packaging facility(ies) that enables R&D efforts.

- Prototype and pilot scale integration of components fabricated in NSTC facilities or 3rd party sources.

- Baseline packaging flows to support a goal of established package-proven IP.

- The facility should have sufficient tool redundancy to allow groundbreaking research on new materials and processes while still maintaining baseline capacity.

- Partnerships with domestic OSATs and electronics manufacturing services (EMS) to facilitate migration of successful prototypes to a production manufacturing environment.
CHIPS R&D Metrology Program
CHIPS R&D Metrology Program

VISION: CHIPS R&D Metrology catalyzes innovation with emphasis on measurements that are accurate, precise, and fit-for-purpose for the production of microelectronic materials, devices, circuits, and systems.

MISSION: Measure, innovate, lead to enhance a vibrant U.S. ecosystem for semiconductor manufacturing and to promote U.S. innovation and industrial competitiveness.

GOALS:
1. Expanding measurement solutions for the semiconductor ecosystem.
2. Increase the number of solvers by harnessing the diversity of people and ideas, inside and outside of NIST.
3. Expand education and workforce development opportunities that inspire excitement about manufacturing careers and expand career pathways.
Maximizing Impact and Speed
Metrology R&D

- Metrology is **foundational** and **fundamental** for all R&D programming
- Metrology **tools are delivered** to other CHIPS R&D programs;
- High impact research areas **sourced from industry**
- Metrology technologies should reach **commercial scale**
Industry Input is Key

• Measurement science for new materials and packaging
• Physical metrology for next-generation microelectronics
• Computation and data
• Virtualization and automation
• Reference materials and data, and calibrations
• Standards for processes, cybersecurity, and test methods

Strategic Opportunities For U.S. Semiconductor Manufacturing

Metrology for materials purity, properties, and provenance

Advanced metrology for future micro-electronics manufacturing

Enabling metrology for integrating components in advanced packaging

Modeling/ simulating semiconductor materials, designs, and components

Modeling/ simulating semiconductor manufacturing processes

Standardizing new materials, processes and equipment for microelectronics

Metrology to enhance security and provenance of micro-electronic based components and products

Extensive feedback from stakeholders across industry, academia, and government

CHIPS Manufacturing USA Program
Manufacturing USA Network

16 institutes
Members in every state
9 partner federal agencies

- AIM Photonics
  Integrated Photonics
  Albany, NY
  Rochester, NY
- Advanced Fibers and Textiles
  Cambridge, MA
- Modular Chemical Process Intensification
  New York, NY
- America Makes
  Additive Manufacturing
  Youngstown, OH
  El Paso, TX
- Regenerative Manufacturing
  Manchester, NH
- NeXtFlex
  Flexible Hybrid Electronics
  San Jose, CA
- Advanced Composites
  Knoxville, TN
  Detroit, MI
- Sustainable Manufacturing
  Rochester, NY
- ARM Institute
  Robotics & AI
  Pittsburgh, PA
- NIMBL
  Biopharmaceutical Manufacturing
  Newark, DE
- PowerAmerica
  Wide Bandgap Semiconductors
  Raleigh, NC
- lift
  Lightweight Materials
  Detroit, MI
- Smart Manufacturing
  Los Angeles, CA
- Digital Manufacturing & Cybersecurity
  Chicago, IL
- BioMADE
  Biindustrial Manufacturing
  St. Paul, MN
- CYMANII
  Cybersecurity in Manufacturing
  San Antonio, TX

NEW—Electrified Processes for Industry without Carbon (EPIXC)

Phoenix, AZ

DOC sponsors 1 institute + serves as the overall Program Office
DOD sponsors 9 institutes; DOE sponsors 6 institutes
Purpose: inform design of up to three Manufacturing USA Semiconductor Institutes authorized by CHIPS Act

Three public webinars held with 463 registered participants during comment period

93 comments received*

Public comment period Oct 13 – Dec 12, 2022

Public report to be released soon

RFI Responders

- Industry: 61%
- Academia: 4%
- Government: 7%
- Other: 28%

*all comments received are publicly posted at https://www.regulations.gov/docket/NIST-2022-0002/comments
Semiconductor Institute RFI Key Points

1 Institute Scope and Scale
• Several potential topic areas suggested
• No consensus on a single ‘super-sized’ all-topic institute vs. multiple focused institutes

2 Structure and Governance
• Consensus that the design framework for Manufacturing USA is sound, with exception of larger scale needed for impact in semiconductor space
• Consensus for tiered membership structures

3 Coordination
• Consensus that coordination with other CHIPS initiatives and with existing Manufacturing USA institutes in related sectors is critical

4 Sustainability
• Consensus that institutes are likely to need federal funding beyond 5 years
• Consensus that in longer-term, institutes achieve sustainability if focused on industry priorities
MANUFACTURING USA TOPIC EXAMPLES

Cross-cutting technology topics

- Productivity enhancement via early design including co-design, digital twins, and artificial intelligence
- Smart manufacturing and automation
- New and advanced materials
- Metrology and testing

Focused institute topics

- Substrate manufacturing for advanced packaging
- Sensors and microelectromechanical systems
- Infrastructure to support technology transition to manufacturing
Next Steps

- CHIPS R&D Standards Summit
  - September 26-27, 2023, in Washington, D.C.
  - And virtually
  - Sign up at CHIPS.gov

- Learn more
  - Visit CHIPS.gov
  - Get the Manufacturing USA RFI summary and NIST metrology strategy
  - Read the CHIPS Implementation Strategy and NSTC Vision and Strategy paper
  - Join our email list
Thank you