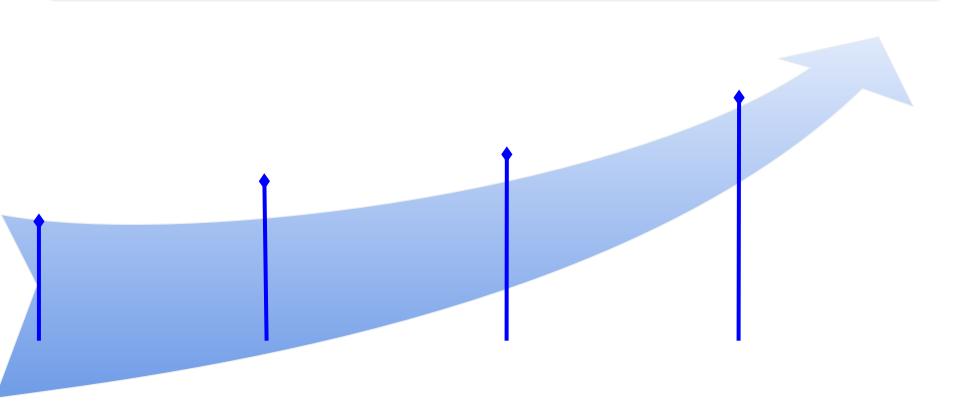
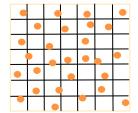


NERSC is the mission HPC facility



NERSC-9 Project Major Scope Items





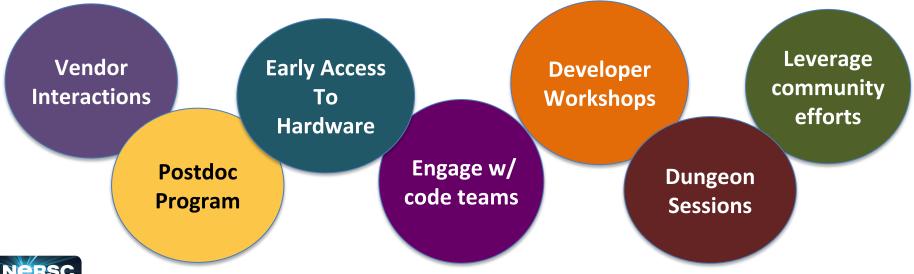
NERSC-9: A System Optimized for Science

From the start NERSC-9 had requirements of simulation and data users in mind



NERSC Exascale Scientific Application Program (NESAP)

- Prepare DOE SC users for advanced architectures like Cori
- Partner closely with ~20 application teams and apply lessons learned to broad NERSC user community.



Transitioning From KNL to AMD Processors

Codes optimized on Xeon Phi (KNL) will run well on Perlmutter

Many KNL architecture features are present on Perlmutter CPUs Many-Core MPI+OpenMP Programming Model Will Continue

Easier Onramp to "Many-Core" with Perlmutter CPUs than with KNL More Traditional Cores Single Memory Technology







NERSC already supports a large number of users and projects

from DOT COlo overented and cheemisticanal facilities

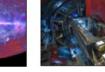




Radiation

ALS

Light Source





Palomar Transient Factory Supernova

Planck Satellite Alice Cosmic Microwave Large Hadron Collider Background

Atlas Large Hadron Collider



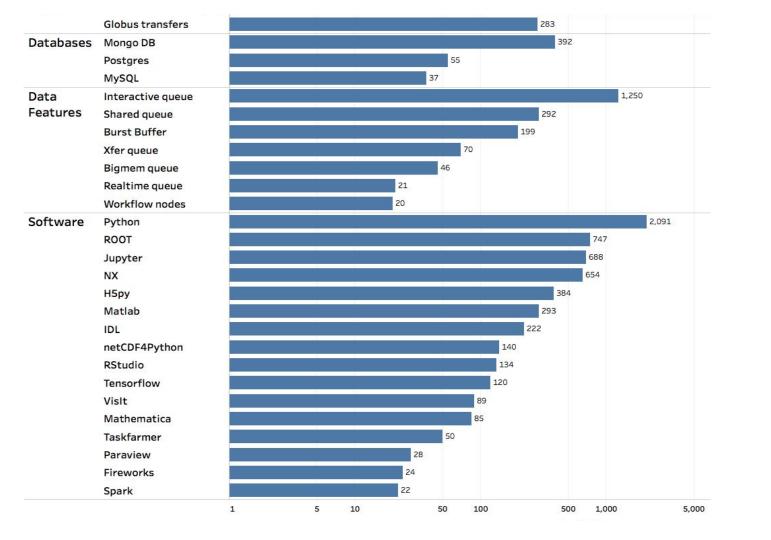
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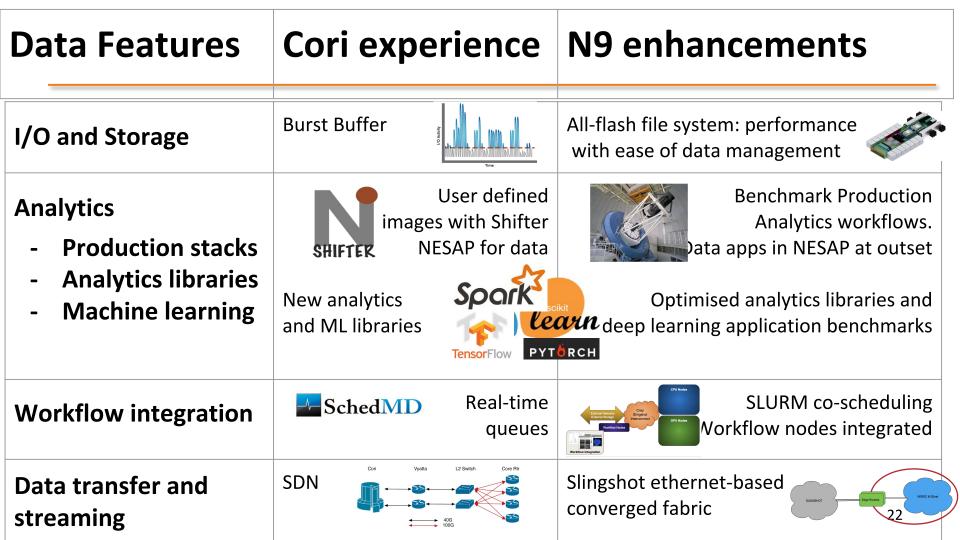


LCLS Light Source



Joint Genome Institute Bioinformatics









GPU Programming Models

We will support and engage our user community where their apps are:

CUDA: MILC, Chroma, HACC ...

CUDA FORTRAN: Quantum ESPRESSO, StarLord (AMREX)

OpenACC: VASP, E3SM, MPAS, GTC, XGC ...

Kokkos: LAMMPS, PELE, Chroma ...

Raja: SW4



Engaging around Performance Portability





NERSC is working with PGI/NVIDIA to enable OpenMP GPU acceleration

NERSC Hosted Past C++ Summit and ISO C++ meeting on HPC.



NERSC Will Pursue Membership in 2018



Doug Doerfler Leading Accepted Performance Portability Workshop at SC18. and 2019 DOE COE Perf. Port. Meeting 30

😔 🛛 Performance Portabi	lity / Measurements / Measurement Techniques	Q Search
speed and vector/instruction-sets)		
Performance Portability Introduction	 The application or algorithm may be fundamentally limited by different aspects of the system on different HPC system. 	Table of contents Measuring Portability
Office of Science Facilities ~	As an example, an implementation of an algorithm that is limited by memory bandwidth may be	Measuring Performance
Performance Portability ^ Overview	achieving the best performance it theoretically can on systems with different architectures but could be achieving widely varying percentage of peaks FLOPS on the different systems.	 Compare against a known, well-recognized (potentially non-portable), implementation.
Definition	Instead we advocate for one of two approaches for defining performance against expected or	2. Use the roofline approach to
Measurements ^ Measurement Techniques	optimal performance on the system for an algorithm:	compare actual to expected performance
Collecting Roofline on KNL		
Collecting Roofline on GPUs	 Compare against a known, well-recognized (potentially non-portable), 	
Strategy	implementation.	
Approaches ~	Some applications, algorithms or methods have well-recognized optimal (often hand-tuned) implementations on different architectures. These can be used as a baseline for defining relative performance of portable versions. Our Chroma application case-study.shows this approach. See	
Case Studies ~		
Summary		

NERSC is leading development of performanceportability.org